Palestine Polytechnic University

College of Engineering & Technology
Electrical and Computer Engineering Department
Biomedical Engineering

Graduation Project

Experimental Board for Biomedical laboratory

Project Team
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Project Supervisor

Eng. Abdullah Erman

Hebron – Palestine
July ,2004

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According to the direction of the supervisor and by agreement all of the committee member ,this project submitted to department of electrical and computer in college of engineering and technology to partially fulfill to the bachelor requirement for the department .

Supervisor signature Dept .Head Signature

Name:…….. Name:……..

Abstract

Experiment Board for Biomedical laboratory.

By

Bashar Al-Trawa

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Supervisor

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In this project we will design and implement an experimental board for the biomedical laboratory .It includes circuits as (op amp, instrument rectifier ,low pass filter, high pass filter, comparator-Schmitt trigger ,negative impedance converter ,gyrator)and bridge circuits as inputs to sensors such as (temperature ,phototransistor, pressure, etc…).With A/D converter and D/A converter.

تقوم فكرة المشروع على بناء لوحة لتجارب تستخدم في مختبر الأجهزة الطبية تتضمن الدوائر الإلكترونية المناسبة لذلك(مكبرات تشغيلية، مكبر فرقي، مرشح ترددات منخفضة نوعيه نشطه، مرشح ترددات مرتفعه نوعيه نشطه، مقوم نشط، محول المقاومة الكهربائيه، دارة جايريتر) بالإضافة إلى المجسات (حراري، ضوئي، الضغط)التي تكون ضمن قنطرة وتستوون، بالإضافة إلى محول أشارة مستمرة/رقمية ورقمية/مستمرة.

Dedication

To our parents …

To our families …

To our country …

To our supervisor Eng. Abdullah Erman …

To our friends and any one who loves us …

Bashar & Yousef & Raeid

Acknowledgments

We would like to thank our families and our friends for their support and encouragement through our study.

Also ,we would like to thank our supervisor Eng. Abdullah Erman for his efforts and his notes.

Table of contents

List of the Tables

List of Figures

Chapter One

1.1Project Overview

1.2Time plan

1.3 Report contents

Chapter One: Introduction

1.1Project Overview:

To cope with the development of technology and science in the fields that involve human beings and health care, new branch of science has emerged to the surface dealing with the biomedical instruments. This science is called the Biomedical Engineering.

The biomedical instrument is an electric device that has outputs and sensors. Biomedical instruments are very important in medicine and health fields. Through these instruments, we can examine and diagnose the state of various patients, give them treatment, and put them under continuous observation .

The biomedical engineering lab is considered the backbone for this field. It gives and supports the students with theoretical and practical information about biomedical instruments by using modern boards. These boards are comprehensive and powerful learning tools that help student study sensors and electronic circuits. These boards are used for the application of the experiments. The main purpose of each experiment is to familiarize students with the general principle involved in practical application and to achieve great understanding.

In this project we will introduce one of these equipments that supports our lab with additional sensors and experimental board coverage of fundamental modern instruments. This board consists of three units. Each unit has been carefully selected to fulfill the practical experience requirements. The first unit is the input sensor unit (U1). This unit contains the signal detecting bridge that accepts any type of sensors.

The second unit is the operational amplifier unit (U2). This unit consists of separated op-amp with resistances diodes and capacitors. They can connect whatever needed from processing: (op-amp (inverting and noninverting), instrumentation amplifier, comparators (Schmitt Trigger), low pass filter-high pass filter, instrument rectifier, and negative impedance convert (NIC). The third unit is data conversion unit (U3). It is a signal converter that is divided into A/D converter and D/A converter sections which can give us the output by indicator LEDs.

Project Cost:

- Equipment cost: It included the cost of main components of the project. Here, we list the main parts and the approximate cost of each part:
  - Electronic pieces - (40 $).
  - A/Dc D/Ac - (10 $).
  - Board printing - (20 $).
  - Other electrical and mechanical components - (40 $).
  - Additional cost - (50 $).

  Total = 160 $

- Project team expenses: It includes all the miscellaneous expenses required by the project team to accomplish this project**.** These costs are invaluable.

1.2Time plan:

The time period given to accomplish the work in this project is limited to two semesters, 15 weeks each .this section shows an illustration to the time plan which applied through the different stage to accomplish the work in the project. In the first semester, the work is divided into eight tasks are the following:

1. Selecting the project idea.

2. Discussing the idea.
3. Requirement analysis.
4. Gathering information related to the project.
5. Primary design.
6. Hardware system design.
7. Report documentation.

week / task	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Selecting the project															
Discussing the idea															
Requirement analysis															
Gathering information															
primary design															
Hardware design															
Report documentation															

Table1.1: Time scheduling in first semester.

In the second semester ,we began the real implementation of system .this work is also divided into 15 weeks .the main stages of our work at this period include:

1. Buying the components.
2. Building the boards units.
3. Testing.

1.3 Report contents:

The report is divided into five chapters; these chapters are described as follows:

Chapter one: Introduction.

Chapter two: this chapter illustrates the general block diagram and input stage which contain sensors types and how connect to Whitestone bridge.

Chapter three: contains of the detail system hardware components(op amp ,instrumentation amplifier, instrument rectifier, Schmitt trigger comparator ,low pass filter ,high pass filter, negative impedance converter, gyrator , D/Ac , A/D converters)

Chapter four: this chapter describes the testing process by showing testing stages by details .

Chapter five: conclusion and future work.

Chapter Two

2.1 Introductions

2.2 sensor unit (U1)

2.3 Measurement of instrumentation

2.4 Sensors and transducers

2.5 Wheatstone bridge

Chapter Two

2.1 Introductions

This chapter describe sensor unit (U1), then we talk about some kind of biomedical sensors as application for our projects and describe the Wheatstone bridge circuits which we will use it in the Biomedical transducers.

2.2 sensor unit (U1):

The sensor unit shown in figure (2.1) contain the signal detecting bridge circuits ,the bridge inside unit is a resistor bridge , and accepts any type of sensors which presents resistance changes as the results of the sensing .

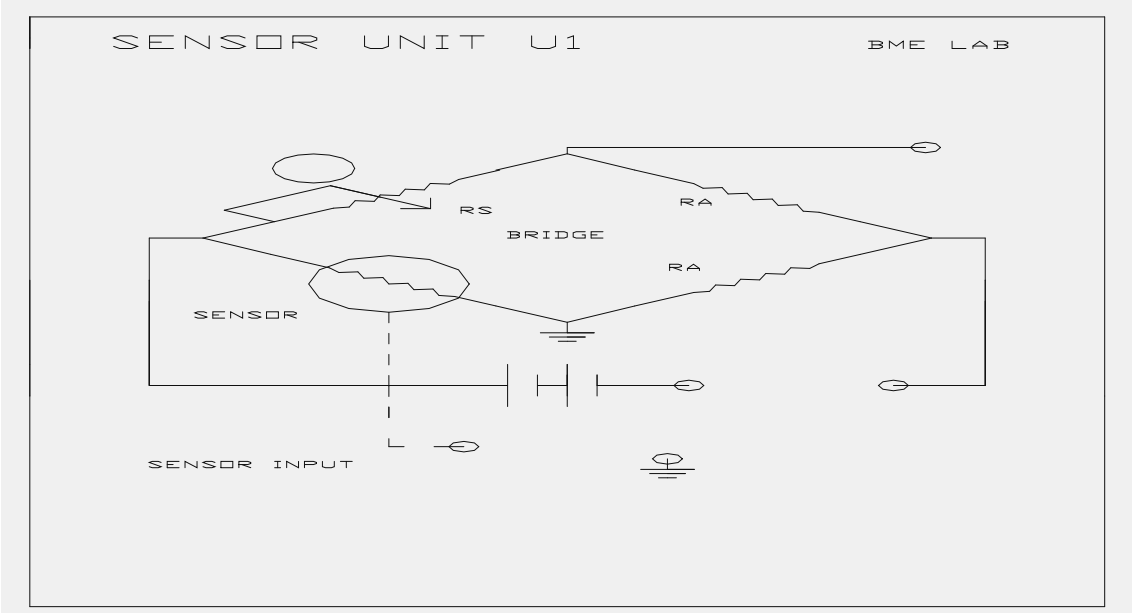
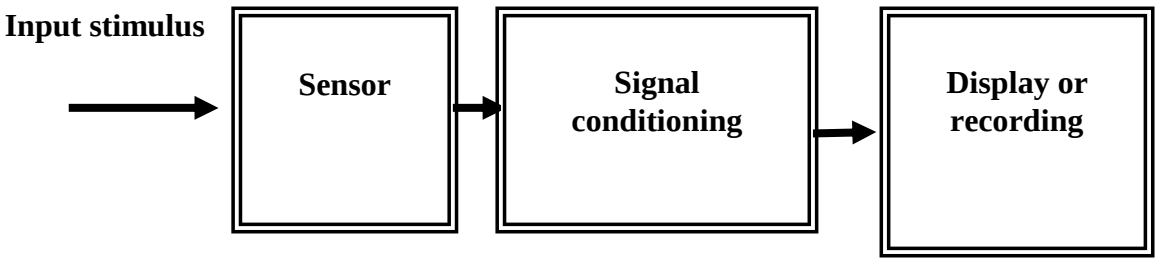


Figure (2.1): sensor unit U1

2.3 Measurement of instrumentation:

A measuring system is required to compare a quantity with a standard or to provide an output that can be related to the quantity being measured. The quantity to be measured is detected by the input sensor. The detected quantity may be converted to a mechanical form or electrical form of energy. For most biomedical purposes, the form is electrical . The measurement is greatly increased when all factors the measurement are understood. This requires a detailed knowledge of the measurement process and the possible interactions of the measurement process on the system being measured.

Most instrumentation systems comprise three basic general sections :one for sensing the measured ,the next for conditioning the sensed signal and finally one for displaying or recording the conditioned signal figure (2.2):



Figure(2.2): block diagram for experimental board system

2.4 Sensors and transducers:

The sensor and transducer are referring to measurement systems. transducers are electromechanical devices that convert a change in a mechanical quantity such as displacement or force into a change in an electrical quantity that can be monitored as a voltage after signal processing. A wide variety of transducers are available for use mechanical quantities. Transducer characteristics are determined primarily by sensor that is incorporated into the transducer to produce the electrical output.

A sensor is a device that detects a change in a physical stimulus and turns it into a signal which can be measured or recorded, normally, the sensor is just the sensing element itself.

Sensors classified according to the physical property that they use (piezoelectric, photovoltaic, etc.) or according to the function that they perform (measurement of length, temperature, etc.). Since energy conversion is an essential characteristic of the sensing process, the various forms of energy should be considered. The following table lists the main forms of energy and their occurrence:

Types of energy	**occurrence**
electrical	Electric fields, currents
magnetic	Magnetic fields
thermal	Kinetic energy of atoms and molecules
mechanical	Motion, displacement, forces

Table(2.1) : the types energy and their occurrence

2.4.1 **Photosensors:**

Photosensors are electronic control units that automatically adjust the output level of electric lights based on the amount of light detected. Lighting control devices enable occupants to control their lighting environment by either dimming the lights or switching them on and off. Some control devices, such as light switches, manual dimmers, and window blinds, can be directly accessed and controlled by occupants. Others, such as occupancy sensors, timers, and photo sensors, often are designed to take the place of occupant actions.

Photosensors are a form of automatic control that replaces or accompanies occupant control. The main reason for installing control devices is to conserve energy by switching off or dimming the electric lights when full output is not needed. The benefit of automatic control is that energy savings can occur throughout the day without human intervention. When combined with dimming electronic ballasts, photosensors can dim lights based on the amount of daylight entering a room. Problems easily arise, however, when occupants are disturbed by insufficient illumination levels or by sudden light level fluctuations. Meeting the occupants' visual and comfort needs as well as their expectations about good lighting is of primary importance for automatic lighting controls.

Photosensor respond to incident light energy, and produces an electrical signal as a result. The strength of the output signal is proportional to the intensity of the light. Some photosensor have built in light transmitters and receives. Photosensor can be

classified in terns of an optical, infrared, or a laser sensor depending upon the wavelengths of the light energy utilized.

2.4.1 LEDs and phototransistor:

Infrared LED and a receiver transistor in object detection. Two methods are use: In the first method, the transmitted light signal from the source is interrupted by the object. Therefore , the detection of an object is represented by non-existence of the light energy at the receiver(phototransistor).in contrast, the second method is based on the existence of the light signal at the receiving end that means the light source and receiver are arranged in such a way that the reflection from the object reaches the receiver.

Parameters characterize photo detection technique:

. **Light sensitivity**: the sensitivity depends on the distance between the source and object as well as the sensitivity of the receiver.

. **Response time**: a filament type lamp has a time delay due to the time taken in heating, or cooling the filament. In contrast, a semiconductor based light source response much faster when the energy source is turned on and off.

.**wavelengths:** normally, photosensor react to wavelengths of 751-950nm

.the input voltage and light output of a light source has a linear relationship within the limit.

.photosensor should be isolated from unwanted lights.

2.4.2 Temperature sensors

2.4.2.1 Thermoresistive sensors

Thermoresistive sensors Based on materials whose resistance changes in accordance with temperature, from this type the following Resistance Temperature Detectors (RTDs) the material is metal (platinum, nickel, copper) are typically used, and has positive temperature coefficients (PTC), which mean; the resistance of RTDs increases as temperature increases, and decreases as temperature decreases.

Rt=R0 [1+ α1T +α2T^2 + α3T^3+…+ αnT^n]……..2.1

Take only the first two terms and ignore the other terms from the above equation then Rt become as below.

Rt=R0 [1+ α1T]…….2.2

Where:

Rt = RTDs resistance.

T = absolute temperature in Kelvin’s.

α = material constant for RTDs.

To = standard reference temperature (K).

2.4.2.2 Thermistor (thermally sensitive resistor):

It is a thermoresitive sensor, which based on material whose resistance changes in accordance with temperature. Thermistor is a semiconductor material composes of a ceramic and metallic oxide (Mn, Co, Cu or Fe), and have negative temperature coefficient (NTC), which means (the resistance of thermistors decreases as temperature increases, and increases as temperature decreases).

Specifications of thermistor:

1.Resistivity used for biomedical applications is between 0.1-100Ω.m.

2.Small in size (they can be made less than 0.5 mm in diameter).

3.Large sensitivity to temperature changes (-3 to -5%/C).

4. Excellent long-term stability characteristics (± 0.2% of nominal resistance value per year.

$$Rt = Roe^{\wedge} [\beta (To-T)/TTo] \quad \text{…….2.3}$$

Where

Rt = thermistor resistance.

T = absolute temperature in Kelvin's.

β = material constant for thermistor it is usually 4000k.

To = standard reference temperature (K).

Sensitivity of Thermistor: sensitivity of an instrument determines how small a variation of a parameter can be reliably measure.

The definition of the temperature coefficient as a fractional change in resistance per unit change in temperature produces a result in which the fractional change in voltage per unit change in temperature is given by alpha as well.

$$sensitivity = \frac{dR}{dT} \qquad \text{…….2.4}$$

$$\frac{dR}{dt} = \left(-\frac{B}{T^2} \right) \times Rt \text{.....2.5}$$

2.5 Wheatstone bridge:

Many biomedical transducers are use in a circuits configuration called a Wheatstone bridge The basic form of Wheatstone bridge has a d.c. supply and each arm is a resistance see figure (2.3) . The resistances in the arms of the bridge (R1, R2, R3, andR4) are so adjusted that the output potential difference Vo is zero .In this condition the bridge is said to be balanced. When the output potential difference is zero then the potential at B must equal that at D .This means that the potential difference across R1 (VAB) must equal that across R3 (VAD), I1 pass through R1, I2 pass through R3.

I1R1 = I2R3 ……..2.6

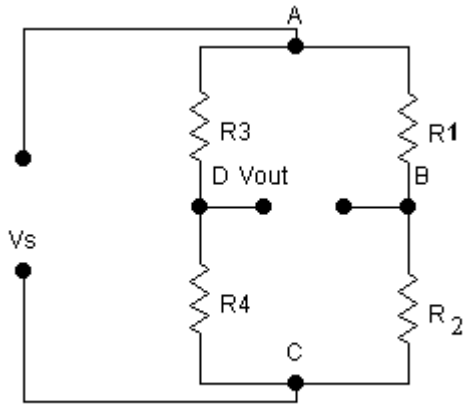
It also means that VBC must equal VDC .Since there is no current through BD then the current through R2 must be I1 and that through R4 must be I2 .Thus

$I_1R_2 = I_2R_4$ ……..2.7

Hence

$I_1R_1 = I_2R_3 = (I_1R_2/R_4)\ R_3$ ……2.8

$R_1/R_2 = R_3/R_4$ ……..2.9



Figure(2.3) : Whetstone Bridge

The balance condition is independent of the supply voltage .it depends only on the resistances in the four bridge arms .If R2 and R4 are known fixed resistances from about 1ohm to 1megaohm .The accuracy is determined by the accuracy of the known resistors and the sensitivity of the null detector .

Chapter Three

3.1 Bioelectric Amplifiers

3.2 Amplifier Circuit

3.3 Instrumentation Amplifier

3.4 Filters

3.5 Comparator

3.6 Active rectifier

3.7 Negative Impedance Converter and Gyrators

3.8 Data conversion unit (U3)

Chapter Three

This chapter talk about operational amplifier unit (U3) , OP AMP unit is shown in figure(3.1) which consisted of four OP AMP and 16 resistors with 2 potentiometers 3 diodes 3 capacitors each one separately from others . U2 introduces basics operational amplifier characteristics and applications including :instrumentation amplifier ,instrumentation rectifier ,Schmitt trigger comparator ,first and second low pass filter also high pass filter ,negative impedance converter .Then we will talk about data conversion unit U3. which contain D/A converter and A/D converter .

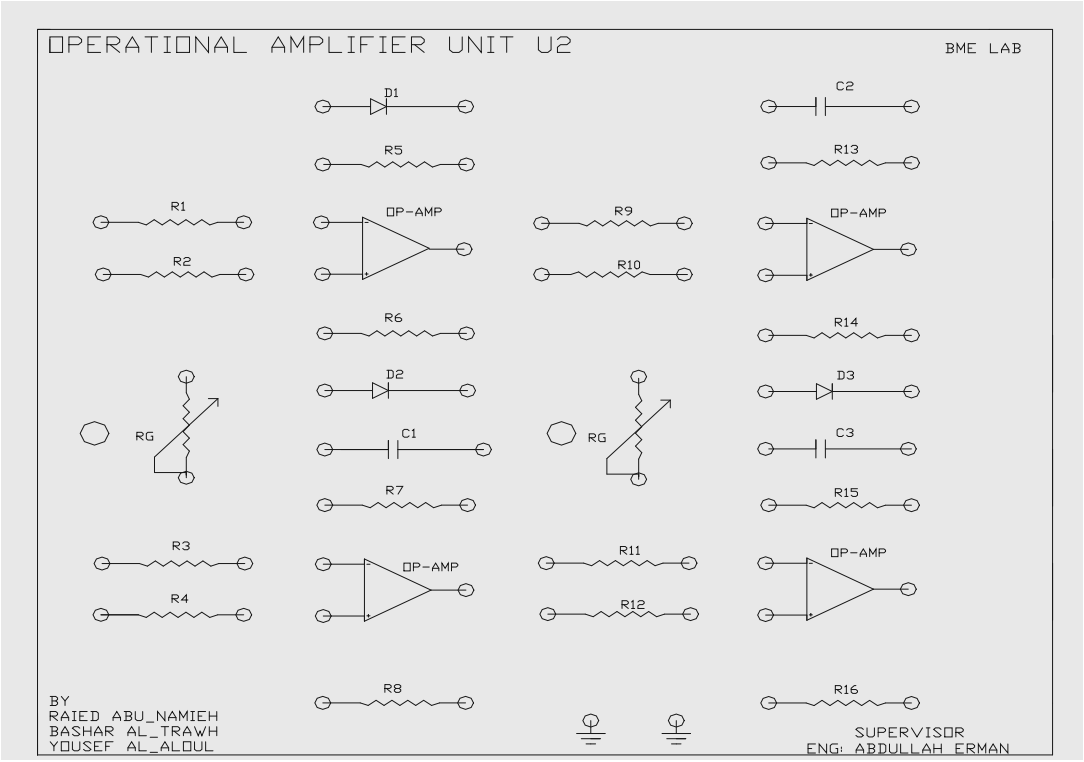


Figure (3.1): operational amplifier unit U2

3.1 Bioelectric Amplifiers:

Amplifiers used to process biopotentials are called bioelectric amplifiers, but this designation applies to a large number of different types of amplifier. The gain of a "bioelectric amplifier" for example, may be low, medium, or high (i.e., x10, x100, x1000, x 10,000). Similarly, some bioelectric amplifiers are ac coupled, while others are dc coupled. The frequency response of "typical" bioelectric amplifiers may be from dc (or near dc. i.e.: 0.05 Hz) up to 100 kHz.

The high-frequency response is the frequency where the gain drops 3 dB below its midfrequency value. In some cases the -3 dB high-frequency point will be a frequency as low as 30 Hz, but in most cases it is usually 10 kHz. Specialized models used to process specific waveforms may have a particular response ECG amplifier, for example; usually have a frequency response of 0.05 to 100 Hz**.**

A few general-purpose amplifiers have adjustable frequency response and are thus usable for a wide range of applications. In general, it is wise to use only the minimum frequency response needed to insure good reproduction of the input waveform. This practice permits rejection of high-frequency noise.

Low-gain amplifiers are those with gain factors between x I and x 10. The unity-gain (x1) amplifier is used mostly for isolation, buffering, and possibly impedance transformation between signal source and readout device. Low-gain amplifiers are often used for the measurement of action potentials and other relatively high-amplitude bioelectric events.

Medium-gain amplifiers are those that provide gain factors between x 10 and x 1000 and are used for the recording of ECG waveforms, muscle potentials, and so forth.

High-gain or low-level signal amplifiers have gain factors over x 1000. with some having factors as high as x 1.000,000. This type of amplifier is used in very sensitive measurements such as the recording of brain potentials (EEG).

Two important parameters in bioelectric amplifiers, especially those in the high- and medium-gain classes, are *noise* and drift. Drift is the (spurious) change in output signal voltage due to changes in operating temperature (rather than input signal changes). Noise, in this case, normally is the thermal noise generated in resistances and semiconductor devices. Good design and prudent component selection reduce these problems to the negligible level in modern equipment.

All three classes of bioelectric amplifiers must have a very high input impedance. This requirement is the one commonality between all bioelectric amplifiers, because almost all bioelectric signal sources exhibit a high source impedance. Most bioelectric sources have an impedance between $l0^3$ and $10^7\ \Omega$, and ordinary engineering design practices dictate an amplifier input impedance that is at least an order of magnitude higher than the source impedance. Modern amplifier (op-amp) devices have input impedances on the order of 1 tcraohm ($10^{12}\ \Omega$).

3.2 Amplifier Circuit:

Before jumping into op-amps, let's first go over some amplifier fundamentals. An amplifier has an input port and an output port. a port consists of two terminals, one of which is usually connected to the ground node. In a linear amplifier, the output signal = A ´ input signal, where A is the amplification factor or "gain." Depending on the nature of the input and output signals, we can have amplifier gain: voltage gain (voltage out / voltage in). The circuit model of an amplifier is shown in Figure(3.2). The input port plays a passive role, producing no voltage of its own, and is modeled by a resistive element R*i* called the input resistance. The output port is modeled by a dependent voltage source AV*i* in series with the output resistance Ro, where Vi is the potential difference between the input port terminals. Figure(3.2) shows a complete amplifier circuit, which consists of an input voltage source *Vs* in series with the source resistance *Rs*, and an output "load" resistance RL. From this figure, it can be seen that we have voltage-divider circuits at both the input port and the output port of the amplifier. This requires us to re-calculate V*i* and *Vo* whenever a different source and load is used:

$$Vt = \left(\frac{Rt}{Rs + Rt} \right) \text{Vs} \quad \text{.....3.1}$$

$$\text{Vo} = \left(\frac{Rl}{Ro + Rl} \right) \text{AVs} \quad \text{.....3.2}$$

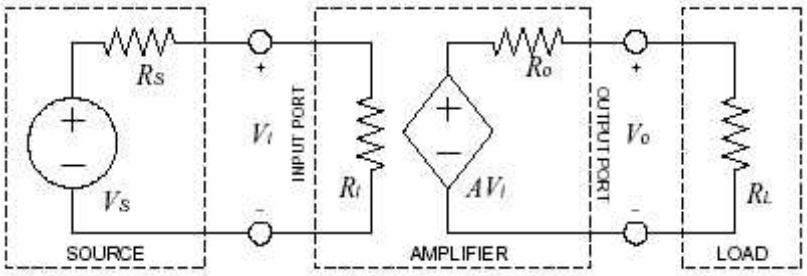


Figure (3.2): Circuit model of an amplifier circuit.

3.2.1 The Operational Amplifier: Ideal Op-Amp Model

The amplifier model shown in Figure (3.3) is redrawn in Figure (3.4) showing the standard op-amp notation. An op-amp is a "differential to single-ended" amplifier, i.e. it amplifies the voltage difference *Vp – Vn = Vi* at the input port and produces a voltage Vo at the output port that is referenced to the ground node of the circuit in which the op-amp is used.

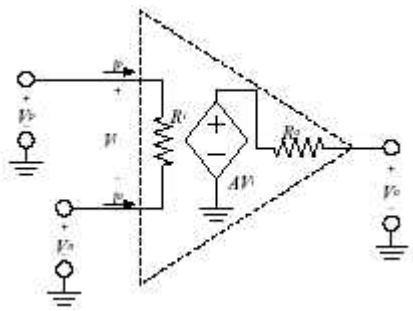


Figure (3.3) **:** Standard op-amp

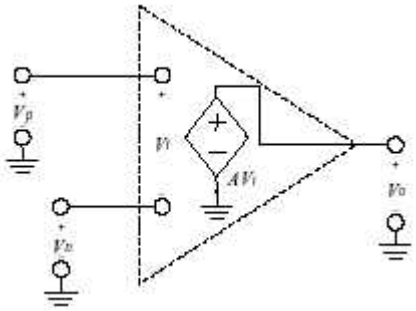


Figure (3 .4**) :** Ideal op-amp

The ideal model makes three simplifying assumptions or characteristics:

Gain is infinite: A = ∞

Input resistance is infinite: R*i* = ∞

Output resistance is zero: R*o*= *0*

Applying these assumptions to the standard op-amp model results in the ideal op-amp model shown in Figure (3.4) . Because R*i* = ∞ and the voltage difference Vp – Vn= Vi at the input port is finite, the input currents are zero for an ideal op-amp:

in = ip = 0

Hence there is no loading effect at the input port of an ideal op-amp:

Vt=Vs

In addition, because *Ro* = 0, there is no loading effect at the output port of an ideal op-mp:

$Vo = A \times Vi$ ……..3.3

Finally, because A = ∞ and Vo must be finite, $Vi = Vp - Vn = 0$, or

Vp = Vn

3.2.2Open loop gain:

A_{OL} is the ratio of a change of output voltage to the change input voltage which is applied directly to the amplifier input terminals(not dependent on the circuits).at ideal voltage amplifier we will get infinite open loop gain then:

$a \to \infty$

and ideal characteristics:

$r_d = \infty$

$r_o = 0$

$i_p = i_n = 0$

so A dependant on a .

3.2.3 Closed loop gain:

A_{CL} In closed loop gain we refer to as ideal so:

Let $a \to \infty$

Then:

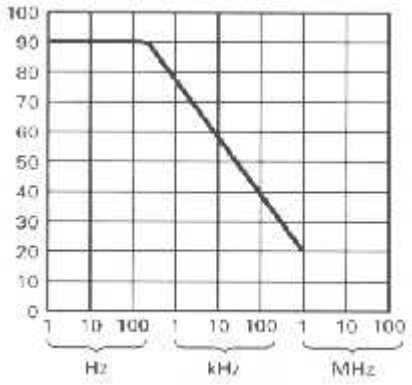
$A_{ideal} = \lim_{a \to \infty} A$ ……..3.4

so the gain here independent of a and determine by the external resistance ratio.

3.2.4COMMON MODE REJICTION RATIO:

The common mode rejection ratio (CMMR)is defined as the differential voltage gain divided by common mode voltage gain :

$$CMMR = \frac{A}{Acm} \quad \text{……..3.5}$$



Figure(3.5): frequency response

Some care must be exercised in designing a circuit ,the higher CMMR the better ,A higher CMMR means that amplifying the wanted signal and discriminate against the common mode signal, data sheet usually specify CMMR in decibels :

$CMMR_{dB}$ =20 log CMMR…….3.6

3.2.5 Bias And Offsets :

A diff amp has input bias and offsets that produce an output error when there is no input signal in many applications. When this false signal is amplified unwanted dc voltage V_{error} appear across the out put.

In many cause V_{error} can be ignored .such as in ac amplifier not important but at some kind precision dc amp needs to be taken into account .

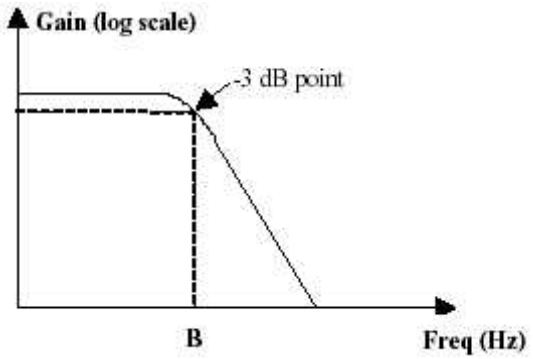
Then by using nulling circuit we eliminate the bias current by using equal base resistors

.

Also to eliminate the effect of an input offset current and voltage using potentiometer by adjust this potentiometer with no input signal ,we can null or zero the output voltage.

3.2.6 Frequency Response:

The frequency response of an amplifier is the graph of its gain versus the frequency . The gain expressed in dB is 20 log10|G|. The frequency response of an op-amp is a low pass characteristic (*i.e.* passing low-frequency signals, attenuating high-frequency signals) as shown in Figure(3.6):



Figure(3.6) : Frequency response of op-amp.

The unity- gain frequency is the frequency at which the voltage gain equal 1. data sheet .Usually specify the value of f_{unity} because it represent the upper limit on the useful gain of an amp. The bandwidth is the frequency at which the power of the output signal is reduced to half that of the maximum output power. This occurs when the gain drops by 3 dB. In Figure (3.6) , the bandwidth is B Hz. For all op-amps, the Gain*Bandwidth product is a constant. Hence, if the gain of an op-amp is decreased, its operational bandwidth increases proportionally. This is an important trade-off consideration in op-amp circuit design. , we assumed that the op amp has infinite bandwidth.

3.2.7 Slew rate :

The initial slop of the exponential wave form by compensating inside a capacitor is called slew rate :

$$S_R = \frac{\Delta v_{out}}{\Delta t} \quad \text{……..3.7}$$

this refer to the fastest response that op amp can have ,the data sheet of op amp always specifies the slew rate because this quantity limits the average signal response of an op amp, if the out put sine wave is very small or the frequency is very low , slew rate will distort the out put signal :

$S_s = 2\Pi f V_P$ ……3.8.1

S_s : initial slope of sine wave

f: frequency

V_P : peak value

To avoid slew rate distortion of sine wave , S_s has to be less than or equal to S_R .when the two are equal we are at the limit on the average of slew rate distortion at this :

$S_R = S_s = 2\Pi f V_P$ ……..3.8.2

Solving fore f:

$$f_{\max} = \frac{S_R}{2\Pi V_P} \text{ …….3.9}$$

where f_{max} or (band width-large signal bandwidth of op amp) is the highest frequency that can amplified without slew rate distortion.

3.3 Instrumentation Amplifier

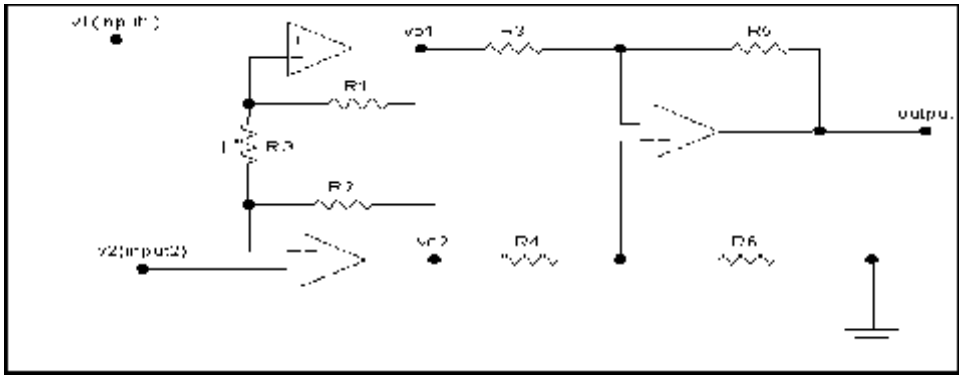
Instrumentation amplifier, which is a differential voltage gain device that amplifies the difference between the voltages existing at its two input terminals, the main purpose of an instrumentation amplifier is to amplify a small signals riding on large common voltage.

The characteristics of instrumentation amplifier:

1- High input impedance.
2- High common mode rejection ratio.
3- Low output offset.
4- Low output impedance.

A basic instrumentation amplifier is made up of three operational amplifiers, and resistors. The voltage gain is set with external resistor (RG). The voltage gain is given by

$$A_V = \frac{V_{OUT}}{Vin} \qquad \text{…….3.10}$$



Figure(3.7): Instrumentation Amplifier

Derive of gain equitation:

Assume A_3 unity gain ($R_3 = R_4 = R_5 = R_6$)

$$V_{O2} = \left(\frac{R_2}{R_G} + 1\right) V_2 - V_1 \left(\frac{R_2}{R_G}\right) \text{……..3.11}$$

$$V_{O1} = \left(\frac{R_1}{R_G} + 1\right) V_1 - V_2 \left(\frac{R_1}{R_G}\right) \text{……..…3.12}$$

Assume $R_1 = R_2$

$$V_{O2} - V_{O1} = (V_2 - V_1)\left(\frac{R_2}{R_1} + 1\right) + (V_2 - V_1)\left(\frac{R_2}{R_G}\right) \text{…….3.13}$$

$$V_{O2} - V_{O1} = (V_2 - V_1)\left(\frac{R_2}{R_G} + 1 + \frac{R_2}{R_G}\right) \text{.....3.14}$$

$$V_{O2} - V_{O1} = (V_2 - V_1)\left(\frac{2R_2}{R_G} + 1\right) \text{.....3.15}$$

$$A_v = \frac{2R_1}{R_G} + 1 \text{ .....3.16}$$

then if A_3 non zero

$$A_V = \left(\frac{2R_1}{R_G} + 1\right)\left(\frac{R_5}{R_3}\right) \text{.....3.17}$$

3.4 Filters:

There are many types of medical instruments in which it is necessary to select the frequency components of the input signal because the signal generated with range of frequencies. It is often necessary to use filter to select the signals with wanted frequencies and reject the signal unwanted frequencies, in electroencephalograph (EEG-measure the electrical activity of brain), various brain states, and produce distinctive frequency band frequency band 4-8Hz indicate sleep,13-22Hz indicate a high state of alertness.

Filters may be used to direct these frequency bands to different channels to facilitate signal processing and disease diagnosis. filtering is useful in reducing noise.

❖ Active filter :

A filter can be either passive or active filter; passive filters are built with resistors, capacitors, and indicators. Active filters are built with resistors, capacitors, and op amps.

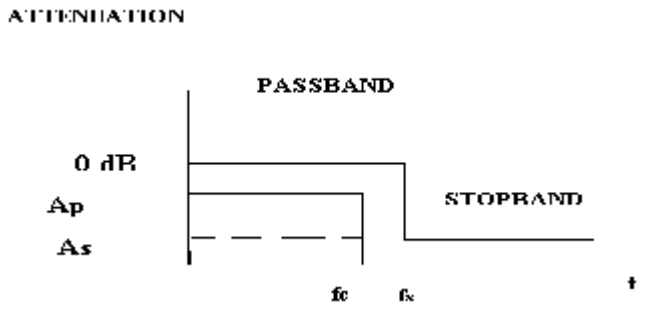
filter are usually categorized in manner which the output voltages varies with frequance of input voltage.

3.4.A passband and stopband attenuation :

it is the loss of signal with constant input voltage :

$$Attenuation = \frac{V_{out}}{V_{out(mid)}} \quad \text{……..3.18}$$

then the passband is set frequency between 0 and f_c (cutoff frequency).the stopband is all the frequency above f_S . The transition region is between f_c and f_S (stopband frequency). see figure (3.8) :



Figure(3.8): realistic low pass response.

the five approximation trade off the characteristics of passband ,stopband .transition region .

3.4.B filter Approximate response :

each type of filter can be designed using five approximation used as compromise for ideal response to dealing with practical circuits . the approximation chosen by what acceptable application.

3.4.B.1 Butterworth Approximation:

The passband attenuation is zero through most of the passband and decrease gradually to A_P (gain passband) at edge of bass band , above edge the frequency the response rate roll off

roll off= 20n dB/decade …….3.19

n: order of the filter

the flat response is in passband.

The advantage of Butterworth is the flatness of the passand ,the major disadvantage is the relatively slow rate compared with other approximation.

3.4.B.2 Chebysheyev Approximation:

In some application a flat response is not important such as chebysheyev this preferred because it roll off faster in transition region than Butterworth filter. because of this the attenuation with a chebysheyev filter is always greater than the attenuation of the Butterworth .

Ripple= $\frac{n}{2}$ …….3.20

3.4.B.3 Inverse Chebyshev Approximation

it has a flat passband response and rippled stopband response. the roll off rate in the transition region is comparable to roll off rate a chebyshev filter.

3.4.B.4 Elaiptic Approximation:

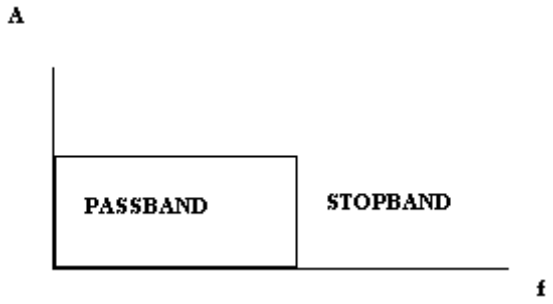
if we need fastest possible roll off in the transition region if rippled stopband and the ripple passband is acceptable . this give us optimized transition region.

3.4.B.5 Bessel Approximation:

The Bessel approximation has a flat passband a monotonic stopband similar to those of the Butterworth approximation .however the roll off in the transition region is much less with a Bessel filter than with a Butterworth.

The Bessel approximation is producing a linear phase shift increase with frequency .

3.4.1 Low pass filter :



Figure(3.9): ideal low pass response

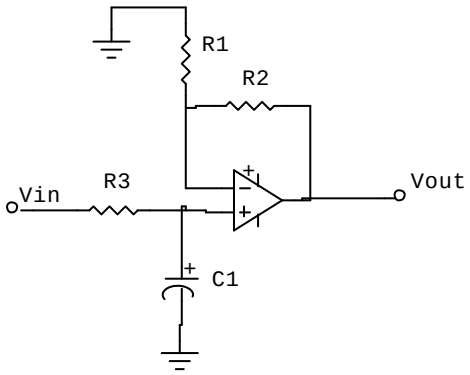
The low pass filter has the output frequency response ,the frequency of input signal voltage increase ,the output voltage decreases slightly .

when the input frequency reaches the upper critical (or break)frequency (f_c) ,the output voltage has decreased to 70.7 % of the maximum output voltage. Which pass

all frequencies from zero to the cut off frequency and block all frequencies above cut off frequency.

3.4.1.1 first order Low-pass filter:

First order noninverting low pass active filter, it has RC lag Figure(3.10):



figure(3.10)first order low pass stage

$$V_O = \left(1 + \frac{R_2}{R_1}\right) V_C \quad \text{……3.21}$$

But:

$$K = \left(1 + \frac{R_2}{R_1}\right) \quad \text{……..3.22}$$

$$V_C = \frac{1/J2\Pi f_C}{R_i + 1/j2\Pi f_C} \quad \text{…….3.23}$$

Multiple Vc:

$$V_C \times \frac{1}{j\,2\,\Pi\,f_C}$$

Then:

$$V_C = \frac{1}{1+ j2\Pi f R_i C}\ \text{Vin} \quad \ldots\ldots\ldots\ldots\ldots\ldots 3.24$$

substitute eqauation 2.2 in 1:

$$\frac{V_O}{V_i} = k\left(\frac{1}{1+ j2\Pi f R_i}\right)$$

$$\left|\frac{V_O}{Vi}\right| = \frac{k}{\sqrt{1+\left(\ j2\Pi f\ R_i\ \right)^2}} \quad \ldots\ldots\ldots\ldots\ldots\ldots 3.25$$

the cut off frequency at critical is given by:

$$\left|\frac{V_O}{Vi}\right| = \frac{1}{\sqrt{2}} \quad \ldots\ldots\ldots\ldots 3.26$$

$$2\Pi f_C R_i C = 1$$

then $f_c = \frac{1}{2\Pi RiC}$ ……..3.27

$$\left|\frac{V_O}{V_i}\right| = \frac{k}{\sqrt{1+\left(\frac{f}{f_C}\right)^2}} \quad \text{……3.28}$$

3.4.1.2 low pass filter second order:

second order or 2-pole stages Sallen-key, it consisted from two capacitor and two resistor, second order has a resonant frequency and a Q to determine how much peaking occurs, the roll off will be -40dB/decade.

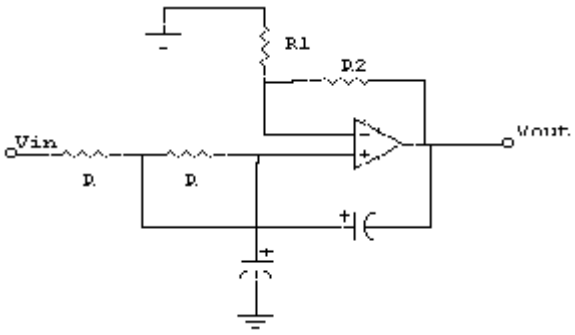


Figure (3.11): second order low pass filter

With kirchhoffs current low at node one:

$$I_1 = I_2 + I_3 \quad \text{……..3.29}$$

or

$$\frac{V_{in} - V_A}{R_2} = \frac{V_A - V_O}{1/SC_2} + \frac{V_A - V_1}{R_3} \quad \text{……..3.30}$$

by divider rule:

$$V_1 = \frac{1/SC_3}{R_3 + 1/SC_3} V_A \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 3.31$$

since $R_i = \infty, I_B \cong 0A$

$$= \frac{V_A}{R_3C_3S + 1}$$

$$V_A = (R_3C_3S + 1)V_1 \ldots\ldots\ldots\ldots\ldots 3.32$$

substituting equation * in equation ** :

$$V_1 = \frac{(R_3)(V_{in}) + (R_3R_2C_2S)V_O}{(R_3C_3S + 1)(R_2 + R_3 + R_3R_2C_2S) - R_2} \ldots\ldots\ldots\ldots\ldots 3.33$$

however:

$$V_O = (A_F)V_1 \ldots\ldots\ldots\ldots\ldots\ldots 3.34$$

where $A_F = 1 + \frac{R_F}{R_1}$ ……..3.35

therefore ;

$$V_O = \frac{A_F[(R_3)(V_{in}) + (R_3R_2C_2S)(V_O)]}{(R_3C_3S + 1)(R_2 + R_3 + R_3R_2C_2S) - R_2} \ldots\ldots\ldots\ldots\ldots 3.36$$

solving the equation for V_O/V_{in} :

$$\frac{V_O}{V_{in}} = \frac{A_F}{S^2 + \frac{(R_3C_3 + R_2C_3 + R_2C_2 - A_F R_2C_2)}{R_2R_3C_2C_3} + \frac{1}{R_2R_3C_3C_2}} \quad \ldots\ldots\ldots\ldots\ldots\ldots 3.37$$

for the frequency above fp the gain of second – order low pass filter rolls off at rate of – 40 dB/ decade . with two real and equal roots this mean:

$$w_p{}^2 = \frac{1}{R_3R_2\ C_3C_2} \quad \ldots\ldots\ldots\ldots\ldots\ldots 3.38$$

or

$$w_p = \frac{1}{\sqrt{R_3R_2\ C_3C}} \quad \ldots\ldots\ldots\ldots\ldots\ldots 3.38^*$$

$$F_P = \frac{1}{2\Pi\sqrt{R_2R_3C_2C_3}} \quad \ldots\ldots\ldots\ldots\ldots\ldots 3.39$$

3.4.2 High pass filter:

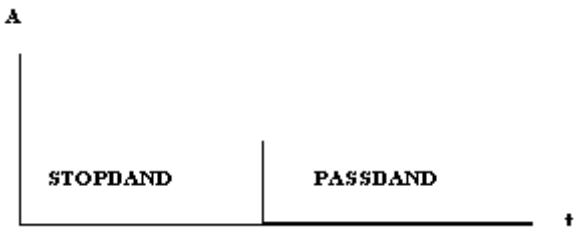


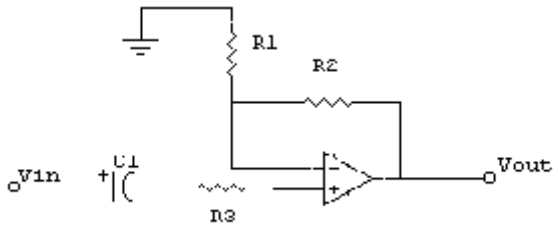
Figure (3.12): ideal high-pass response.

The high pass filter has the output frequency response ,the frequency of input signal voltage increase ,the output voltage increase slightly .

when the input frequency reaches the above critical (or break)frequency (f_c) ,the output voltage has increase to 70.7 % of the maximum output voltage. Which pass all frequencies above the cut off frequency and block all frequencies below cut off frequency.

3.4.2.1 High pass filter first order:

First order noninverting highpass active filter the voltage gain:
Figure (3.13):



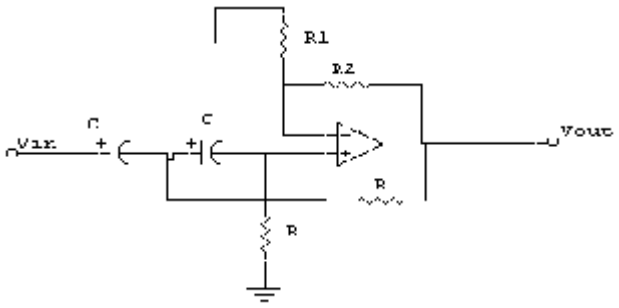
figure(3.13): first order high pass stages .

$$Av = \frac{R_2}{R_1} + 1 \qquad \text{…….3.40}$$

the 3 dB frequency is given by :

$$f_c = \frac{1}{2\Pi R_3 C_1} \qquad \text{……..3.41}$$

3.4.2.2 high pass filter second order:



Figure(3.14): Second order high pass filter

f_b : pole frequency

with second order low pass filter:

at $R_2 = R_1$ & $C_1 = C2$ then

$$Av = \frac{R_2}{R_1} + 1 \quad \text{…….3.42}$$

$$Q = \frac{1}{3 - A_V} \quad \text{……..3.43}$$

$$f_p = \frac{1}{2\Pi RC} \quad \text{…….....3.44}$$

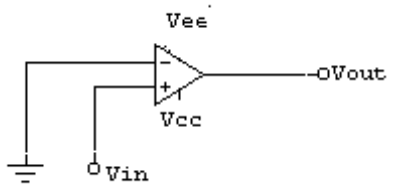
3.5 Comparator:

Often we want to compare one voltage with other to see which is larger. Comparator is similar to an op amp because it has to input voltage (noninverting and inverting) and one out put voltage.

Then the pacemaker from the most application area the comparator play one of the most important roll to provide electronic digital pulse to determine the energy delivered to the heart.

Ideal comparator:

To build comparator is to connect an op amp that has an open loop gain (A_{OL}) that is finite (∞) see figure(3.15):



figure(3.15): ideal comparator

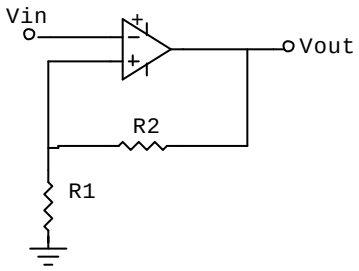
The minimum input voltage that produce saturation is :

$$V_{in} = \frac{\pm V_{sat}}{A_{OL}} \quad \text{.....3.45}$$

if the input voltage more $\pm V_{in\ (\min)}$ the output voltage will go to more positive or negative saturation .

SCHMITT TRIGGER:

if the input to comparator contains a large amount of noise, the out put will be effect with the noise , then by using a comparator with positive feed back this will prevent noise because produce two separate trip point. A comparator with positive feedback called a Schmitt trigger



Figure(3.16): Schmitt Trigger

When the comparator is positively saturated, a positive voltage is feedback to the noninverting input. This positive feed back voltage holds the out put in the high state. if the output negatively saturated a negative fed back to noninverting input , holding the output in the low state .the feed back fraction:

$$B = \frac{R_1}{R_1 + R_2} \quad \text{…….3.46}$$

When the output is positively saturated, the reference voltage applied to the noninverting input is:

$$V_{ref} = +BV_{sat} \quad \text{…….3.47}$$

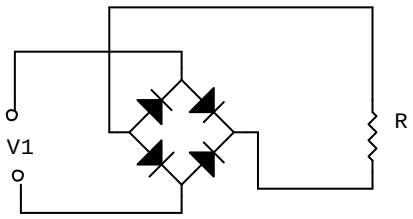
When the output is negatively saturated, the reference voltage is:

$$V_{ref} = -BV_{sat} \quad \text{…….3.48}$$

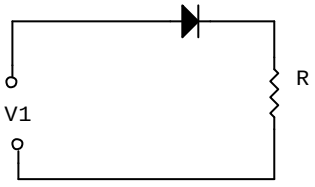
The output voltage will remain in a given state until the input voltage exceeds the voltage for that state.

3.6 Active rectifier:

Semiconductor diodes that are connected in the half and full wave rectifier circuits in will have the output waveforms for sinusoidal inputs.



figure(3.17):full wave



figure(3.18):half wave

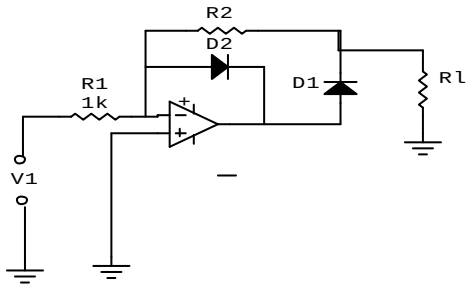
These waveforms cause operation of the diode in the normal operating region for most of the input cycle.

The input voltage for rectifier is usually much larger than 0.7 volts, therefore there are no problems.

In some medical applications there are problems in some times exist to rectify very small AC voltages in millivolt such as the ECG signal , if the input voltage is less than 0.7 volts , which is the barrier voltage of silicon diodes , the diode is not operating in the normal range . For these low voltages, the diode is not turned on even though the diode is biased forward. this problem can be overcome by placing the diode within the feedback loop of an op amp.

3.6 Instrument Rectifier

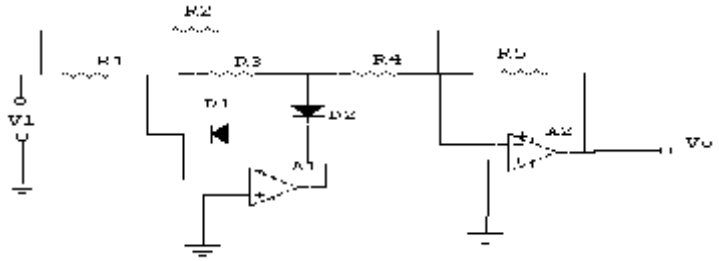
Half wave rectifier When the input signal goes positive output goes positive and turns on the diode. and the positive half cycle appears across the load resistor. input goes negative, the op-amp output goes negative and turns off the diode. Since the diode is open, no voltage appears across the load resistor. The final output is almost a perfect half-wave signal.



Figure(3.19): Half wave rectifier

There are two distinct *modes* or regions of operation. First, when the input voltage is positive, the diode is conducting and the operation is linear. In this case, the output voltage is fed back to the input, and we have negative feed. back. Second, when the input voltage is negative, the diode is nonconducting and the feedback path is open. In this case, the op-amp output is isolated from the load resistor.

Full wave rectifier as the fig(3.21) we will a have a full wave out put .during the nonconducting half cycle of the diode D_2 ,the input positive voltage is applied to the output through resistors R22 this adds the order half cycle to the output to produce the full wave rectifier out put.



Figure(3.20):full wave rectifier

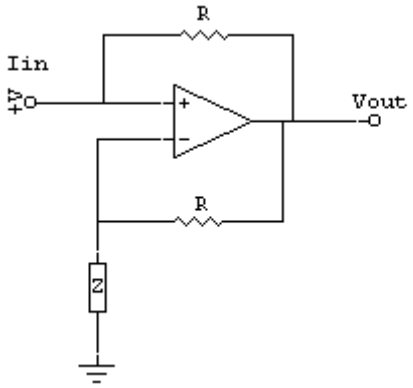
3.7 Negative Impedance Converter and Gyrators

These two device can mimic properties of inductors while using only resistors and capacitors in additional to op amp.

3.7.A NIC circuits:

The NIC they used op-amp ,resistors ,capacitors, it converts impedance to its

negative Z_{in} = -Z, the NIC there for converts a capacitor to a "back ward" inductor:



figure(3.21):NIC

$$i_{in} = \frac{V_{in} - V_O}{R} \quad \text{.....3.49}$$

$$V_O = \left(1 + \frac{R}{Z}\right) V_{in} \quad \text{.....3.50}$$

substituting equation 1 in equation 2 :

$$i_{in} = \frac{V_{in} - \left(1 + \frac{R}{Z}\right) V_{in}}{R} \quad \text{.....3.51}$$

then :

$$\frac{V_{in}}{i_{in}} = Z_{in} = -Z \quad \text{.....3.52}$$

if Z capacitor then :

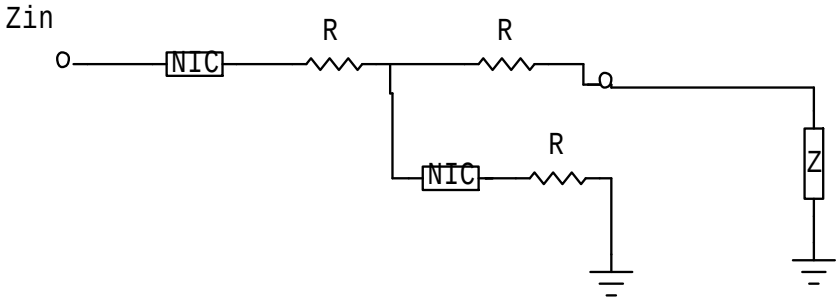
$$Z_C = \frac{1}{jwc} \rightarrow Z_{NIC} = \frac{-1}{jwc} = \frac{j}{wc} \quad \text{.....3.53}$$

it mimics a backward inductor (inverse proportional with frequency)

3.7.B Gyrator:

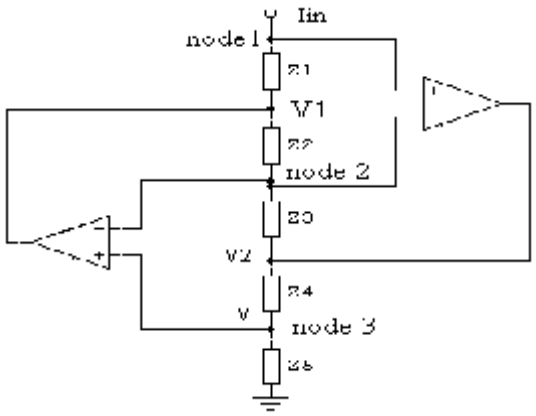
whereas the gyrator converts an impedance to its inverse $Z_{in} = \frac{R^2}{Z}$. The gyrator coverts capacitor to true inductors :

$$Z = \frac{1}{jwc} \rightarrow Z_{in} = jwcR^2 \quad \text{……..3.54}$$



Figure(3.22):gyrator

- **Generalized impedance converter**:



figure(3.23): Generalized impedance converter.

with node analysis:

$$I = \frac{V - V_1}{Z_1} \quad \text{…….3.55}$$

$$\frac{V_1 - V}{Z_2} + \frac{V_2 - V}{Z_3} = \ 0\ .\ 0 \quad \text{…….3.56}$$

$$\frac{V_2 - V}{Z_4} + \frac{0 - V}{Z_5} = 0.0 \quad \text{……..3.57}$$

from equation(3.55):

$-V_1 = IZ_1 - V$ then $V_1 = V - IZ_1$ ……..3.58

substituting equation * in equation (3.56) :

$$\frac{V - IZ_1 - V}{Z_2} + \frac{V_2 - V}{Z_3} = 0$$

so:

$$-\frac{IZ_1}{Z_2} + \frac{V_2 - V}{Z_3} = 0 \Rightarrow \frac{IZ_1}{Z_2} = \frac{V_2 - V}{Z_3}$$

$$V_2 - V = \frac{IZ_1 Z_3}{Z_2}$$

$$\Rightarrow \qquad V_2 = \frac{IZ_1 Z_3}{Z_2} + V \qquad \text{……3.59}$$

we sub . equation (3.58)in equation (3.57):

$$\frac{\left(I\frac{Z_1Z_3}{Z}\right)+V-V}{Z_4}-\frac{V}{Z_5}=0$$

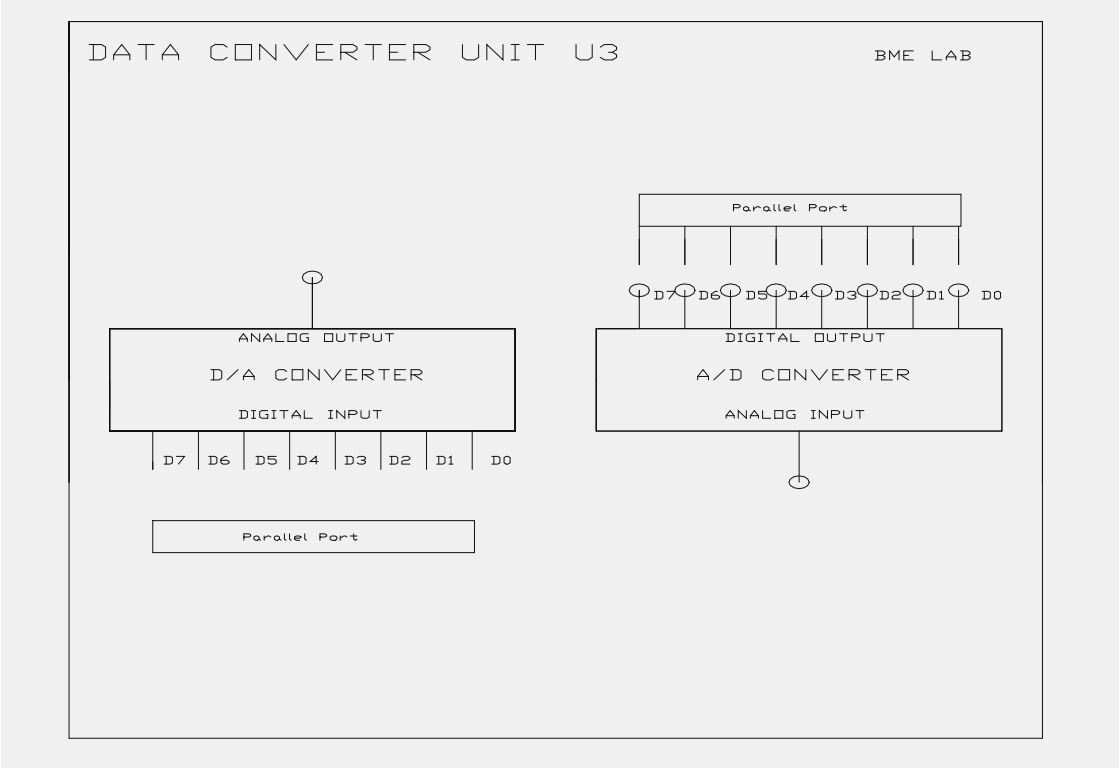
$$\Rightarrow \qquad \frac{IZ_1Z_3}{Z_2Z_4}=\frac{V}{Z_5}\Rightarrow \quad IZ_1Z_3Z_5=VZ_2Z_4 \ \ldots\ldots\ldots\ldots 3.60$$

since $I=\frac{V}{Z_{in}}\Rightarrow\frac{V}{I}=Z_{in}$ ……..3.61

$$\therefore \ \frac{V}{I}=\frac{Z_1Z_3Z_5}{Z_2Z_4} \quad \ldots\ldots\ldots\ldots\ldots 3.62$$

3.8 Data conversion unit (U3):

This unit data conversion is divided into A/D converter and D/A converter section .A/D converter one input analog convert 8 bit output digital (LEDs) female parallel port. D/A converter 8bit input female parallel convert to analog valve shown as figure (3.25).



figure(3.24) : Data Conversion Unit

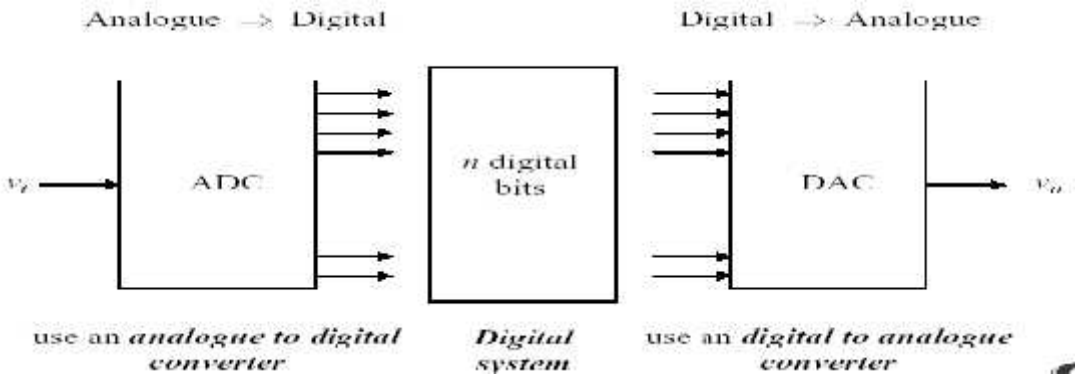
- **Signal converter:**

The microcomputer is a logic device it processes digital signal that are binary and discontinuous. On the other hand ,the real–word physical quantity such as temperature and pressure are continuous .

These are represented by equivalent electrical quantities called analog signal. Even through an analog signal may represent a real physical parameter with accuracy, it is difficult to process or store the analog signal for later use without introducing considerable error. Therefore, in microprocessor based industrial products, it is

necessary to translate an analog signal into a digital signal. The electronic circuit that translates an analog signal into a digital signal is called an analog to digital (A/Dc) converter (A/Dc).

Similarly a digital signal needs to be translated into analog signal to represent a physical quantity .this translator is called a digital to analog (D/A) converter. Both A/D and D/A are also known as data conversion.



figure(3.25): ADc toDAc process

3.8.1 Digital to analog converter (D\ Ac):

DAc are needed whenever the digitized signals through ADc are to be converted back to analog signal. Digital-to-Analog Converter – converts an digital signal (current-voltage) to digital value.

Most D/Ac uses a series of resistor in an R, 2R ,4R ,8R etc see the fig(1) each has double the previous resistor :

$$I_O = \frac{V_{REF}}{R}\left(\frac{A_1}{2} + \frac{A_2}{4} + ... + \frac{A_n}{2^n}\right) \quad \text{……..3.63}$$

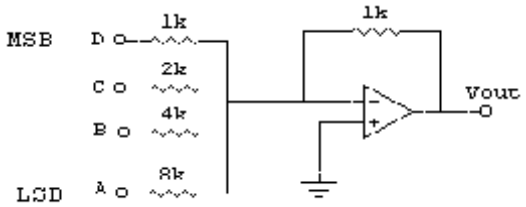


figure (3.26)) : D/Ac summing amplifier with binary weighted input resistors.

- **D/Ac characteristics:**

DAc has conversion speed as the successive approximation ADc.

3.8.2 Analog to digital signal A/Dc:

For the analog signals to be accepted by digital system or a microprocessor controller. The analog signals must be converted into digital signals. An A/Dc is used for:

1. Pc is a logic device (digital – discontinues).
2. The physical quantity as temperature, pressure is analog signal.
3. Digital signal reduction human error. Also it is easy to process or to store for later use.

(A\Dc) Analog-to-Digital Converter – converts an analog value to digital value (current-voltage).

- **A/Dc types**:

1. Successive approximation
2. Flash
3. Ramp
4. Integrating
5. Tracking
6. Delta sigma converter

- **How do we represent our' analogue' signal as a digital code?**

The number of signal levels depends upon the number of bits used e.g.:

4bit - 2^4 levels - 16 levels.

8bit- 2^8 levels - 256 levels.

16bit - 2^{16} levels – 65536 levels.

- **A/DC basic conversion methods:**

1. Direct conversion (voltage $\Rightarrow$ binary).

1.1 Counting converter (includes DAC).

1.2 Successive approximation (includes DAC).

1.3 Flash

2. Indirect conversion (voltage $\Rightarrow$ time $\Rightarrow$ binary)

Integrating ADC

(single slope and dual slope)

Chapter four

Testing

- **Unit testing:**
- **Sub-systems testing**
- **System testing .**

Testing :

The testing procedure is the most important part in the design of the hardware, to make sure that the hardware parts are working correctly and there are no errors.

The testing process includes the following stages:

- unit testing .
- Sub-systems testing.
- System testing .

Unit testing:

Here the testing is performed over the individual components are tested to ensure that they operate correctly.

All the electrical components, ICs are tested individually, were components noticed to function properly.

Sub-systems testing:

Here, the testing is performed over a collection of modules which have been integrated into sub-system.

The following sub-system were tested individually:

- 0804 A/Dc .
- 08cp D/Ac.
- Inverting amplifier.
- Noninverting amplifier .
- Instrumentation amplifier.
- Instrumentation rectifier.
- One poles and two poles low and high pass filter.
- Schmitt trigger.
- Negative impedance converter.
- Whetstone bridge .

0804 A/Dc testing:

Testing A/Dc 0804 is performed by choosing one input channel on specific voltage and display the digital value on the output ports.

08cp D/Ac testing:

Testing D/Ac 08cp is performed by choosing 8-bit valve and observes the output Voltages.

Inverting amplifier:

In testing this circuits ,we input voltage and observes the voltages output is inverted and the amplification of the input voltages according to calculation of the output voltages .

.

Non inverting amplifier:

In testing this circuits ,we input voltage and observes the amplification of the output voltages according to calculation of the output voltages .

.

Instrumentation amplifier:

In testing this circuits ,we input voltage and observes if amplified according to calculation of the output voltages .

Instrumentation rectifier:

to make sure that is working correctly we input sinusoidal voltage and observes half wave output to halfwave circiut rectifier and the fullwave to fullwave circuit rectifier .

One pole and two poles low and high pass filter:

Low pass filter we sure, if the input signal had frequency more than f_C Hz it was rejected, and if the input signal had a frequency less than f_C it was passed.

high pass filter we sure if the input signal had frequency less than f_C Hz it was rejected , and if the input signal had a frequency more than f_C it was passed.

Schmitt trigger:

In testing this circuit, we make sure that it worked correctly by comparing the input voltage with the reference voltage and making sure that the output is correct.

Whetstone Bridge:

Connect whetstone bridge with sensor turn on the power supply adjust the potentiometer to zero output voltage then stimulates the sensor see the change in voltage output of the bridge .

Negative impedance converter:

In testing this circuits , we observes the relation between the Z_{in} and theZ_{out}, when Z_{out} become $-Z_{in}$.

System testing:

After finishing the testing of sub-systems, the sub-systems are integrated to makeup a system . testing here is concerned with errors that generated from anticipated interaction between sub-system and system components .

The system testing itself is divided into the following stages:

1. Sensor unit test .
2. Operation amplifier unit test.
3. Data conversion unit test.

At first stage , sensor are connected to input resistance whetstone bridge, then stimulate sensor read output voltage of bridge .this testing was done .

Second stage , operation amplifier unit tested by connect input to of from output of sensor unit or function generator to oscilloscope and see the output. this testing is accomplished successfully .

Data conversion unit , take input voltage from sensor unit output or from operational amplifier unit first to input of A/Dc then to D/Ac .this testing was done successfully and achieved the desired results.

CHAPTER FIVE

Conclusion and Future work

Conclusion and future work

We have built the experimental board .And we have tested the board according to experiments sheet.

For future work we recommend to interface this board to the personal computer.

A. Book References:

1. George Clayton &Bruce Newby, (1992),"Operational Amplifiers ", (3rd ed.), Newnes

2. Albert Paul Malvino, (1999),"Electronic Principles", (6th ed.), Mc Graw-hill.

3. W.Bolten, (1996),"sensors and transducer"(3rd ed.).

4. Johan G.Webester, (1988),"medical Instromentaion"(3rd ed.), National Academy.

5. Johan J .Carr&Johan M.brown, (1993),"Introduction to Biomedical Equipment", (2nd ed.), Prentice Hall.

B. Internet Reference:

6. http://www.electronic.com/search,op+amp

PREFACE:

This manual is designed to help the user with the, insight of biomedical Electronics. It discusses implementation of various IC s for industrial utilities. By the end of the course user are expected to have understanding of the electronic devices and their usage.

Bioelectronics Lab Manual

Laboratory

Operational Amplifier

Name

PURPOSE:

1. Investigate the non-inverting amplifier .calculate and measure the voltage gain .
2. Investigate the inverting amplifier. .calculate and measure the voltage gain.
3. Determine characteristics of the circuit

EQUIPMENT:

1. Operation amplifier U2.
2. Function generator**.**
3. Oscilloscope.
4. DVM.

A. Non-inverting Amplifier

1. Preliminary design work

before you come to lab ,design and sketch a noninverting amplifier

Build and test this circuit:

. 1. connect the circuits as the figure

2. Apply a small amplitude sine wave from signal generator , and verify the operation of this circuit..

3. Use a DMM to measure R_1 , R_2 and calculate the gain.

R_1 = Ω

R_2 = Ω

gain= $1+\frac{R_2}{R_1}$.

4. mesure the input voltage and the output voltage , calculate the gain .

V_{in} = v

V_{out} = v

$$gain = \frac{V_{out}}{V_{in}}$$

B. inverting Amplifier

1. Preliminary design work

before you come to lab ,design and sketch a inverting amplifier

Build and test this circuit:

1. connect the circuits as the figurer

2. Apply a small amplitude sine wave from signal generator , and verify the operation of this circuit..

3. Use a DMM to measure R_1, R_2 and calculate the gain.

R_1 = Ω
R_2 = Ω

gain= $-\frac{R_2}{R_1}$ = .

4. mesure the input voltage and the output voltage , calculate the gain .

V_{in} = v

V_{out} = v

$gain = -\frac{V_{out}}{V_{in}} =$

Bioelectronics Lab Manual

Laboratory **SCHIMIT TRIGER**

Name

PURPOSE:

1. Sketch the comparator circuit that has positive feedback.
2. Obtain the output of the with square wave.
3. Determine characteristics of the circuit

EQUIPMENT:

1. operation amplifier U2.
2. Function generator**.**
3. oscilloscope.
4. DVM.

Build and test this circuit:

1. connect the circuits as the figure.

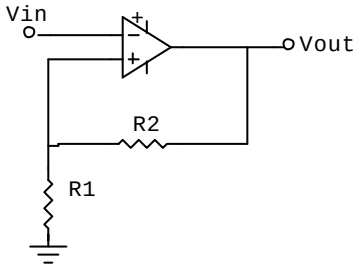


Figure: Schmitt trigger

2. Connect the triangle wave voltage from signal generator.

3. Calculate the voltage feedback:

$$V_{fb} = \pm \frac{R_1}{R_1 + R_2} V_{sat}$$

4. Slowing increase input voltage and note the output.

rectifier

Name

PURPOSE:

to understand operation of the circuits and determine characteristics of the circuits

EQUIPMENT:

1. Operation amplifier U2.
2. Function generator**.**
3. Oscilloscope.
4. DVM.

A. Half wave rectifier

Build and test this circuit:

1. connect the circuits as in the figure.

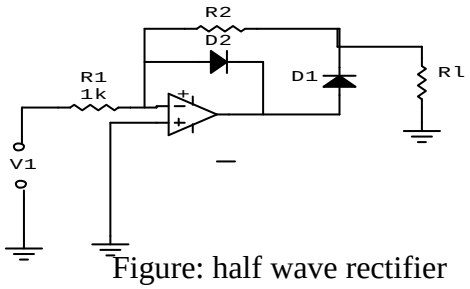


Figure: half wave rectifier

2. connect sin wave voltage from signal generator

3. draw the output voltage

A. full wave rectifier

Build and test this circuit:

1. Connect the circuits as in the figure

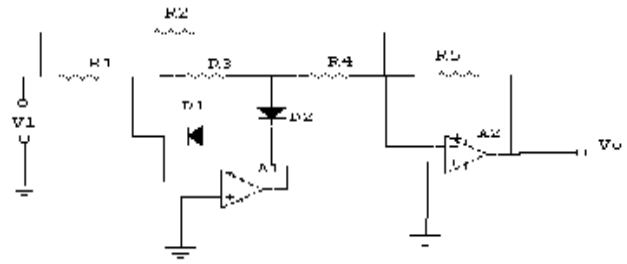


Figure: full wave rectifier

2. Connect sin wave voltage from signal generator

3. Draw the output voltage

Bioelectronics Lab Manual

Laboratory **Instrumentation amplifier**

Name

PURPOSE:

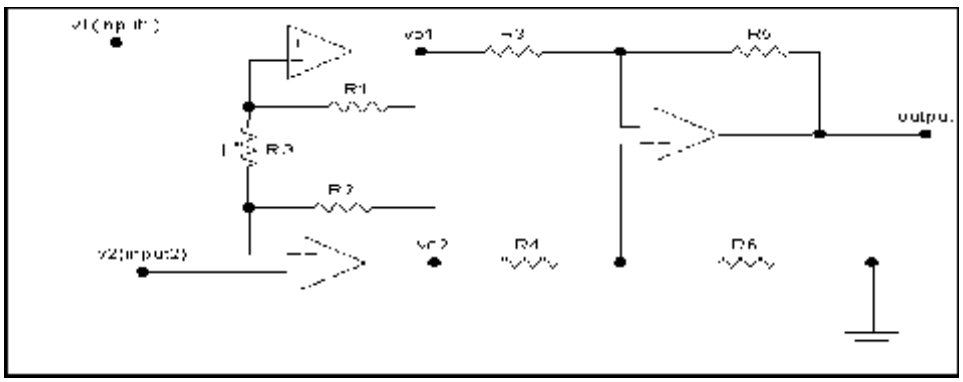
1. determine the output of instrumentation amplifier
2.determine characteristics of the circuit

EQUIPMENT:

1. Operation amplifier U2.
2.Function generator**.**
3.Oscilloscope.
4.DVM.

Build and test this circuit:

1. connect the circuits as in the figure



Figure(3.6): Instrumentation Amplifier

2. connect input signal to V1,V2
3. measure R_1, R_3, R_5, R_G

R_1 =

R_3 =

R_5 =

R_G =

$$A_V = \left(\frac{2R_1}{R_G} + 1\right)\left(\frac{R_5}{R_3}\right) =$$

4. draw the out put voltage

Bioelectronics Lab Manual

Laboratory

Negative Impedance Converter

Name

PURPOSE:

1. To know principle of operation and characteristics of circuit .

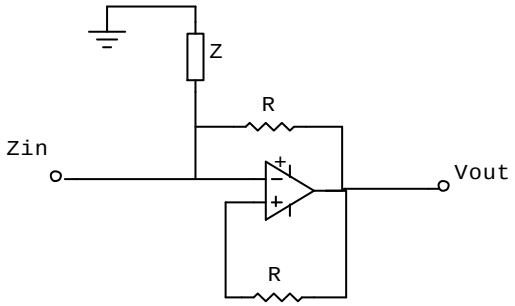
2.To find output impedance.

EQUIPMENT:

1. Operation amplifier U2.
2. Function generator**.**
3. Oscilloscope.
4. DVM.

Build and test this circuit:

1. connect the circuits as in the figure.



2. measure C , connect V_{in} and obsearve.

$Z_{in} = -Z$

$V_{in} =$

4. draw the output voltage

$V_{out} =$

Bioelectronics Lab Manual

Laboratory **Filters**

Name

PURPOSE:

1. Know principle of operation the circuits
2. Determine Characteristics of first and second order low pass filter.
3. Determine Characteristics of first and second order high pass filter.
4. Determine the frequency response of low and high pass filter.

EQUIPMENT:

1. Operation amplifier U2.
2. Function generator**.**
3. oscilloscope.
4. DVM.

A. low pass filter

1. First order

Build and test this circuit:

1. connect the circuits as in the figure

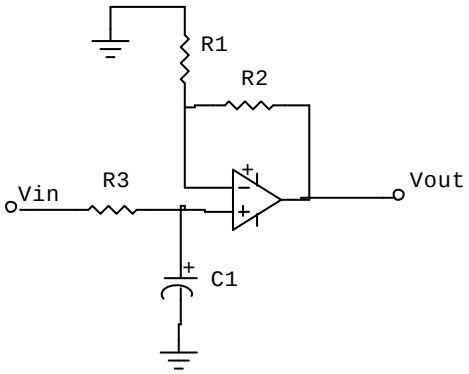


figure: first order low pass filter

2. Adjust the signal generator to sinusoidal waveform
3. Vary the frequency and observe V_{out}
4. Calculate the voltage gain of the circuit

$$Av = \frac{R_2}{R_1} + 1 \quad =$$

5. Sketch the frequency response the circuit

2. Second order

Build and test this circuit:

2. connect the circuits as in the figure

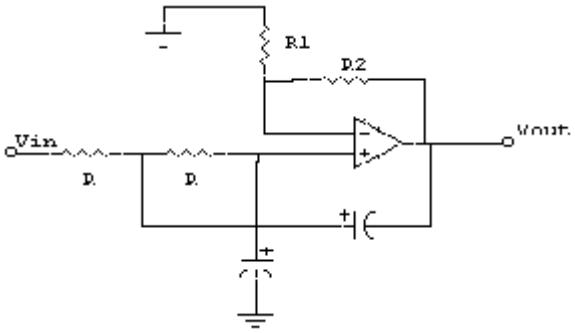


Figure: second order low pass filter

2. Adjust the signal generator to sinusoidal waveform
3. Vary the frequency and observe V_{out}
4. Calculate the voltage gain of the circuit

$$Av = \frac{R_2}{R_1} + 1 \quad =$$

5. Sketch the frequency response the circuit

B. high pass filter:

1.first order

Build and test this circuit:

3. connect the circuits as in the figure

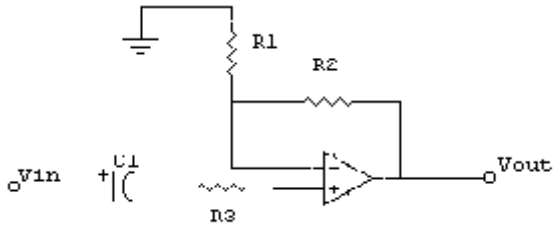


Figure: first order high pass filter

.

2. Adjust the signal generator to sinusoidal waveform

3. Vary the frequency and observe V_{out}

4. Calculate the voltage gain of the circuit

$$Av = \frac{R_2}{R_1} + 1 \quad =$$

5. Sketch the frequency response the circuit

2. second order

Build and test this circuit:

4. connect the circuits as in the figure

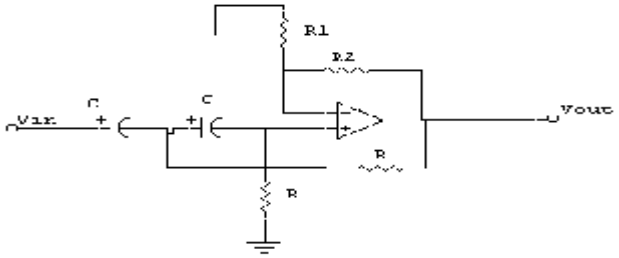


Figure: Second order high pass filter

2. Adjust the signal generator to sinusoidal waveform

3. Vary the frequency and observe V_{out}

4. Calculate the voltage gain of the circuit

$$Av = \frac{R_2}{R_1} + 1 \quad =$$

5. Sketch the frequency response the circuit

Bioelectronics Lab Manual

Laboratory **Data conversions**

Name

PURPOSE:

To learn ADc and DAc technique of the temperature data using Wheatstone Bridge .

EQUIPMENT:

1. Data conversion unit U2.
2. Temperature sensor.
3. DVM.
4. Sensor unit U1.

Build and test this circuit:

1. Connect the temperature sensors to the sensor input terminals of the sensor unit.
2. Adjusting the potentiometer of the set the bridge to balance so the current indication is zero.
3. Connect between the bridge out put of and input of ADc and the DVM .
4. Increase the temperature of the sensors and measure the analog and digital output and fill the table with the results.

	Analog	Digital (8 bit)							
	volts	D7	D6	D5	D4	D3	D2	D1	D0
1									

2									
3									
4									
5									

Table: ADc

5.repeat step 6 but connect ADc out put to DAc input and compare the values

Digital (8 bit)								Analog	
D7	D6	D5	D4	D3	D2	D1	D0	volts	
									1
									2
									3
									4
									5

Table :DAc

- **Low Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Total Harmonic Distortion . . . 0.003% Typ**
- **High Input Impedance . . . JFET-Input Stage**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 13 V/μs Typ**
- **Common-Mode Input Voltage Range Includes V_{CC+}**

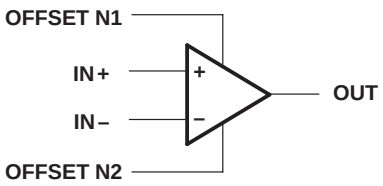
description

The TL08x JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08x family.

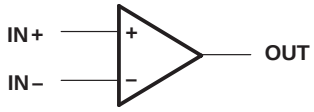
The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The Q-suffix devices are characterized for operation from –40°C to 125°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

symbols

TL081

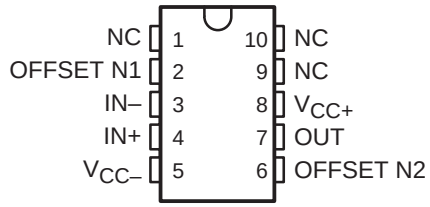


TL082 (EACH AMPLIFIER)
TL084 (EACH AMPLIFIER)

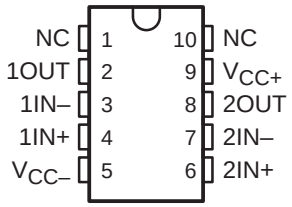


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

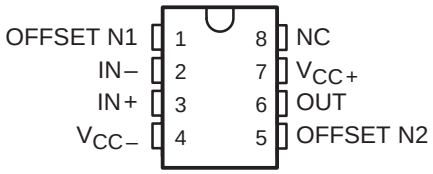
TL081M
U PACKAGE
(TOP VIEW)



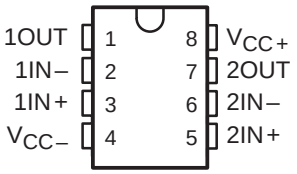
TL082M
U PACKAGE
(TOP VIEW)



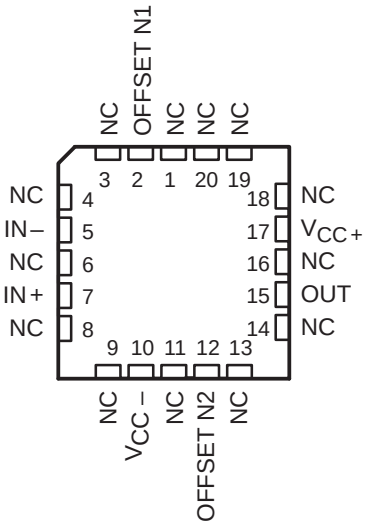
TL081, TL081A, TL081B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



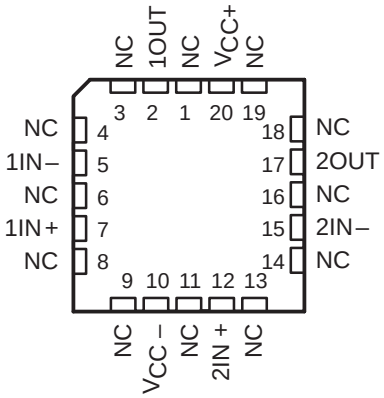
TL082, TL082A, TL082B
D, JG, P, OR PW PACKAGE
(TOP VIEW)



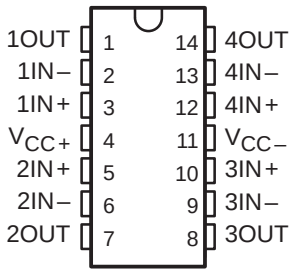
TL081M . . . FK PACKAGE
(TOP VIEW)



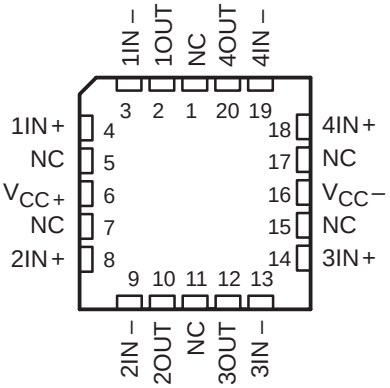
TL082M . . . FK PACKAGE
(TOP VIEW)



TL084, TL084A, TL084B
D, J, N, PW, OR W PACKAGE
(TOP VIEW)



TL084M . . . FK PACKAGE
(TOP VIEW)



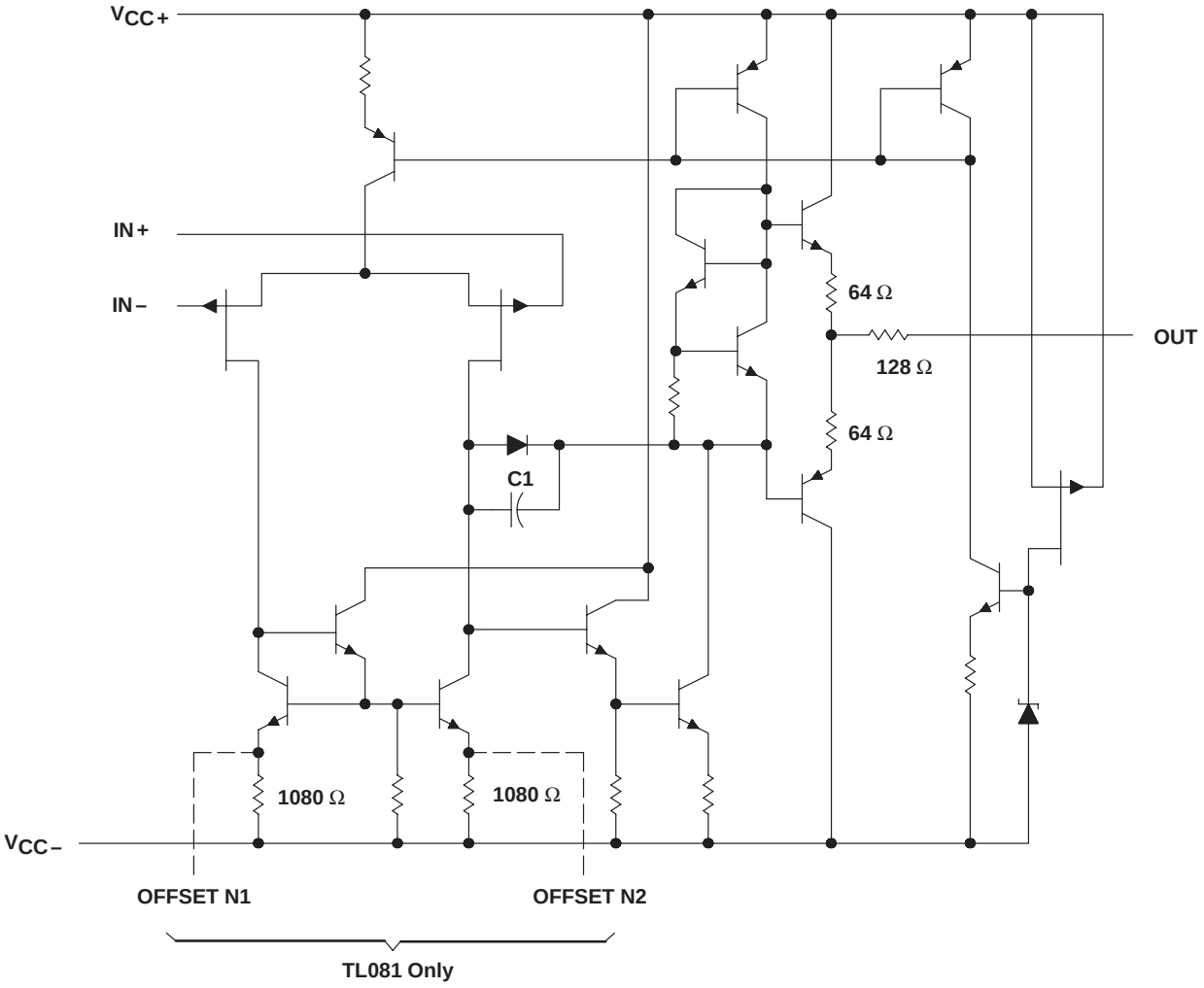
NC – No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES										CHIP FORM (Y)
		SMALL OUTLINE (D008)	SMALL OUTLINE (D014)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)	TSSOP (PW)	FLAT PACK (U)	FLAT PACK (W)	
0°C to 70°C	15 mV 6 mV 3 mV	TL081CD TL081ACD TL081BCD	—	—	—	—	—	TL081CP TL081ACP TL081BCP	TL081CPW	—	—	—
	15 mV 6 mV 3 mV	TL082CD TL082ACD TL082BCD	—	—	—	—	—	TL082CP TL082ACP TL082BCP	TL082CPW	—	—	TL082Y
	15 mV 6 mV 3 mV	—	TL084CD TL084ACD TL084BCD	—	—	—	TL084CN TL084ACN TL084BCN	—	TL084CPW	—	—	TL084Y
–40°C to 85°C	6 mV 6 mV 6 mV	TL081ID TL082ID TL084ID	TL084ID	—	—	—	TL084IN	TL081IP TL082IP	—	—	—	—
–40°C to 125°C	9 mV	—	TL084QD	—	—	—	—	—	—	—	—	—
–55°C to 125°C	6 mV 6 mV 9 mV	—	—	TL081MFK TL082MFK TL084MFK	TL084MJ	TL081MJG TL082MJG	—	—	—	TL081MU TL082MU	TL084MW	—

The D package is available taped and reeled. Add R suffix to the device type (e.g., TL081CDR).

schematic (each amplifier)

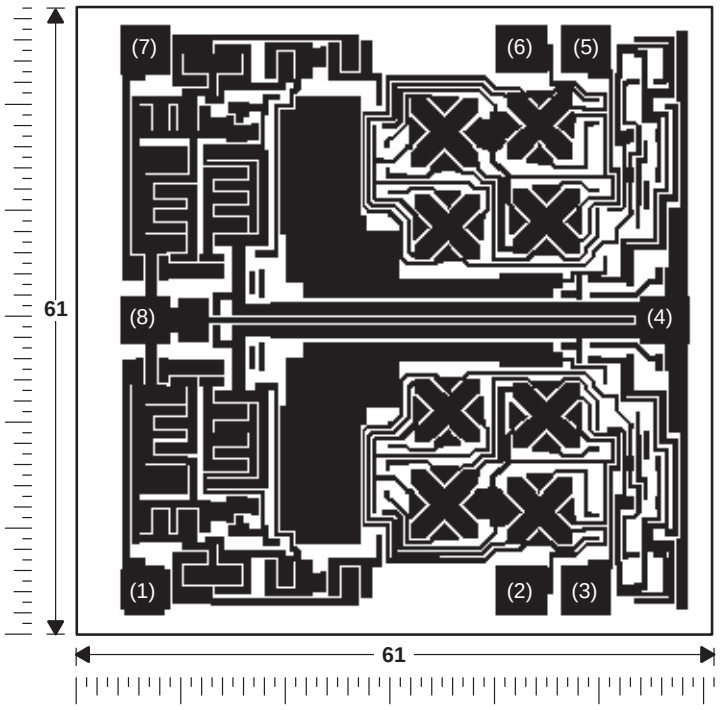


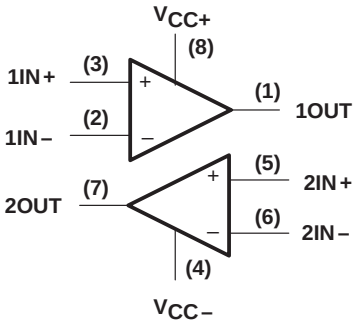
Component values shown are nominal.

TL082Y chip information

These chips, when properly assembled, display characteristics similar to the TL082. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

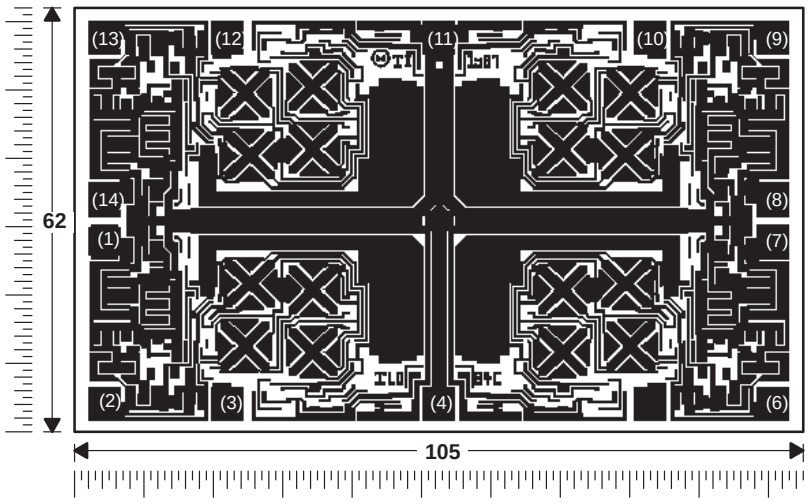
ALL DIMENSIONS ARE IN MILS.

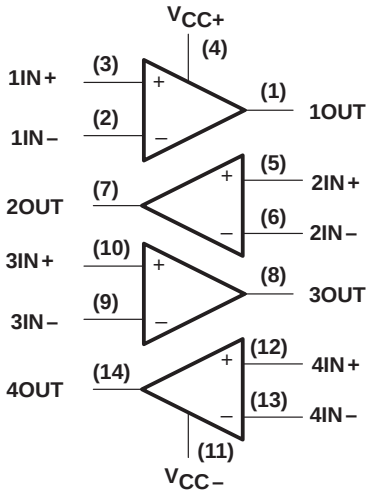
PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

TL084Y chip information

These chips, when properly assembled, display characteristics similar to the TL084. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

		TL08_C TL08_AC TL08_BC	TL08_I	TL084Q	TL08_M	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	18	V
Supply voltage V_{CC-} (see Note 1)		–18	–18	–18	–18	V
Differential input voltage, V_{ID} (see Note 2)		±30	±30	±30	±30	V
Input voltage, V_I (see Notes 1 and 3)		±15	±15	±15	±15	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	unlimited	
Continuous total power dissipation		See Dissipation Rating Table				
Operating free-air temperature range, T_A		0 to 70	– 40 to 85	– 40 to 125	– 55 to 125	°C
Storage temperature range, T_{stg}		– 65 to 150	– 65 to 150	– 65 to 150	– 65 to 150	°C
Case temperature for 60 seconds, T_C	FK package				260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or JG package				300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N, P, or PW package	260	260	260		°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8 pin)	680 mW	5.8 mW/°C	32°C	460 mW	373 mW	N/A
D (14 pin)	680 mW	7.6 mW/°C	60°C	604 mW	490 mW	186 mW
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
J	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
N	680 mW	9.2 mW/°C	76°C	680 mW	597 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A
PW (8 pin)	525 mW	4.2 mW/°C	25°C	336 mW	N/A	N/A
PW (14 pin)	700 mW	5.6 mW/°C	25°C	448 mW	N/A	N/A
U	675 mW	5.4 mW/°C	25°C	432 mW	351 mW	135 mW
W	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	200 mW

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TL081C TL082C TL084C			TL081AC TL082AC TL084AC			TLO81BC TL082BC TL084BC			TL081I TL082I TL084I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	15		3	6		2	3		3	6	mV
			Full range			20			7.5			5			9	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18			18			18		µV/°C
I_{IO}	Input offset current‡	V_O = 0	25°C		5	200		5	100		5	100		5	100	pA
			Full range			2			2			2			10	nA
I_{IB}	Input bias current‡	V_O = 0	25°C		30	400		30	200		30	200		30	200	pA
			Full range			10			7			7			20	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			±12			±12			
		R_L ≥ 2 kΩ		±10	±12		±10	±12		±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	25	200		50	200		50	200		50	200		V/mV
		V_O = ±10 V, R_L ≥ 2 kΩ	Full range	15			25			25			25			
B_1	Unity-gain bandwidth		25°C		3			3			3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	70	86		75	86		75	86		75	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ± 9 V, V_O = 0, R_S = 50 Ω	25°C	70	86		80	86		80	86		80	86		dB
I_{CC}	Supply current (per amplifier)	V_O = 0, No load	25°C		1.4	2.8		1.4	2.8		1.4	2.8		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120			120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is 0°C to 70°C for TL08_C, TL08_AC, TL08_BC and −40°C to 85°C for TL08_I.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 17. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	T_A	TL081M, TL082M			TL084Q, TL084M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	6		3	9	mV
			Full range			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0 R_S = 50 Ω	Full range		18			18		μV/°C
I_{IO}	Input offset current‡	V_O = 0	25°C		5	100		5	100	pA
			125°C			20			20	nA
I_{IB}	Input bias current‡	V_O = 0	25°C		30	200		30	200	pA
			125°C			50			50	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	±12 to 15		±11	±12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L ≥ 2 kΩ		±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	25	200		25	200		V/mV
		V_O = ±10 V, R_L ≥ 2 kΩ	Full range	15			15			
B_1	Unity-gain bandwidth		25°C		3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
I_{CC}	Supply current (per amplifier)	V_O = 0, No load	25°C		1.4	2.8		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.
‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 17. Pulse techniques must be used that maintain the junction temperatures as close to the ambient temperature as is possible.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V,	R_L = 2 kΩ,	C_L = 100 pF,	See Figure 1	8*	13		V/μs
		V_I = 10 V, T_A = – 55°C to 125°C,	R_L = 2 kΩ, See Figure 1	C_L = 100 pF,		5*			
t_r	Rise time	V_I = 20 mV,	R_L = 2 kΩ,	C_L = 100 pF,	See Figure 1		0.05		μs
	Overshoot factor						20%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz				18		nV/√Hz
			f = 10 Hz to 10 kHz				4		μV
I_n	Equivalent input noise current	R_S = 20 Ω,	f = 1 kHz				0.01		pA/√Hz
THD	Total harmonic distortion	$V_I$rms = 6 V, f = 1 kHz	A_{VD} = 1,	R_S ≤ 1 kΩ,	R_L ≥ 2 kΩ,		0.003%		

*On products compliant to MIL-PRF-38535, this parameter is not production tested.

electrical characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL082Y, TL084Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0,	R_S = 50 Ω		3	15	mV
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0,	R_S = 50 Ω		18		μV/°C
I_{IO}	Input offset current‡	V_O = 0,			5	200	pA
I_{IB}	Input bias current‡	V_O = 0,			30	400	pA
V_{ICR}	Common-mode input voltage range			±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ,		±12	±13.5		V
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,	$R_L \geq$ 2 kΩ	25	200		V/mV
B_1	Unity-gain bandwidth				3		MHz
r_i	Input resistance				10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, R_S = 50 Ω	V_O = 0,	70 70	86 86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ± 9 V, V_O = 0,	R_S = 50 Ω	70 70	86 86		dB
I_{CC}	Supply current (per amplifier)	V_O = 0,	No load		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.
‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 17. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V,	R_L = 2 kΩ,	C_L = 100 pF,	See Figure 1	8	13		V/μs
t_r	Rise time	V_I = 20 mV,	R_L = 2 kΩ,	C_L = 100 pF,	See Figure 1		0.05		μs
	Overshoot factor						20%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz				18		nV/√Hz
			f = 10 Hz to 10 kHz				4		μV
I_n	Equivalent input noise current	R_S = 20 Ω,	f = 1 kHz				0.01		pA/√Hz
THD	Total harmonic distortion	$V_I$rms = 6 V, f = 1 kHz	A_{VD} = 1,	$R_S \leq$ 1 kΩ,	$R_L \geq$ 2 kΩ,		0.003%		

PARAMETER MEASUREMENT INFORMATION

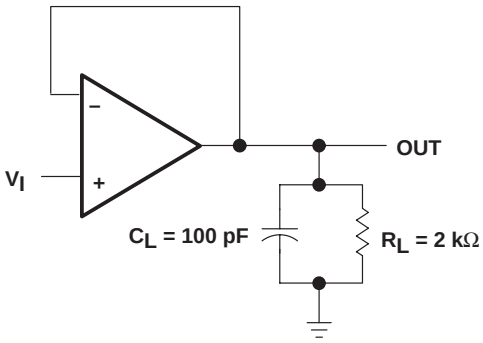


Figure 1

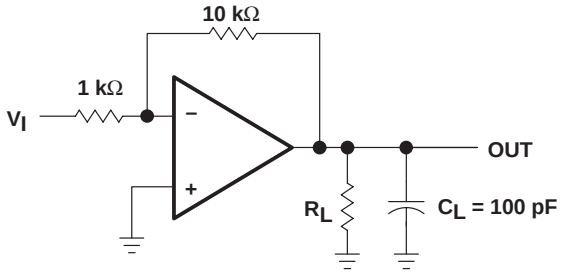


Figure 2

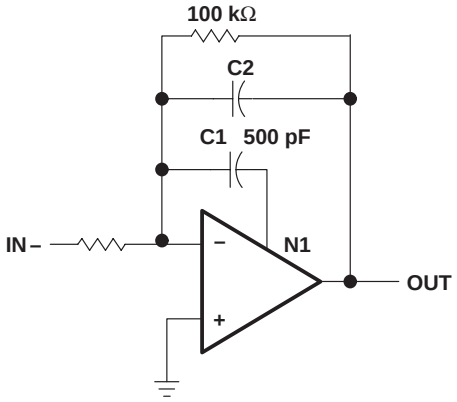


Figure 3

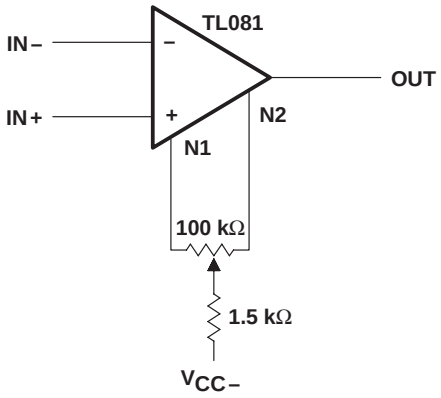


Figure 4

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{OM}	Maximum peak output voltage	vs Frequency vs Free-air temperature vs Load resistance vs Supply voltage	5, 6, 7 8 9 10
A_{VD}	Large-signal differential voltage amplification	vs Free-air temperature vs Frequency	11 12
	Differential voltage amplification	vs Frequency with feed-forward compensation	13
P_D	Total power dissipation	vs Free-air temperature	14
I_{CC}	Supply current	vs Free-air temperature vs Supply voltage	15 16
I_{IB}	Input bias current	vs Free-air temperature	17
	Large-signal pulse response	vs Time	18
V_O	Output voltage	vs Elapsed time	19
CMRR	Common-mode rejection ratio	vs Free-air temperature	20
V_n	Equivalent input noise voltage	vs Frequency	21
THD	Total harmonic distortion	vs Frequency	22

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

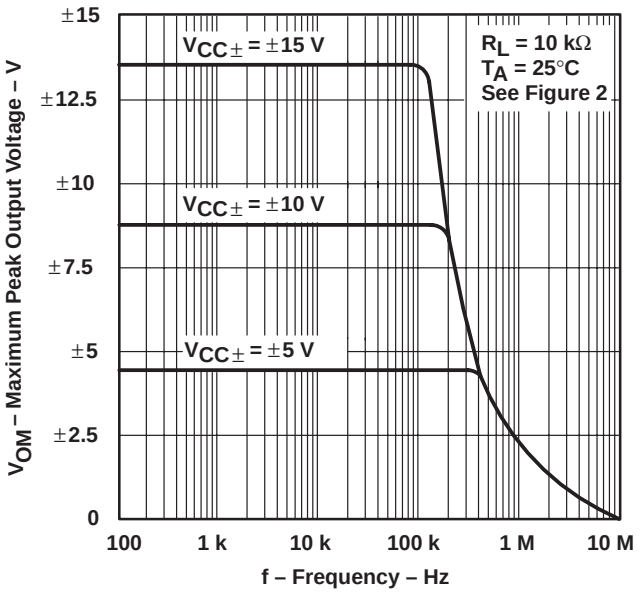


Figure 5

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

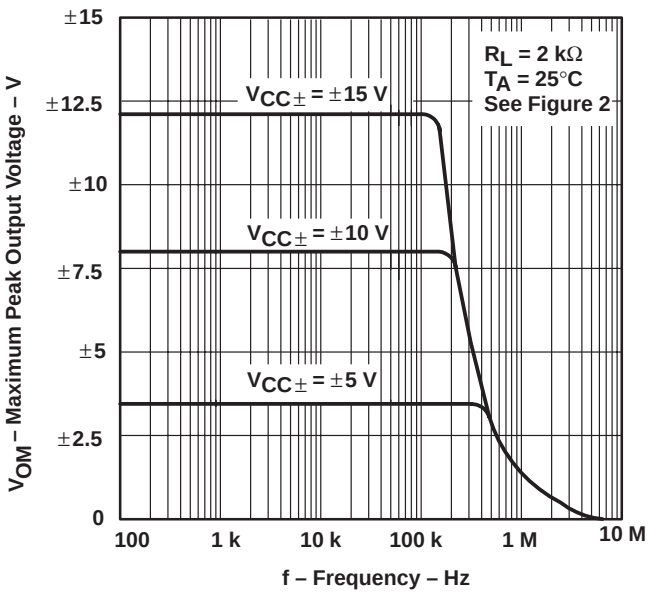


Figure 6

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

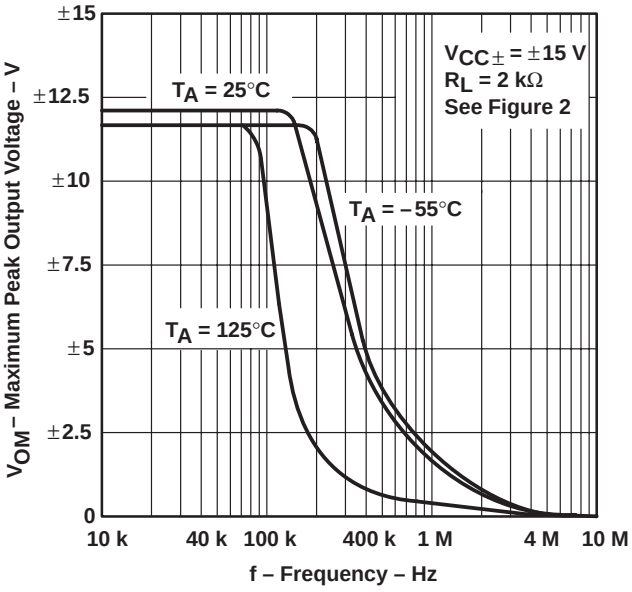


Figure 7

MAXIMUM PEAK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

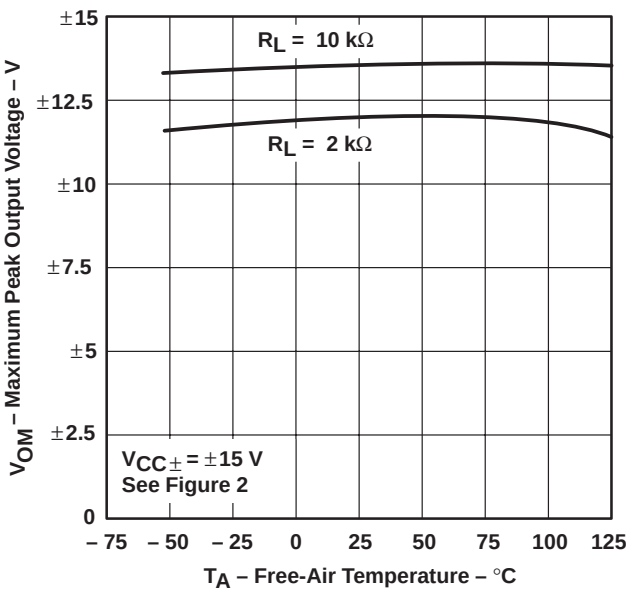


Figure 8

MAXIMUM PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

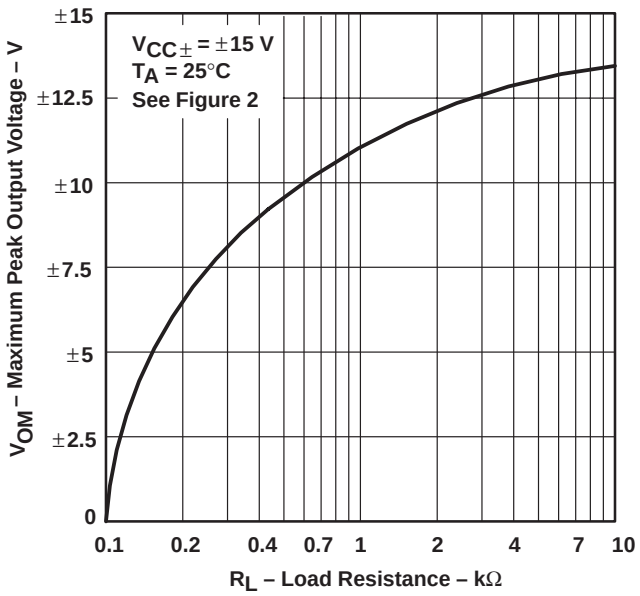


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE vs SUPPLY VOLTAGE

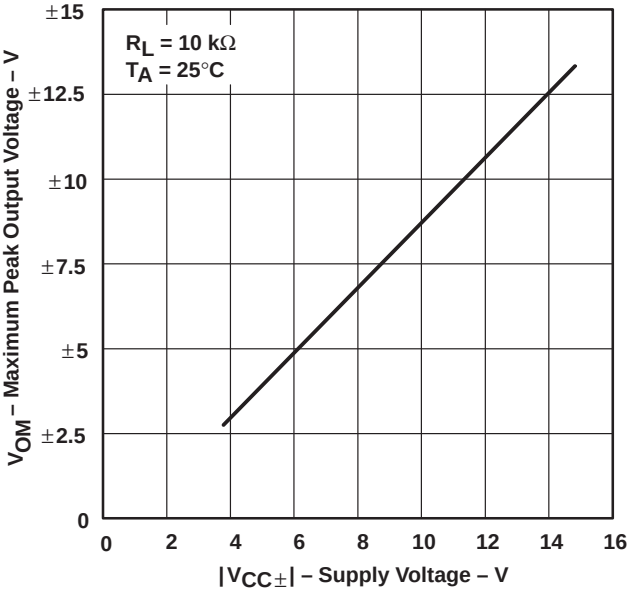


Figure 10

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

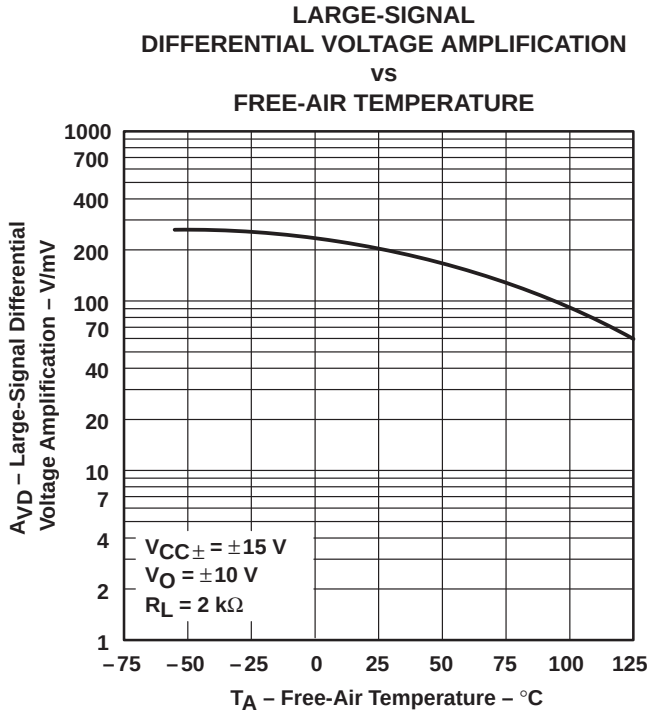


Figure 11

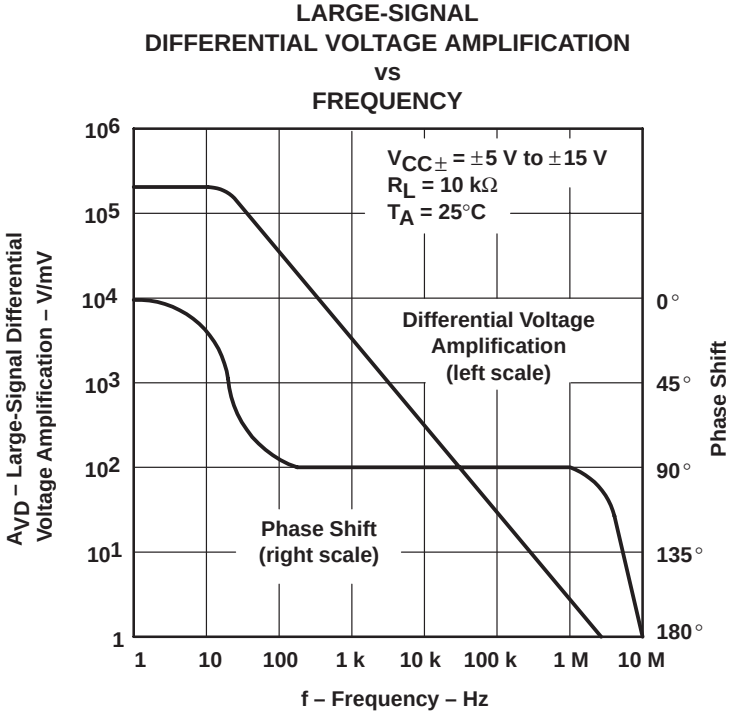


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY WITH FEED-FORWARD COMPENSATION

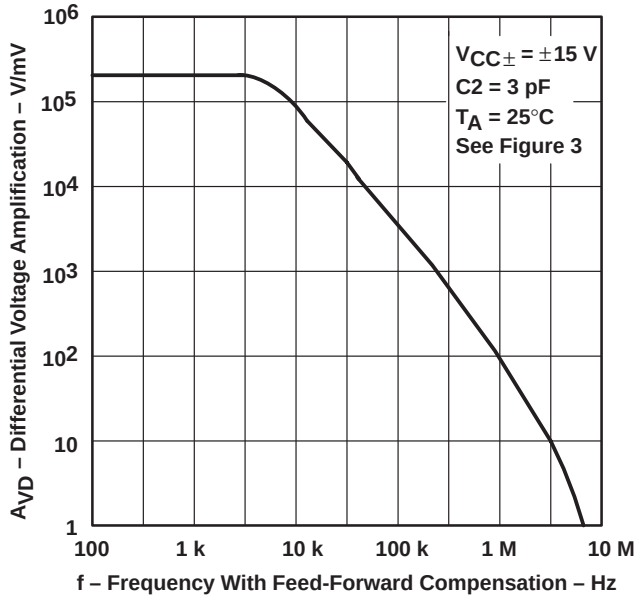


Figure 13

TOTAL POWER DISSIPATION vs FREE-AIR TEMPERATURE

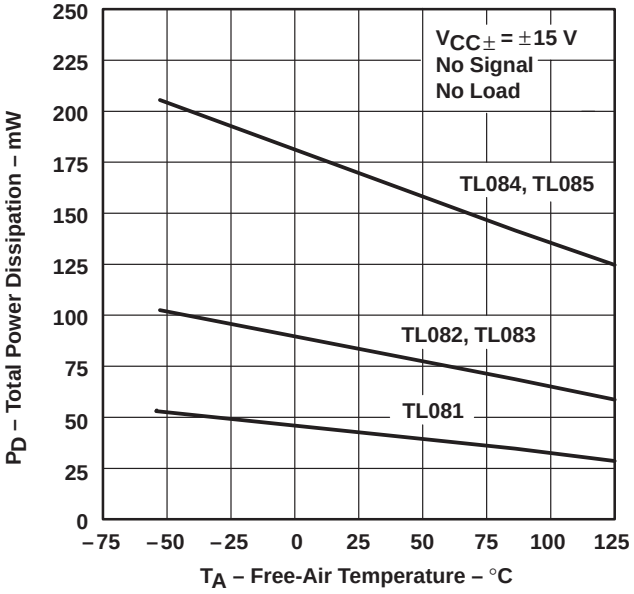


Figure 14

SUPPLY CURRENT PER AMPLIFIER vs FREE-AIR TEMPERATURE

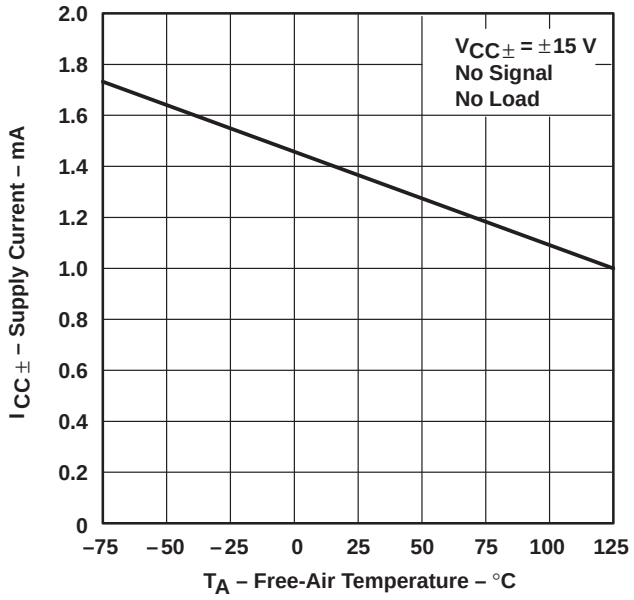


Figure 15

SUPPLY CURRENT vs SUPPLY VOLTAGE

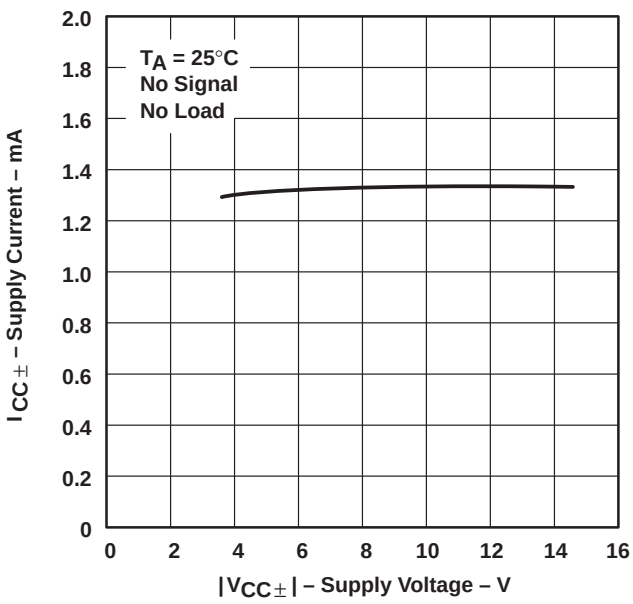


Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

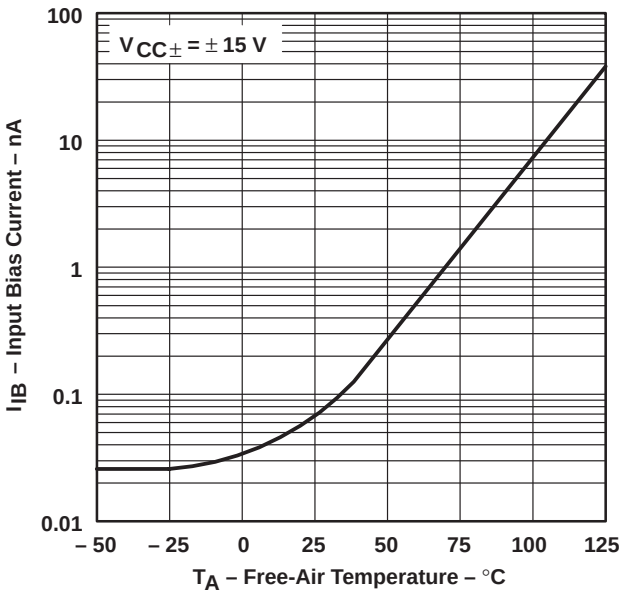


Figure 17

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

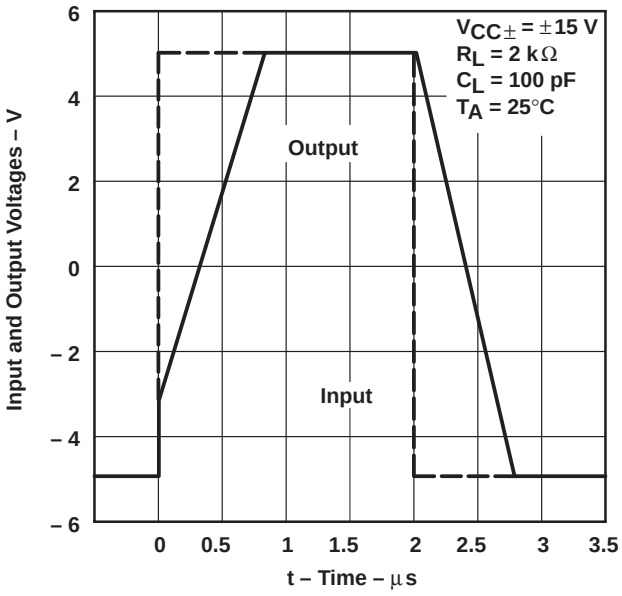


Figure 18

OUTPUT VOLTAGE vs ELAPSED TIME

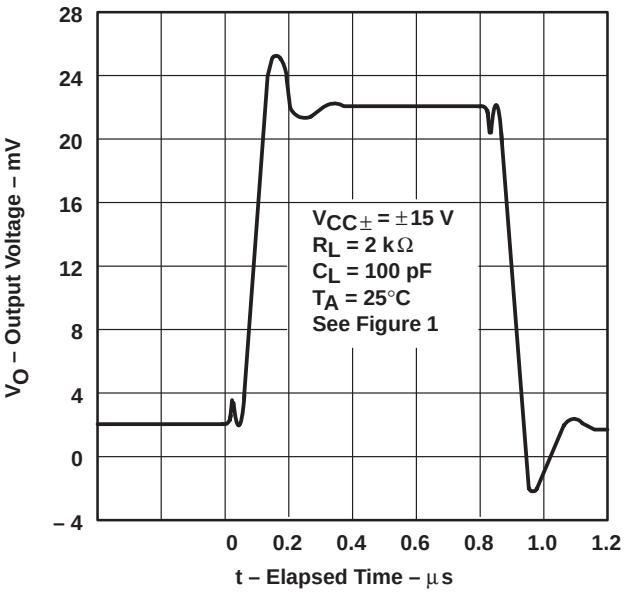


Figure 19

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

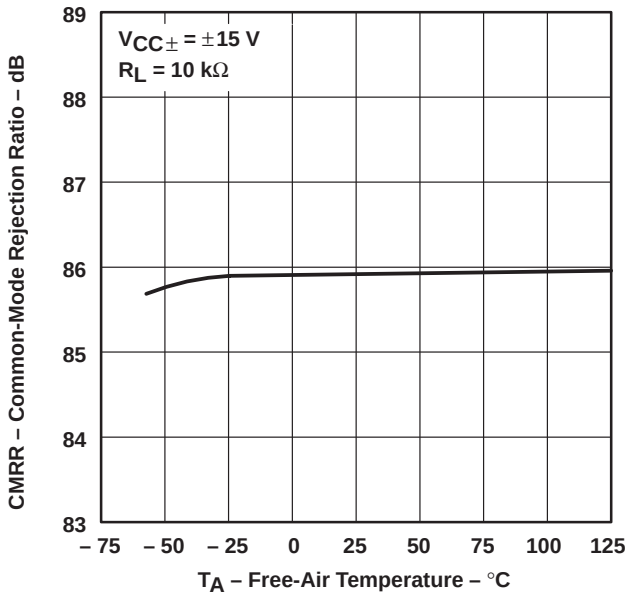


Figure 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

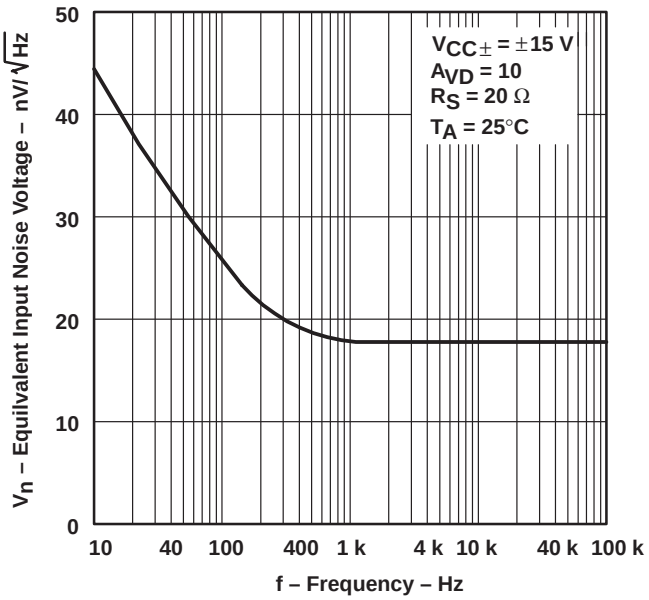


Figure 21

TOTAL HARMONIC DISTORTION vs FREQUENCY

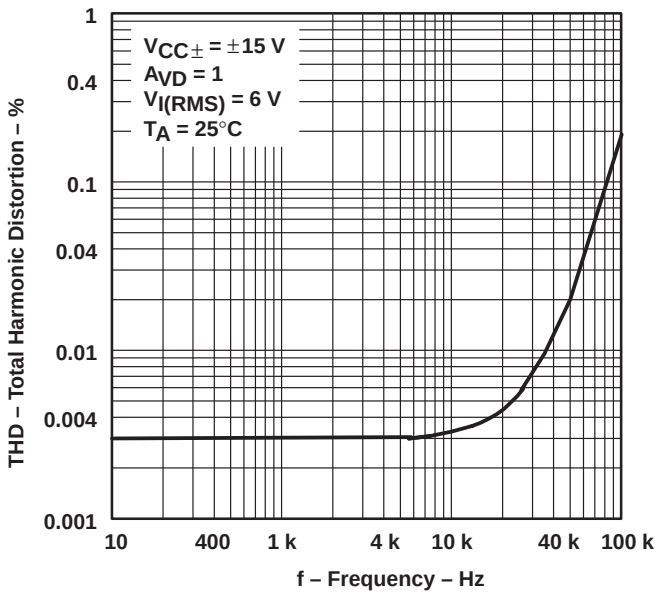


Figure 22

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

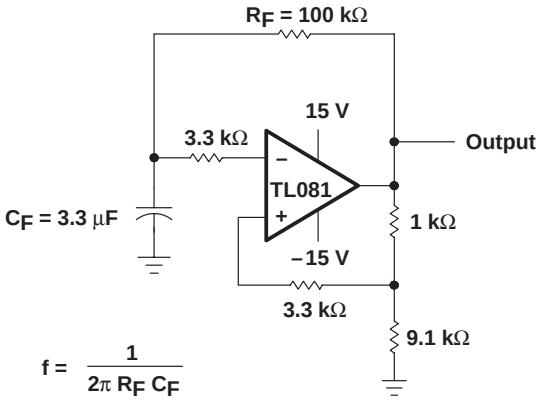


Figure 23

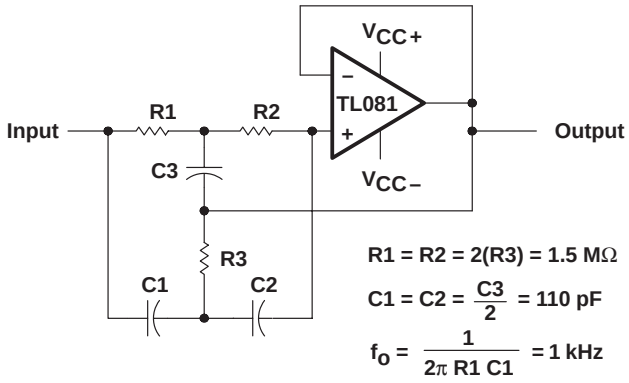


Figure 24

APPLICATION INFORMATION

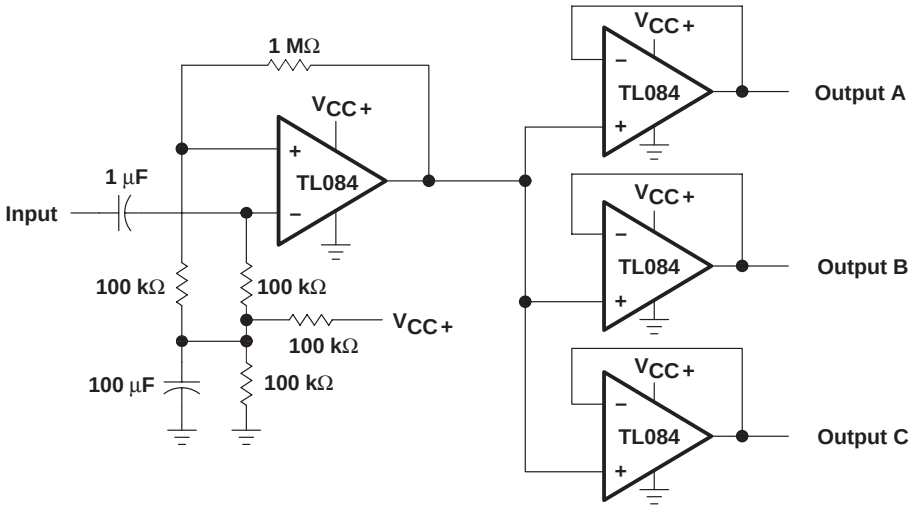
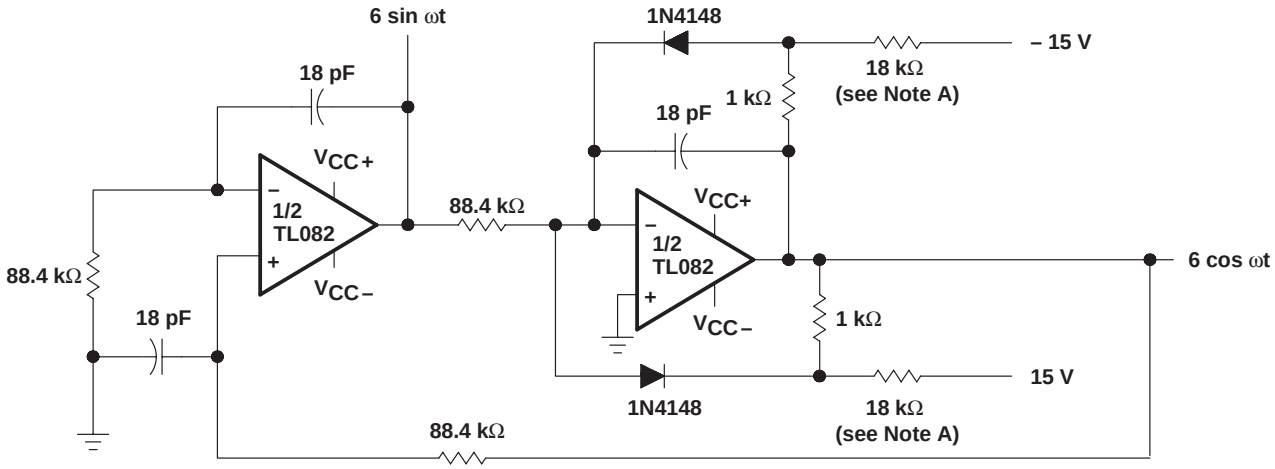


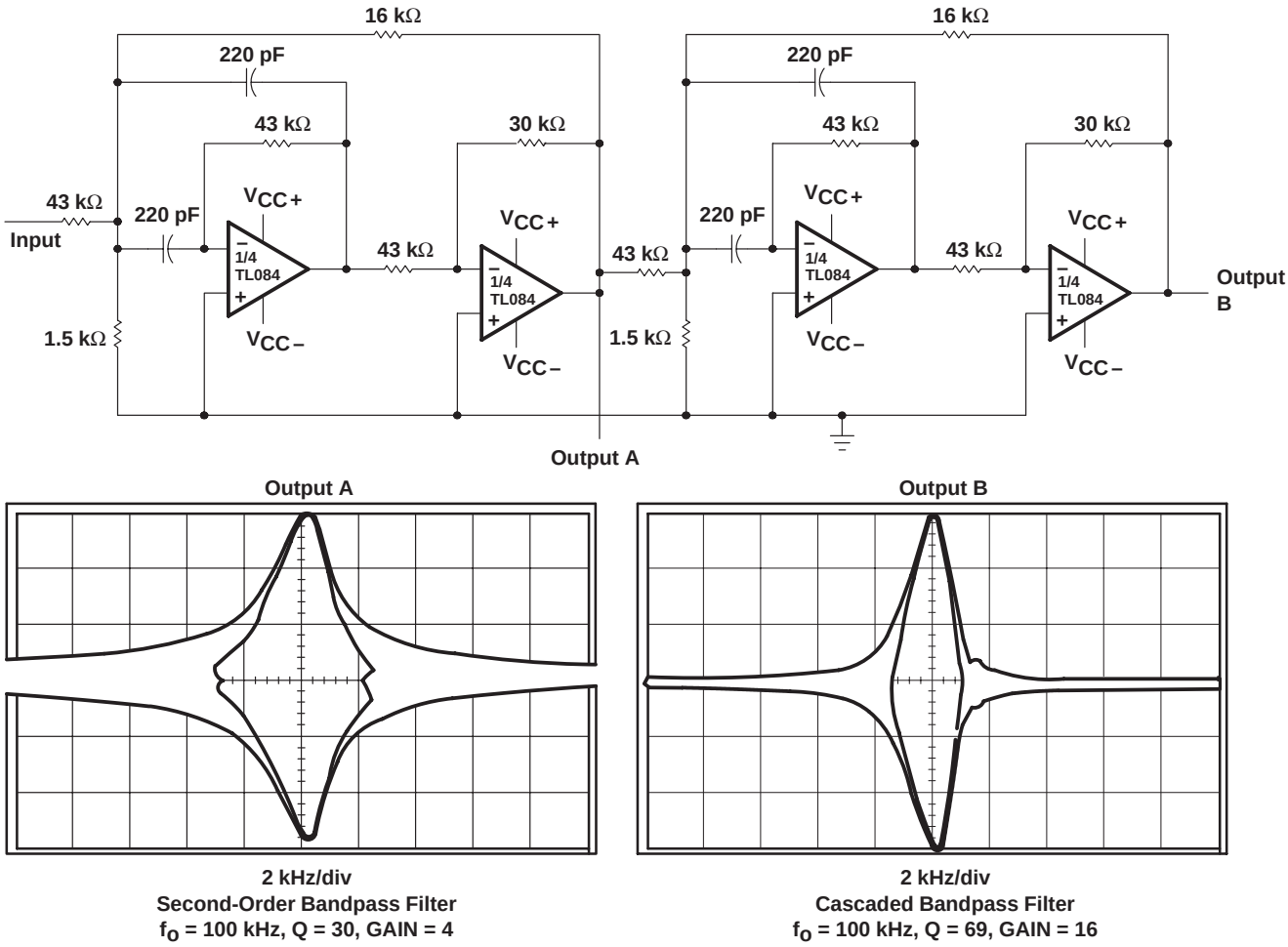
Figure 25. Audio-Distribution Amplifier



NOTE A: These resistor values may be adjusted for a symmetrical output.

Figure 26. 100-KHz Quadrature Oscillator

APPLICATION INFORMATION



Output A

2 kHz/div
Second-Order Bandpass Filter
f_O = 100 kHz, Q = 30, GAIN = 4

Output B

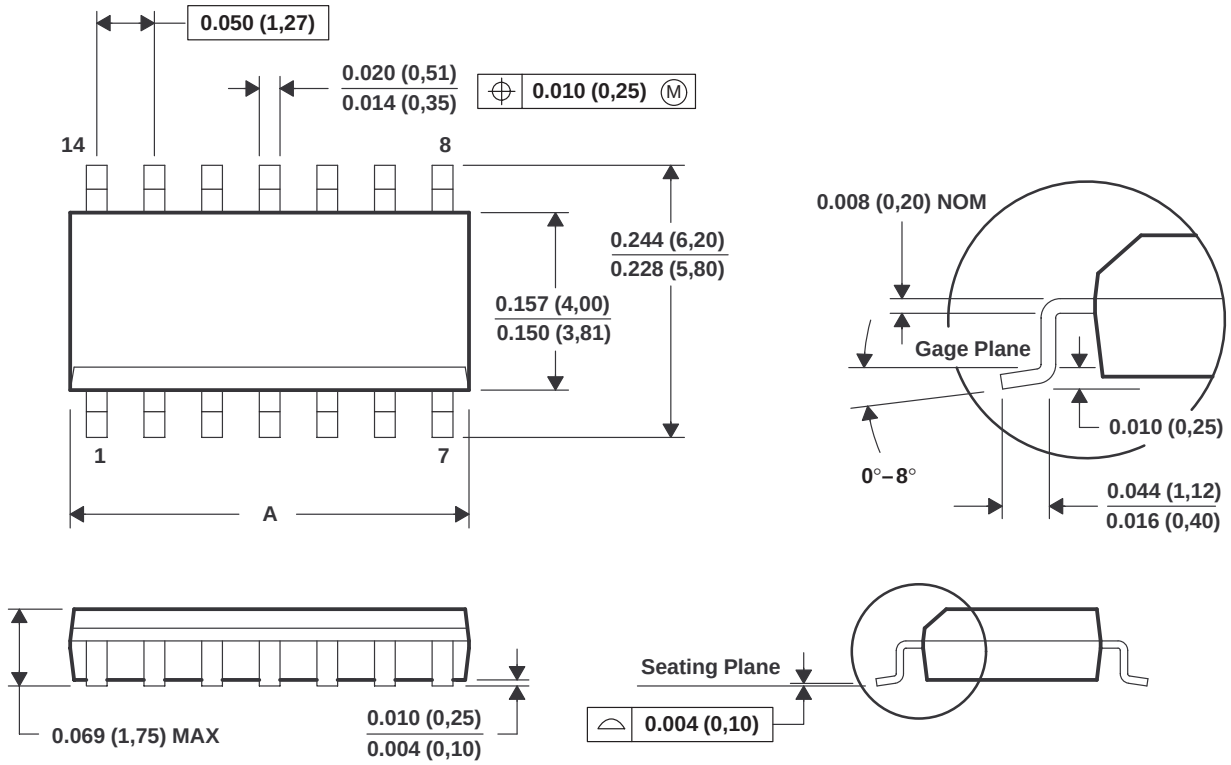
2 kHz/div
Cascaded Bandpass Filter
f_O = 100 kHz, Q = 69, GAIN = 16

Figure 27. Positive-Feedback Bandpass Filter

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

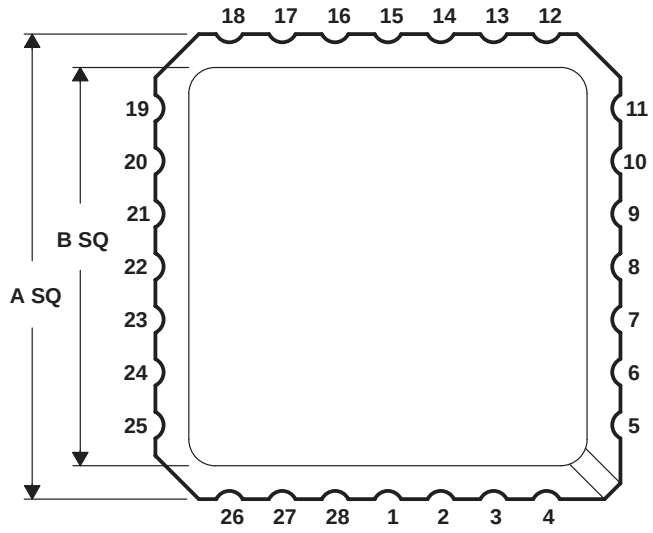
4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

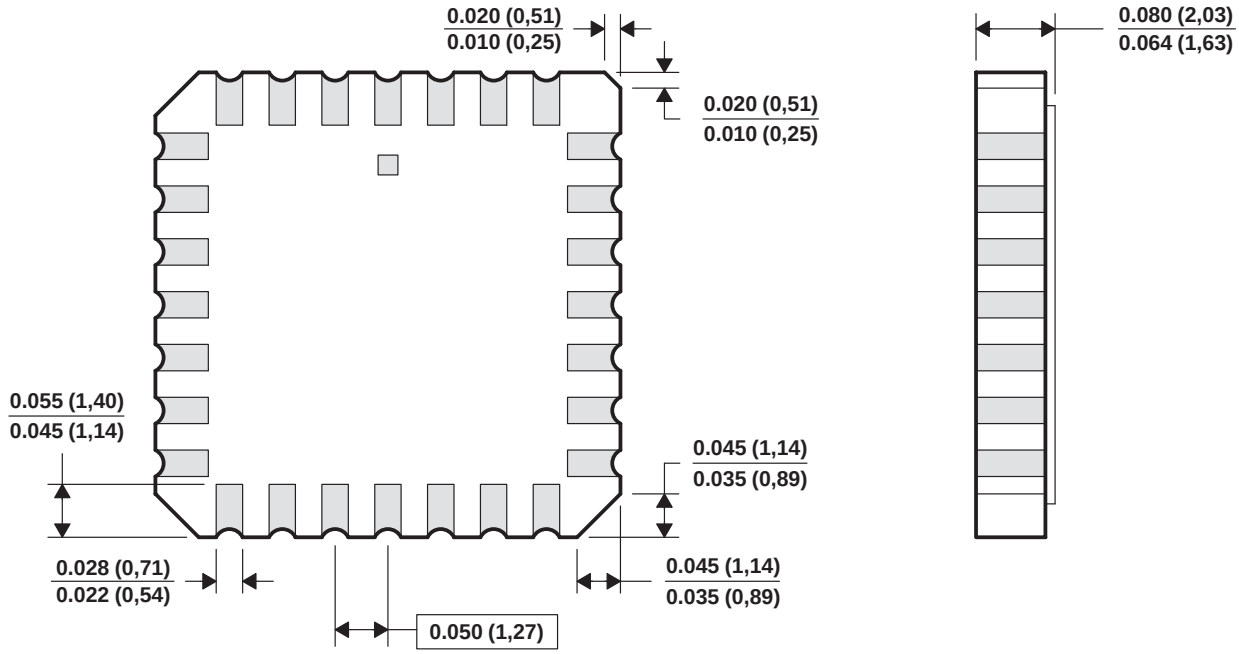
MECHANICAL DATA

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



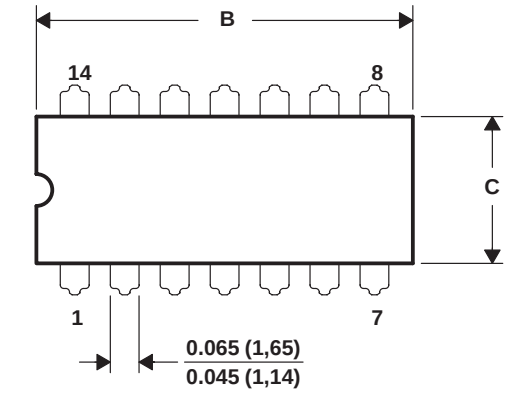
4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

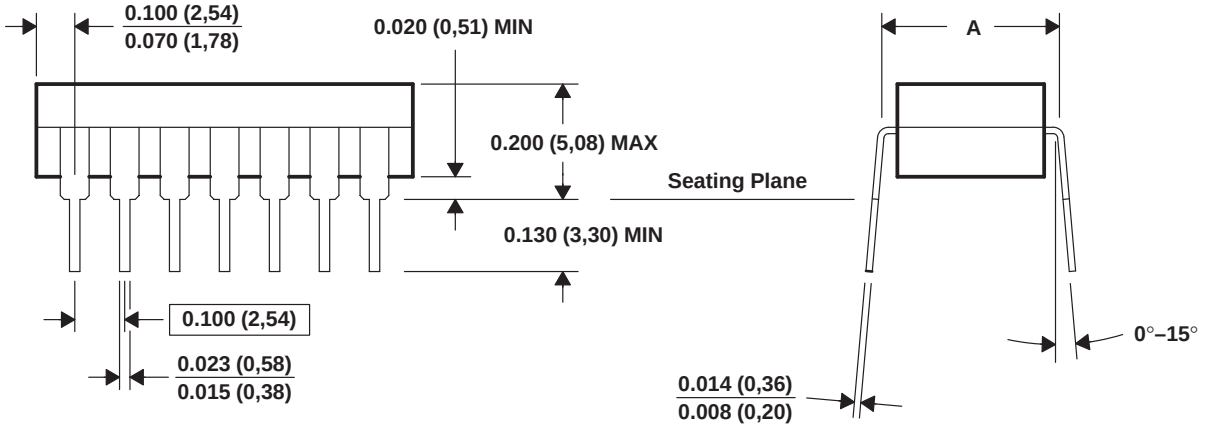
MECHANICAL DATA

J (R-GDIP-T)** **CERAMIC DUAL-IN-LINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)
B MAX	0.785 (19,94)	0.785 (19,94)	0.910 (23,10)	0.975 (24,77)
B MIN	0.755 (19,18)	0.755 (19,18)	—	0.930 (23,62)
C MAX	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)

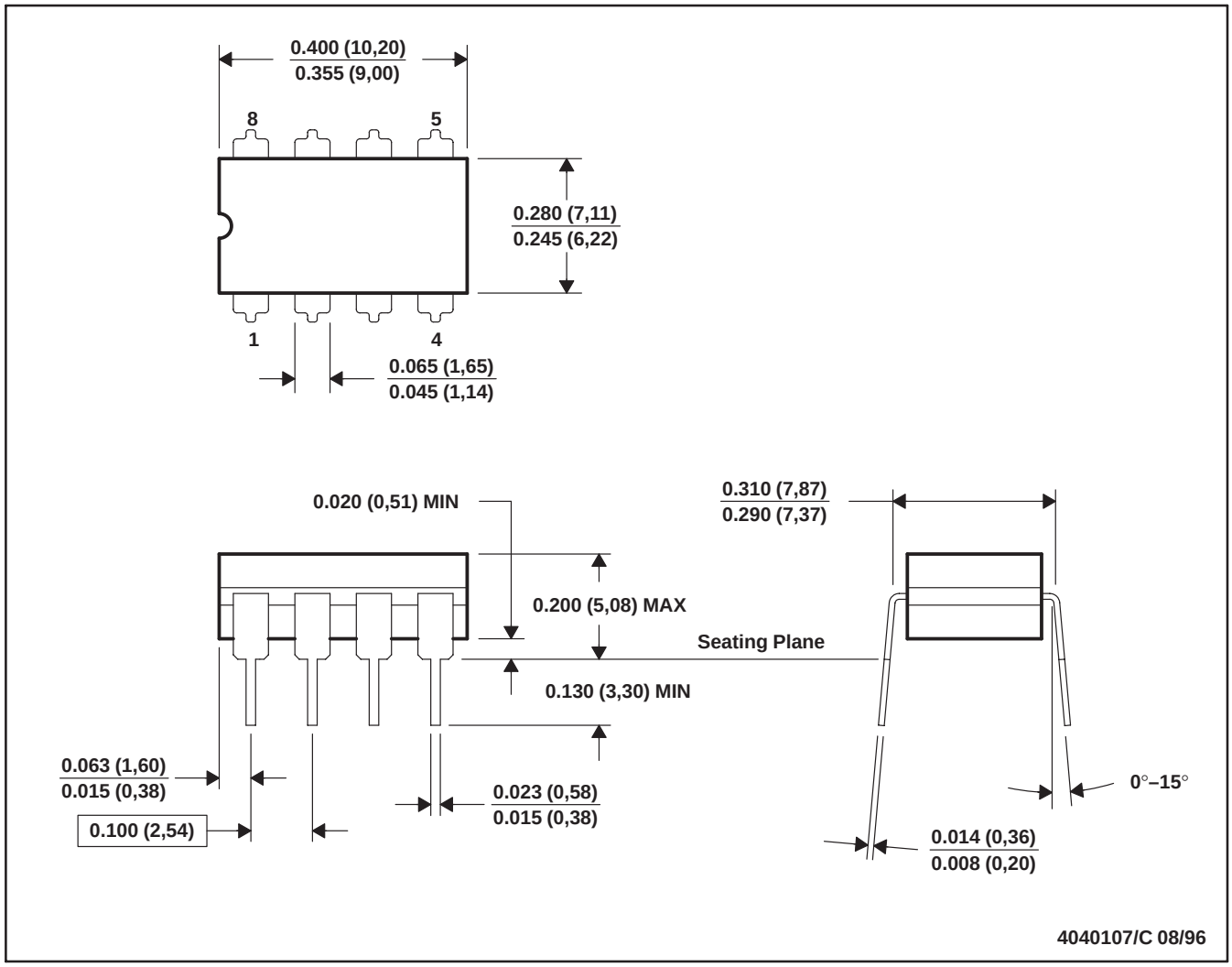


4040083/D 08/98

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, GDIP1-T20, and GDIP1-T22.

MECHANICAL DATA

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE PACKAGE**



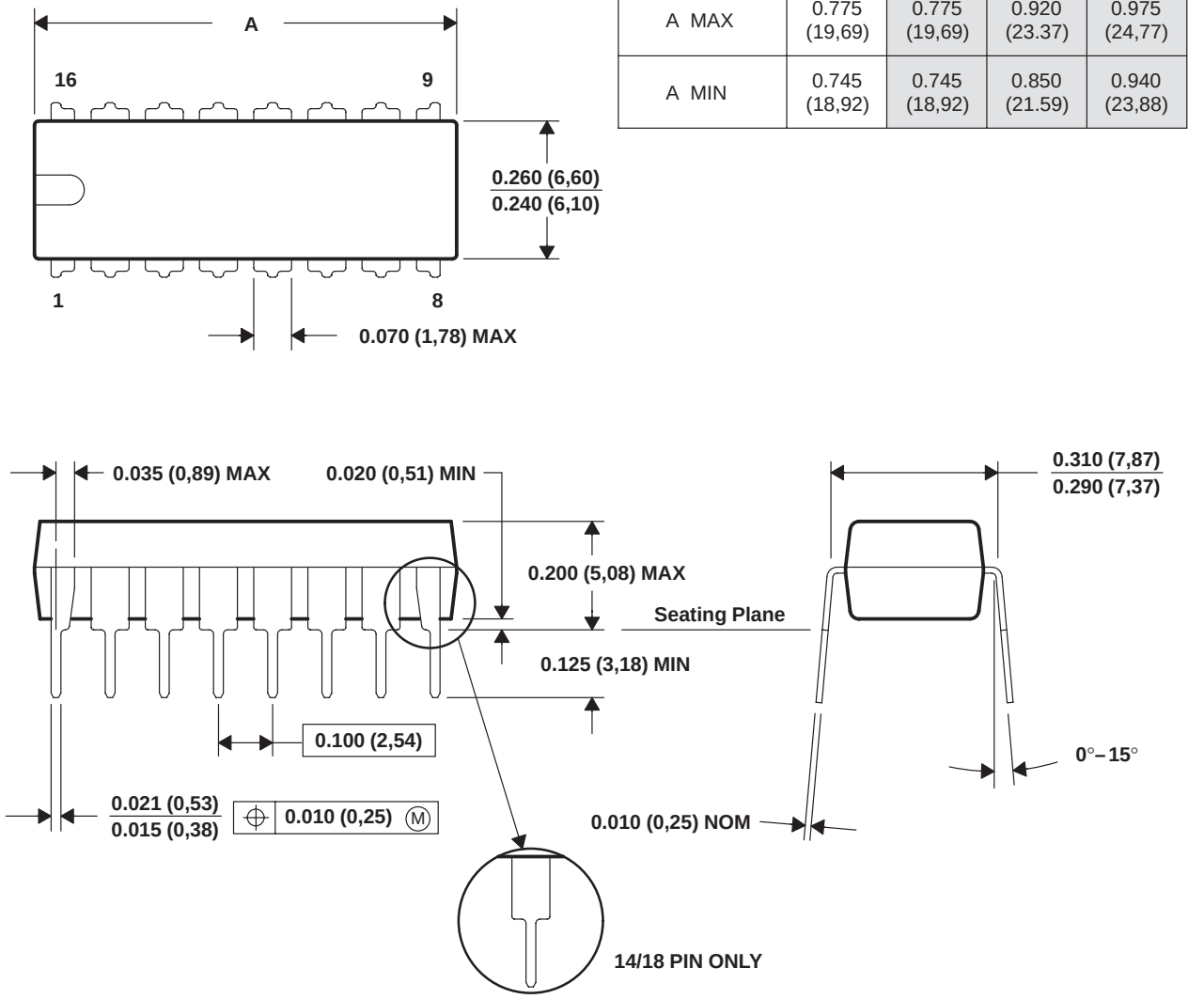
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL-STD-1835 GDIP1-T8

MECHANICAL DATA

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

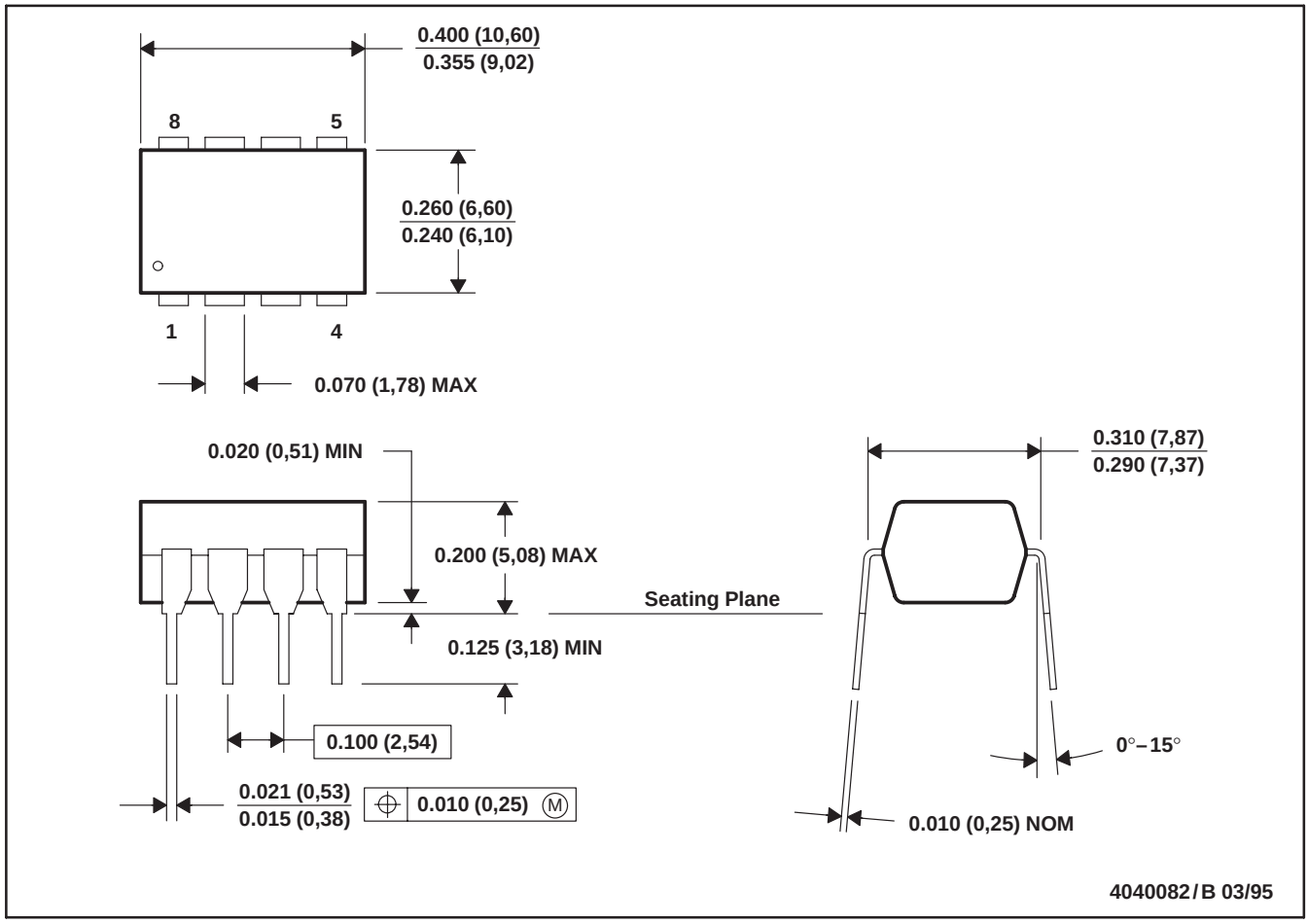
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

MECHANICAL DATA

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**

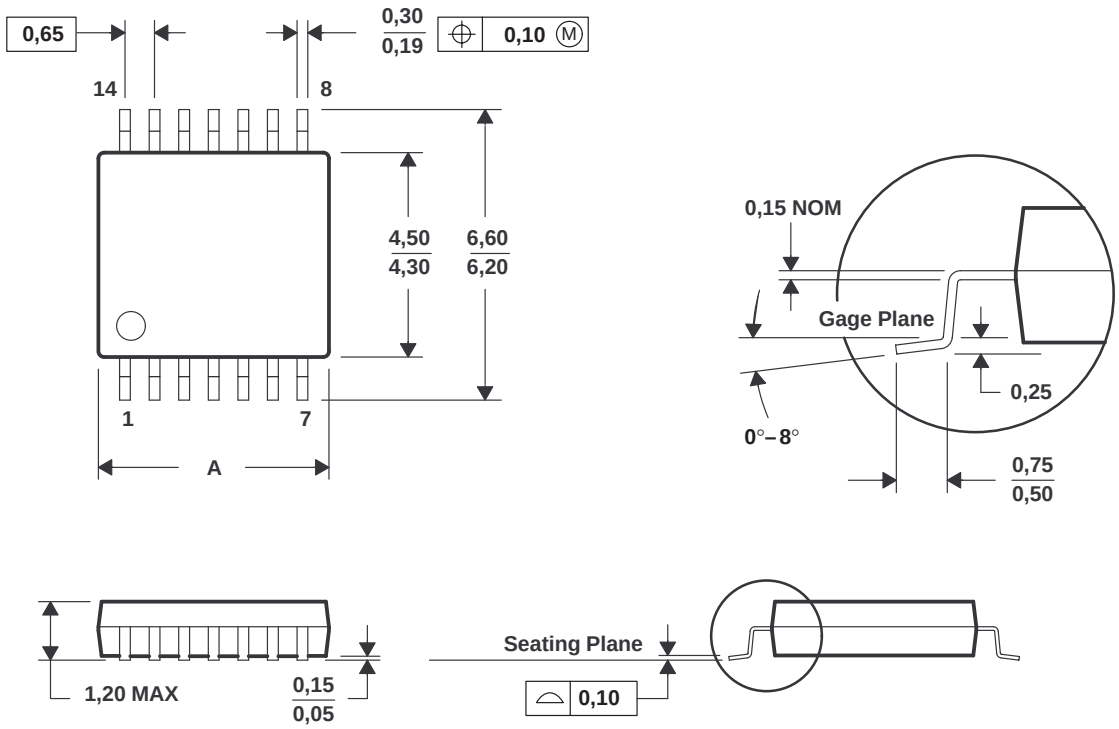


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



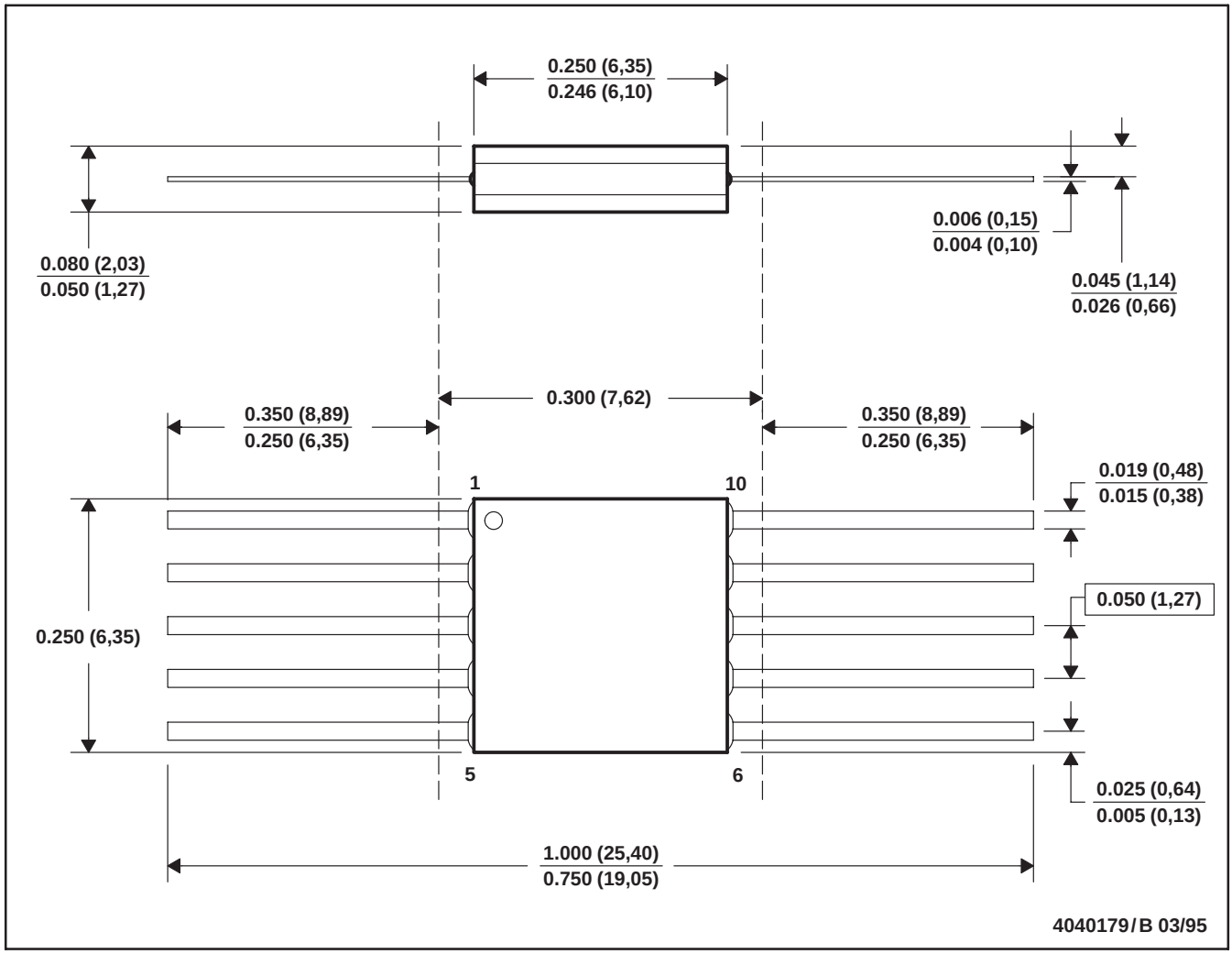
DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/E 08/96

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

MECHANICAL DATA

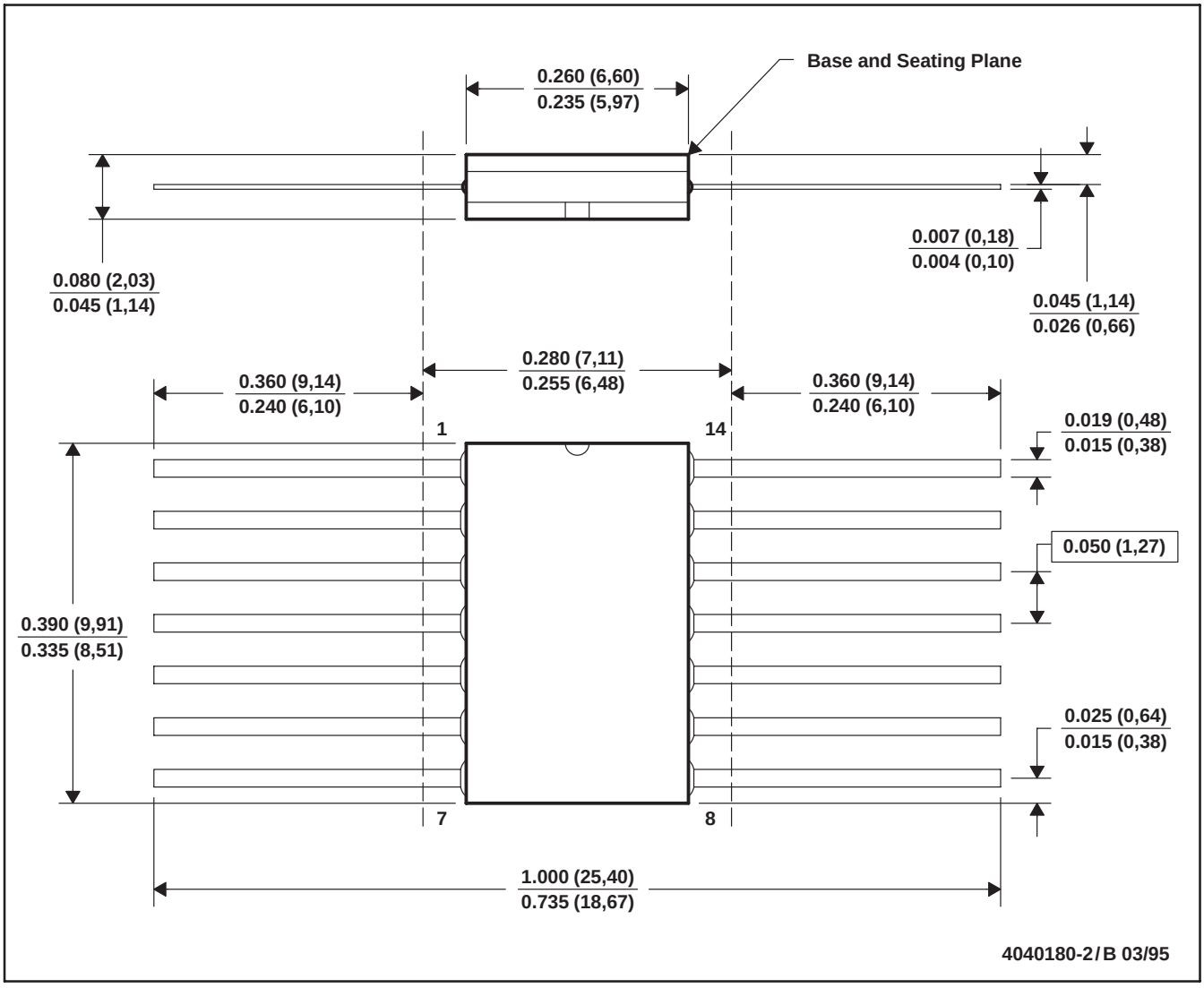
U (S-GDFP-F10) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

MECHANICAL DATA

W (R-GDFP-F14) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

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8-Bit, High Speed, Multiplying D/A Converter (Universal Digital Logic Interface)

DAC08

FEATURES

- **Fast Settling Output Current: 85 ns**
- **Full-Scale Current Prematched to ±1 LSB**
- **Direct Interface to TTL, CMOS, ECL, HTL, PMOS**
- **Nonlinearity to 0.1% Maximum Over Temperature Range**
- **High Output Impedance and Compliance: –10 V to +18 V**
- **Complementary Current Outputs**
- **Wide Range Multiplying Capability: 1 MHz Bandwidth**
- **Low FS Current Drift: ±10 ppm/°C**
- **Wide Power Supply Range: ±4.5 V to ±18 V**
- **Low Power Consumption: 33 mW @ ±5 V**
- **Low Cost**
- **Available in Die Form**

GENERAL DESCRIPTION

The DAC08 series of 8-bit monolithic digital-to-analog converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85 ns settling times with very low "glitch" energy and at low power consumption. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates the need for full-scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic input.

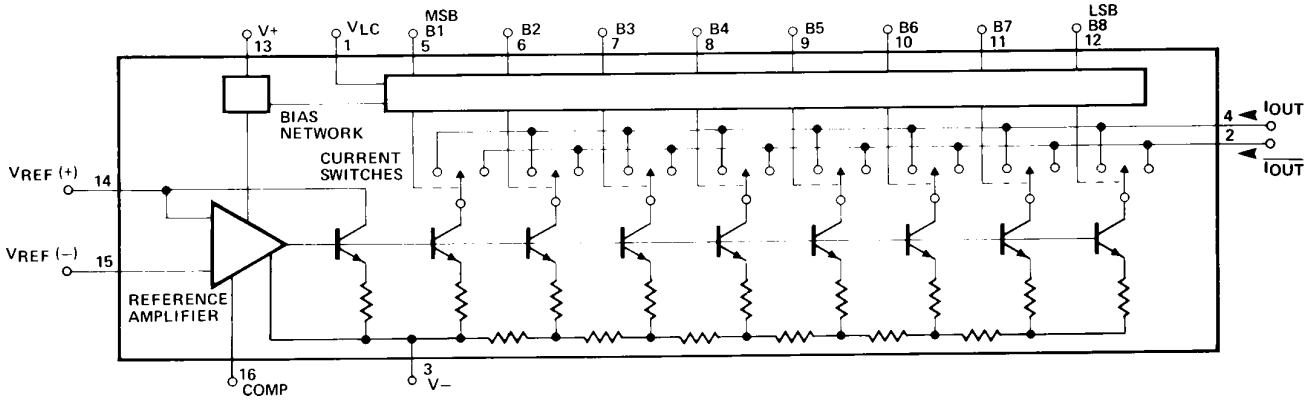
High voltage compliance complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC08 series models guarantee full 8-bit monotonicity, and nonlinearities as tight as ±0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5 V to ±18 V power supply range, with 33 mW power consumption attainable at ±5 V supplies.

The compact size and low power consumption make the DAC08 attractive for portable and military/aerospace applications; devices processed to MIL-STD-883, Level B are available.

DAC08 applications include 8-bit, 1 µs A/D converters, servo motor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high-speed modems and other applications where low cost, high speed and complete input/output versatility are required.

FUNCTIONAL BLOCK DIAGRAM



REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

DAC08–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, I_{REF} = 2.0 mA, –55°C ≤ T_A ≤ +125°C for DAC08/08A, 0°C ≤ T_A ≤ +70°C for DAC08C, E & H unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.)

Parameter	Symbol	Conditions	DAC08A/H Min	DAC08A/H Typ	DAC08A/H Max	DAC08E Min	DAC08E Typ	DAC08E Max	DAC08C Min	DAC08C Typ	DAC08C Max	Units
Resolution			8			8			8			Bits
Monotonicity			8			8			8			Bits
Nonlinearity	NL				±0.1			±0.19			±0.39	% FS
Settling Time	t_S	To ±1/2 LSB, All Bits Switched ON or OFF, T_A = 25°C[1]		85	135		85	150		85	150	ns
Propagation Delay												
Each Bit	t_{PLH}	T_A = 25°C[1]		35	60		35	60		35	60	ns
All Bits Switched	t_{PHL}			35	60		35	60		35	60	ns
Full-Scale Tempco[1]	TCI_{FS}			±10	±50		±10	±80		±10	±80	ppm/°C
		DAC08E						±50				
Output Voltage Compliance (True Compliance)	V_{OC}	Full-Scale Current Change <1/2 LSB, R_{OUT} > 20 MΩ typ	–10		+18	–10		+18	–10		+18	V
Full Range Current	I_{FR4}	V_{REF} = 10.000 V R14, R15 = 5.000 kΩ T_A = +25°C	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry	I_{FRS}	$I_{FR4} - I_{FR2}$		±0.5	±4		±1	±8		±2	±16	µA
Zero-Scale Current	I_{ZS}			0.1	1		0.2	2		0.2	4	µA
Output Current Range	I_{OR1}	R14, R15 = 5.000 kΩ	2.1			2.1			2.1			mA
	I_{OR2}	V_{REF} = +15.0 V, V– = –10 V										
		V_{REF} = +25.0 V, V– = –12 V	4.2			4.2			4.2			mA
Output Current Noise		I_{REF} = 2 mA		25			25			25		nA
Logic Input Levels												
Logic "0"	V_{IL}	V_{LC} = 0 V			0.8			0.8			0.8	V
Logic Input "1"	V_{IL}		2			2			2			V
Logic Input Current		V_{LC} = 0 V										
Logic "0"	I_{IL}	V_{IN} = –10 V to +0.8 V		–2	–10		–2	–10		–2	–10	µA
Logic Input "1"	I_{IH}	V_{IN} = 2.0 V to 18 V		0.002	10		0.002	10		0.002	10	µA
Logic Input Swing	V_{IS}	V– = –15 V	–10		+18	–10		+18	–10		+18	V
Logic Threshold Range	V_{THR}	V_S = ±15 V[1]	–10		+13.5	–10		+13.5	–10		+13.5	V
Reference Bias Current	I_{15}			–1	–3		–1	–3		–1	–3	µA
Reference Input Slew Rate	dI/dt	R_{EQ} = 200 Ω R_L = 100 Ω C_C = 0 pF See Fast Pulsed Ref. Info Following.[1]	4	8		4	8		4	8		mA/µs
Power Supply Sensitivity	$PSSI_{FS+}$	V+ = 4.5 V to 18 V		±0.0003	±0.01		±0.0003	±0.01		±0.0003	±0.01	$\%\Delta I_O/\%\Delta V+$
	$PSSI_{FS-}$	V– = –4.5 V to –18 V I_{REF} = 1.0 mA		±0.002	±0.01		±0.002	±0.01		±0.002	±0.01	$\%\Delta I_O/\%\Delta V-$
Power Supply Current	I+	V_S = ±5 V, I_{REF} = 1.0 mA		2.3	3.8		2.3	3.8		2.3	3.8	mA
	I–			–4.3	–5.8		–4.3	–5.8		–4.3	–5.8	mA
	I+	V_S = +5 V, –15 V,		2.4	3.8		2.4	3.8		2.4	3.8	mA
	I–	I_{REF} = 2.0 mA		–6.4	–7.8		–6.4	–7.8		–6.4	–7.8	mA
	I+	V_S = ±15 V, I_{REF} =		2.5	3.8		2.5	3.8		2.5	3.8	mA
	I–	2.0 mA		–6.5	–7.8		–6.5	–7.8		–6.5	–7.8	mA
Power Dissipation	P_d	±5 V, I_{REF} = 1.0 mA		33	48		33	48		33	48	mW
		+5 V, –15 V, I_{REF} = 2.0 mA		108	136		103	136		108	136	mW
		±15 V, I_{REF} = 2.0 mA		135	174		135	174		135	174	mW

NOTES

[1]Guaranteed by design.

Specifications subject to change without notice.

TYPICAL ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, and I_{REF} = 2.0 mA, unless otherwise noted. Output characteristics apply to both I_{OUT} and $\overline{I_{OUT}}$.)

Parameter	Symbol	Conditions	All Grades Typical	Units
Reference Input Slew Rate	dI/dt		8	mA/μs
Propagation Delay	t_{PLH}, t_{PHL}	T_A = 25°C, Any Bit	35	ns
Settling Time	t_S	To ±1/2 LSB, All Bits Switched ON or OFF, T_A = 25°C	85	ns

NOTES
For DAC08NT & GT 25°C characteristics, see DAC08N & G characteristics respectively.
Specifications subject to change without notice

ABSOLUTE MAXIMUM RATINGS[1]

Operating Temperature
DAC08AQ, Q .....–55°C to +125°C
DAC08HQ, EQ, CQ, HP, EP, CP, CS ..... 0°C to +70°C
Junction Temperature (T_J) .....–65°C to +150°C
Storage Temperature Q Package .....–65°C to +150°C
Storage Temperature P Package .....–65°C to +125°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
V+ Supply to V– Supply .....36 V
Logic Inputs .....V– to V– plus 36 V
V_{LC} ..... V– to V+
Analog Current Outputs (at V_S– = 15 V) ..... 4.25 mA
Reference Input (V_{14} to V_{15}) ..... V– to V+
Reference Input Differential Voltage
(V_{14} to V_{15}) ..... ±18 V
Reference Input Current (I_{14}) ..... 5.0 mA

Package Type	θ_{JA}[2]	θ_{JC}	Units
16-Pin Hermetic DIP (Q)	100	16	°C/W
16-Pin Plastic DIP (P)	82	39	°C/W
20-Contact LCC (RC)	76	36	°C/W
16-Pin SO (S)	111	35	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

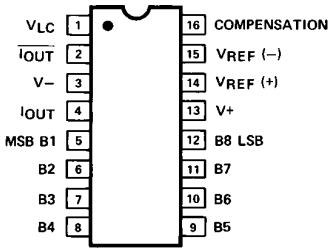
ORDERING GUIDE[1]

NL	16-Pin Dual-In-Line Package			Operating Temperature Range
	Hermetic	Plastic	LCC	
0.1%	DAC08AQ[2]			MIL
	DAC08HQ	DAC08HP		COM
0.19%	DAC08Q[2]		DAC08RC/883	MIL
	DAC08EQ	DAC08EP		COM
0.39%	DAC08CQ	DAC08CP		COM
		DAC08CS[3]		COM

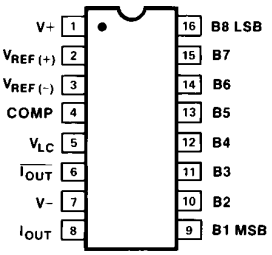
NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic DIP, and TO-can packages.
[2]For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.
[3]For availability and burn-in information on SO and PLCC packages, contact your local sales office.

PIN CONNECTIONS

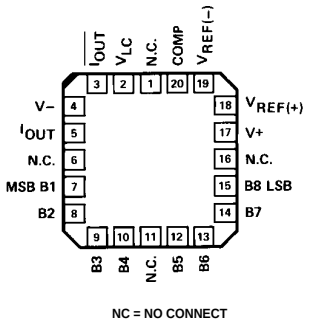
16-Pin Dual-In-Line Package (Q Suffix)



16-Lead SO (S Suffix)



DAC08RC/883 20-Lead LCC (RC Suffix)



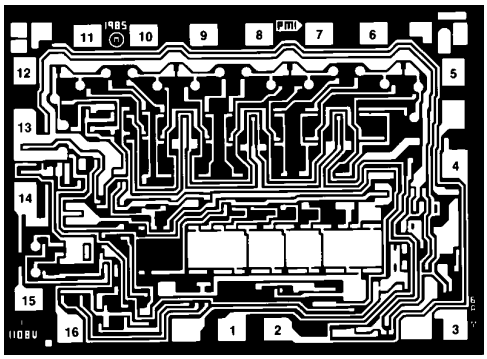
WAFER TEST LIMITS (@ V_S = ±15 V, I_{REF} = 2.0 mA, T_A = 125°C for DAC08NT, DAC08GT devices; T_A = 25°C for DAC08N, DAC08G and DAC08GR devices, unless otherwise noted. Output characteristics apply to both I_{OUT} and $\overline{I_{OUT}}$.)

Parameter	Symbol	Conditions	DAC08NT Limit	DAC08N Limit	DAC08GT Limit	DAC08G Limit	DAC08GR Limit	Units
Resolution			8	8	8	8	8	Bits min
Monotonicity			8	8	8	8	8	Bits min
Nonlinearity	NL		±0.1	±0.1	±0.19	±0.19	±0.39	% FS max
Output Voltage	V_{OC}	Full-Scale Current	+18	+18	+18	+18	+18	V max
Compliance		Change < 1/2 LSB	–10	–10	–10	–10	–10	V min
Full-Scale Current	I_{FS4} or	V_{REF} = 10.000 V	2.04	2.04	2.04	2.04	2.04	mA max
	I_{FS2}	R_{14}, R_{15} = 5.000 kΩ	1.94	1.94	1.94	1.94	1.94	mA min
Full-Scale Symmetry	I_{FSS}		±8	±8	±8	±8	±16	µA max
Zero-Scale Current	I_{ZS}		2	2	4	4	4	µA max
Output Current Range	I_{FS1}	V– = –10 V, V_{REF} = +15 V	2.1	2.1	2.1	2.1	2.1	mA min
	I_{FS2}	V– = –12 V, V_{REF} = +25 V, R_{14}, R_{15} = 5.000 kΩ	4.2	4.2	4.2	4.2	4.2	mA min
Logic Input "0"	V_{IL}		0.8	0.8	0.8	0.8	0.8	V max
Logic Input "1"	V_{IH}		2	2	2	2	2	V min
Logic Input Current		V_{LC} = 0 V						
Logic "0"	I_{IL}	V_{IN} = –10 V to +0.8 V	±10	±10	±10	±10	±10	µA max
Logic "1"	I_{IH}	V_{IN} = 2.0 V to 18 V	±10	±10	±10	±10	±10	µA max
Logic Input Swing	V_{IS}	V– = –15 V	+18	+18	+18	+18	+18	V max
			–10	–10	–10	–10	–10	V min
Reference Bias Current	I_{15}		–3	–3	–3	–3	–3	µA max
Power Supply	$PSSI_{FS+}$	V+ = 4.5 V to 18 V	0.01	0.01	0.01	0.01	0.01	% FS/% V max
Sensitivity	$PSSI_{FS-}$	V– = –4.5 V to –18 V, I_{REF} = 1.0 mA						
Power Supply Current	I+	V_S = ±15 V	3.8	3.8	3.8	3.8	3.8	mA max
		I_{REF} ≤ 2.0 mA	–7.8	–7.8	–7.8	–7.8	–7.8	µA max
Power Dissipation	P_d	V_S = ±15 V, I_{REF} ≤ 2.0 mA	174	174	174	174	174	mW max

NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

DICE CHARACTERISTICS

(+125°C Tested Dice Available)



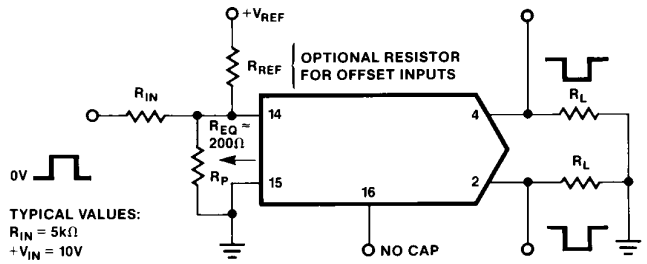


Figure 1. Pulsed Reference Operation

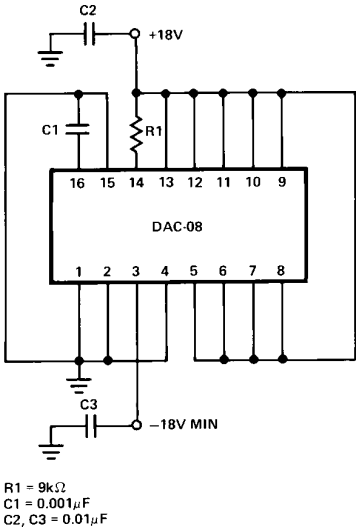


Figure 2. Burn-in Circuit

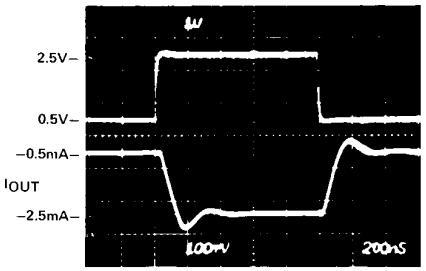


Figure 3. Fast Pulsed Reference Operation

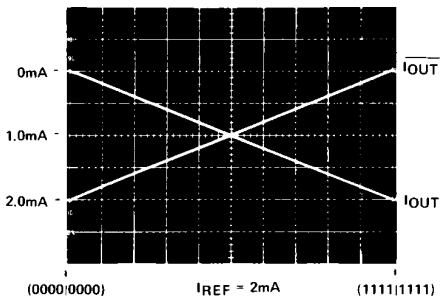


Figure 4. True and Complimentary Output Operation

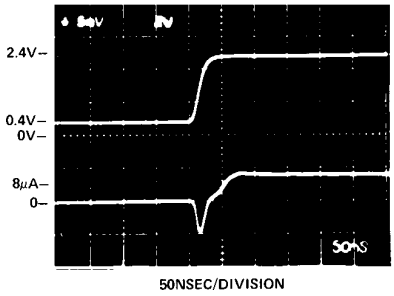


Figure 5. LSB Switching

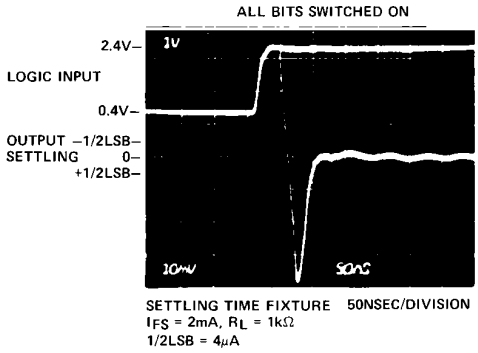


Figure 6. Full-Scale Settling Time

DAC08–Typical Performance Characteristics

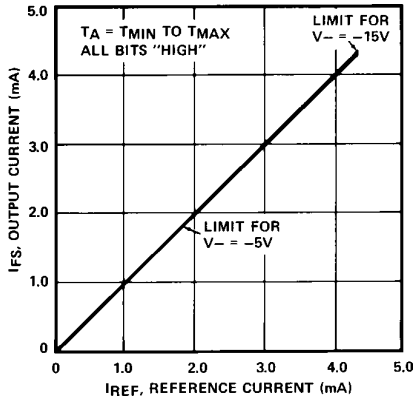


Figure 7. Full-Scale Current vs. Reference Current

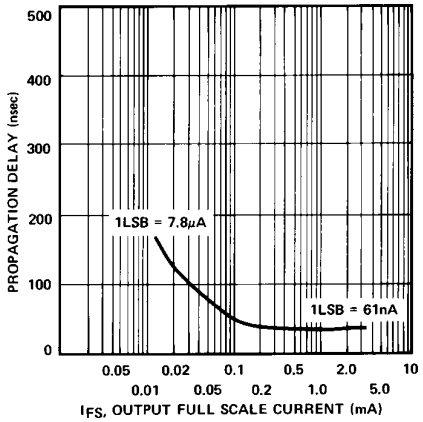


Figure 8. LSB Propagation Delay vs. I_{FS}

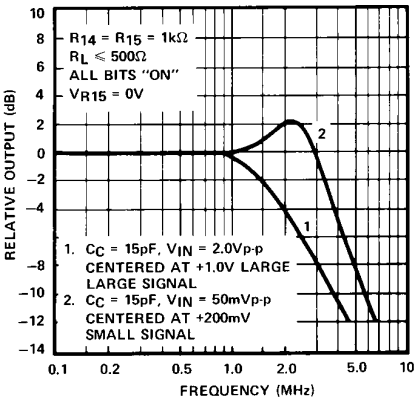


Figure 9. Reference Input Frequency Response

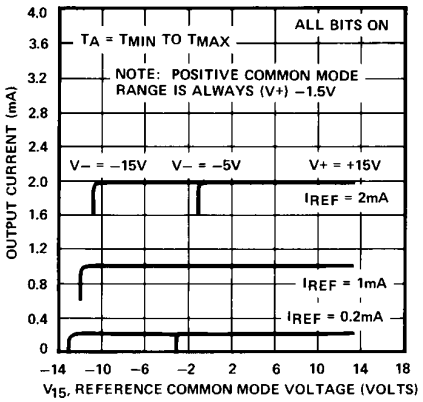


Figure 10. Reference Amp Common-Mode Range

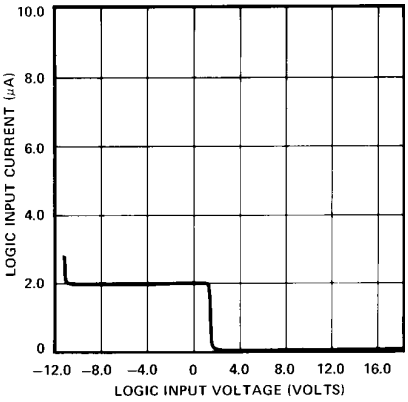


Figure 11. Logic Input Current vs. Input Voltage

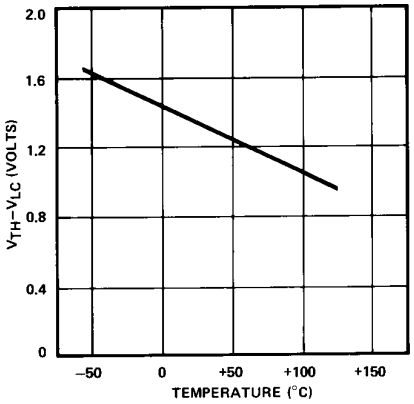


Figure 12. V_{TH}–V_{LC} vs. Temperature

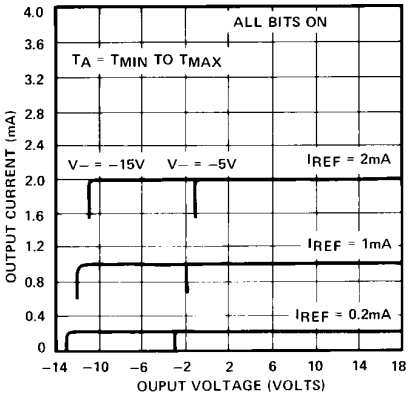


Figure 13. Output Current vs. Output Voltage (Output Voltage Compliance)

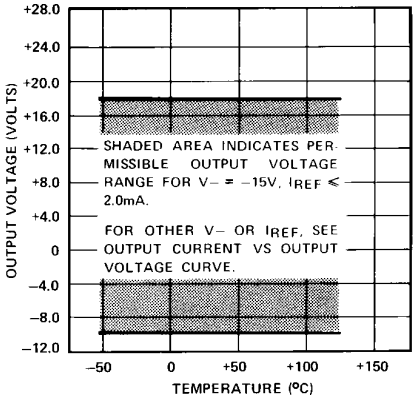


Figure 14. Output Voltage Compliance vs. Temperature

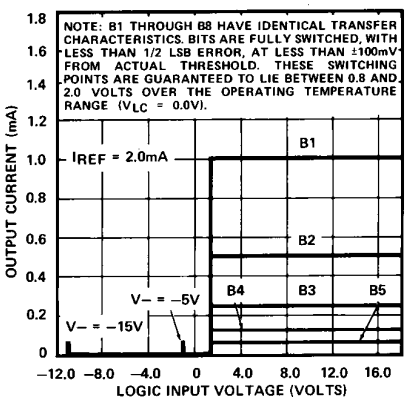


Figure 15. Bit Transfer Characteristics

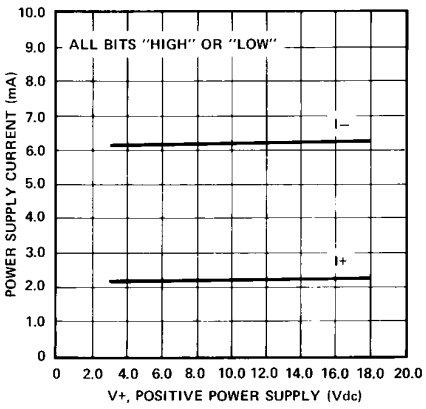


Figure 16. Power Supply Current vs. V+

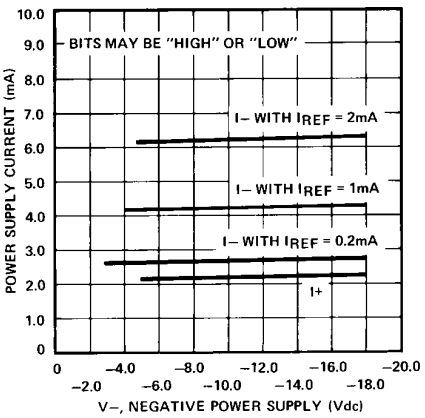


Figure 17. Power Supply Current vs. V–

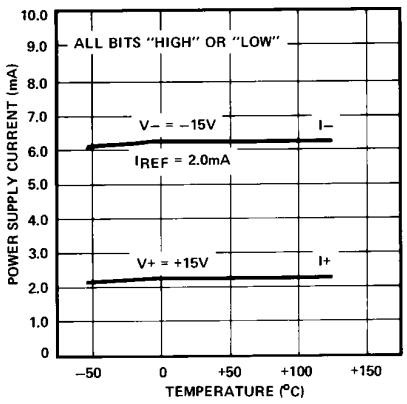


Figure 18. Power Supply Current vs. Temperature

BASIC CONNECTIONS

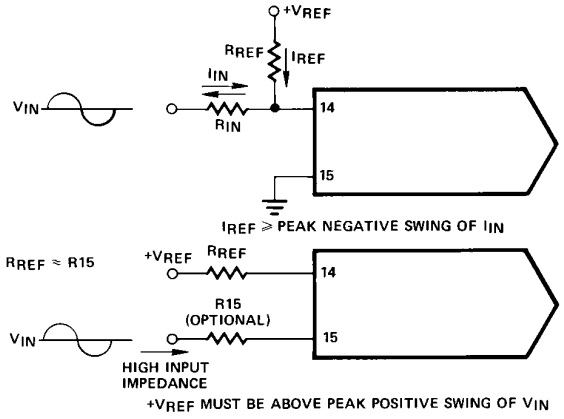


Figure 19. Accomodating Bipolar References

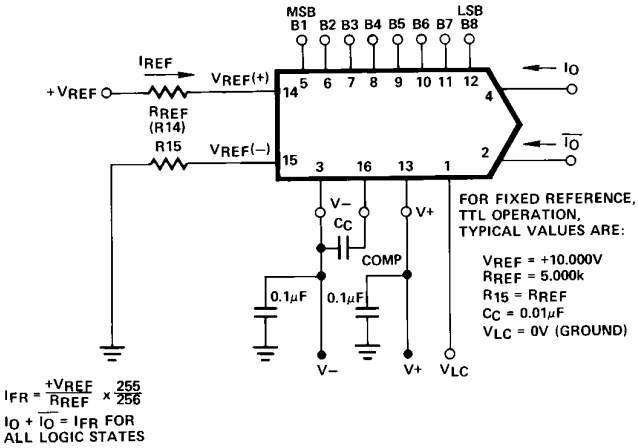
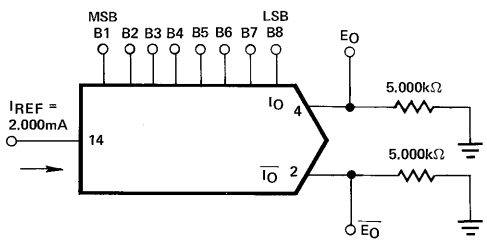
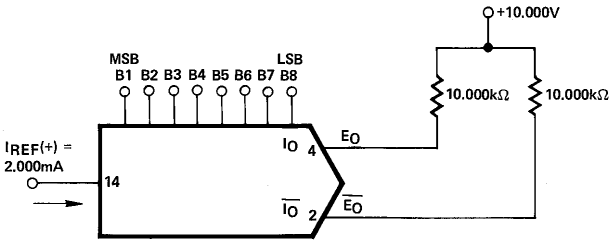


Figure 20. Basic Positive Reference Operation



	B1	B2	B3	B4	B5	B6	B7	B8	I_OmA	$\overline{I_O}$mA	E_O	$\overline{E_O}$
FULL RANGE	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	− .000
HALF-SCALE +LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
HALF-SCALE	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
HALF-SCALE −LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
ZERO-SCALE +LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
ZERO-SCALE	0	0	0	0	0	0	0	0	0.000	1.992	0.000	−9.960

Figure 21. Basic Unipolar Negative Operation



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
POS. FULL RANGE	1	1	1	1	1	1	1	1	− 9.920	+10.000
POS. FULL RANGE −LSB	1	1	1	1	1	1	1	0	− 9.840	+ 9.920
ZERO-SCALE +LSB	1	0	0	0	0	0	0	1	− 0.080	+ 0.160
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000	+ 0.080
ZERO-SCALE −LSB	0	1	1	1	1	1	1	1	+ 0.080	0.000
NEG. FULL-SCALE +LSB	0	0	0	0	0	0	0	1	+ 9.920	− 9.840
NEG. FULL-SCALE	0	0	0	0	0	0	0	0	+10.000	− 9.920

Figure 22. Basic Bipolar Output Operation

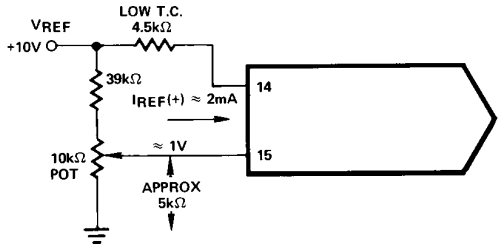


Figure 23. Recommended Full-Scale Adjustment Circuit

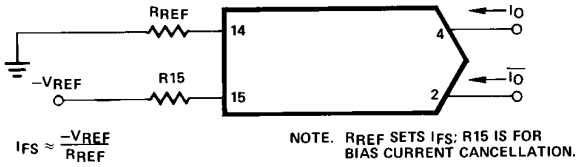
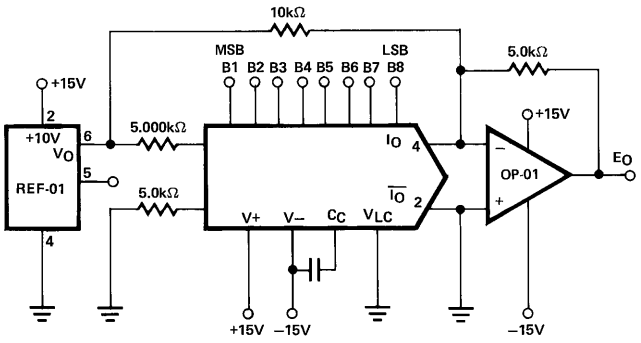
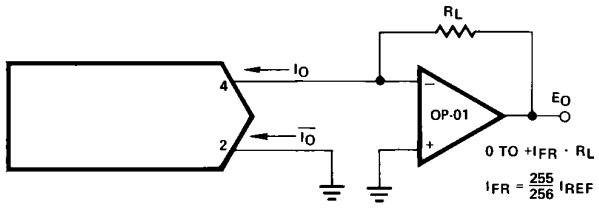


Figure 24. Basic Negative Reference Operation



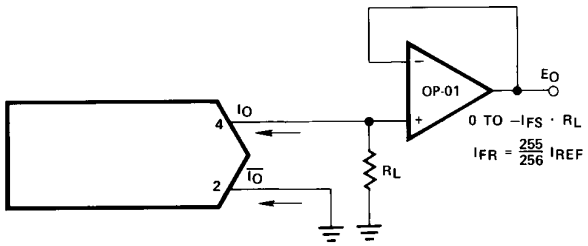
	B1	B2	B3	B4	B5	B6	B7	B8	E_O
POS. FULL RANGE	1	1	1	1	1	1	1	1	+4.960
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000
NEG. FULL-SCALE +1 LSB	0	0	0	0	0	0	0	1	−4.960
NEG. FULL-SCALE	0	0	0	0	0	0	0	0	−5.000

Figure 25. Offset Binary Operation



FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

Figure 26. Positive Low Impedance Output Operation



FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC), CONNECT NONINVERTING INPUT OF OP-AMP TO I_O (PIN 2); CONNECT I_O (PIN 4) TO GROUND.

Figure 27. Negative Low Impedance Output Operation

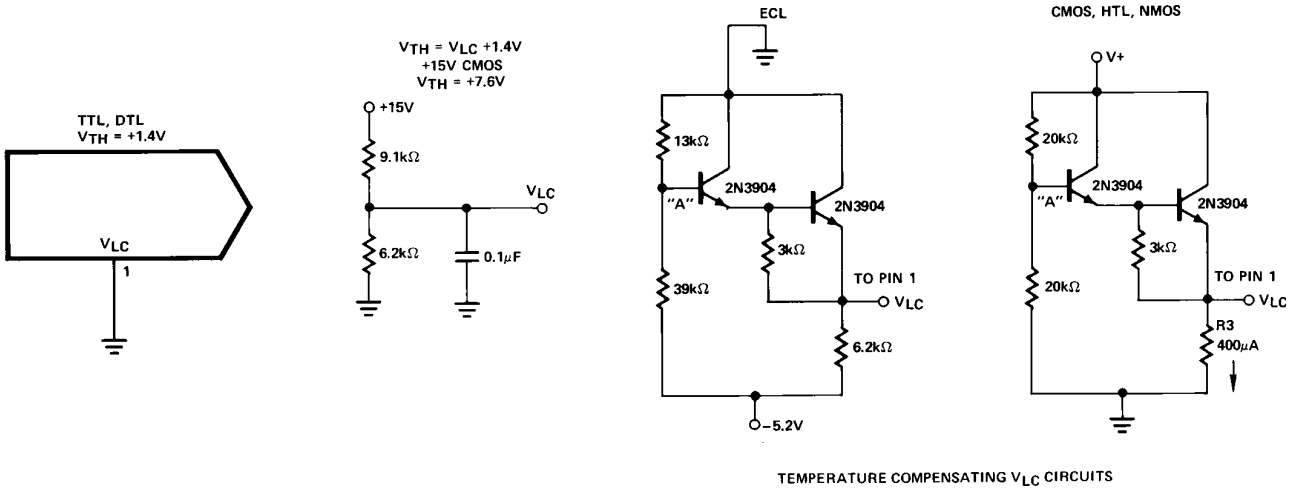


Figure 28. Interfacing With Various Logic Families

APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SET-UP

The DAC08 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0 mA. The full-scale output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{255}{256} \times I_{REF}, \text{ where } I_{REF} = I_{14}.$$

In positive reference applications, an external positive reference voltage forces current through R14 into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15; reference current flows from ground through R14 into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) is used to cancel bias current errors; R15 may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or pin 15. The negative common-mode range of the reference amplifier is given by: $V_{CM}-$ = V– plus ($I_{REF} \times 1\ k\Omega$) plus 2.5 V. The positive common-mode range is V+ less 1.5 V.

When a dc reference is used, a reference bypass capacitor is recommended. A 5.0 V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R14 should be split into two resistors with the junction bypassed to ground with a 0.1 μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14. An improved method of full-scale trimming which eliminates potentiometer T.C. effects is shown in the recommended full-scale adjustment circuit.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common-mode range. The recommended range for operation with a dc reference current is +0.2 mA to +4.0 mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V–. The value of this capacitor depends on the impedance presented to pin 14: for R14 values of 1.0, 2.5 and 5.0 kΩ, minimum values of C_C are 15, 37, and 75 pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin, such that the ratio of C_C (pF) to R14 (kΩ) = 15.

For fastest response to a pulse, low values of R14 enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R14 = 1 kΩ and C_C = 15 pF, the reference amplifier slews at 4 mA/μs enabling a transition from I_{REF} = 0 to I_{REF} = 2 mA in 500 ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full-scale transition (0 mA to 2 mA) occurs in 120 ns when the equivalent impedance at pin 14 is 200 Ω and C_C = 0. This yields a reference slew rate of 16 mA/μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2 μA logic input current and completely adjustable logic threshold voltage. For V– = –15 V, the logic inputs may swing between –10 V and +18 V. This enables direct interface with +15 V CMOS logic, even when the DAC08 is powered from a +5 V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V– plus ($I_{REF} \times 1$ kΩ) plus 2.5 V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC}. For TTL and DTL interface, simply ground pin 1. When interfacing ECL, an I_{REF} = 1 mA is recommended. For interfacing other logic families, see preceding page. For general set-up of the logic control circuit, it should be noted that pin 1 will source 100 μA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1 kΩ divider, for example, it should be bypassed to ground by a 0.01 μF capacitor.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FS}$. Current appears at the "true" (I_O) output when a "1" (logic high) is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must be connected to ground or to a point capable of sourcing I_{FS}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36 V above V– and is independent of the positive supply. Negative compliance is given by V– plus ($I_{REF} \times 1$ kΩ) plus 2.5 V.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC08 operates over a wide range of power supply voltages from a total supply of 9 V to 36 V. When operating at supplies of ±5 V or less, $I_{REF} \leq 1$ mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at –4.5 V with I_{REF} = 2 mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8 V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required: however, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

Power consumption may be calculated as follows:

P_d = (I+) (V+) + (I–) (V–). A useful feature of the DAC08 design is that supply current is constant and independent of input logic states; this is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC08 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is low, typically ±10 ppm/°C, with zero-scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full-scale drift. Settling times of the DAC08 decrease approximately 10% at –55°C; at +125°C an increase of about 15% is typical.

The reference amplifier must be compensated by using a capacitor from pin 16 to V–. For fixed reference operation, a 0.01 μF capacitor is recommended. For variable reference applications, see previous section entitled "Reference Amplifier Compensation for Multiplying Applications".

MULTIPLYING OPERATION

The DAC08 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4 mA to 4 mA. Monotonic operation is maintained over a typical range of I_{REF} from 100 μA to 4.0 mA.

SETTLING TIME

The DAC08 is capable of extremely fast settling times, typically 85 ns at I_{REF} = 2.0 mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35 ns for each of the 8 bits. Settling time to within 1/2 LSB of the LSB is therefore 35 ns, with each progressively larger bit taking successively longer. The MSB settles in 85 ns, thus determining the overall settling time of 85 ns. Settling to 6-bit accuracy requires about 65 ns to 70 ns. The output capacitance of the DAC08 including the package is approximately 15 pF, therefore the output RC time constant dominates settling time if R_L > 500 Ω.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±4 μA, therefore a 1 kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture shown in schematic labelled "Settling Time Measurement" uses a cascode design to permit driving a 1 kΩ load with less than 5 pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1.0 mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value, and thus settling times may be observed at lower values of I_{REF}.

DAC08 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1 μF capacitors at the supply pins provide full transient protection.

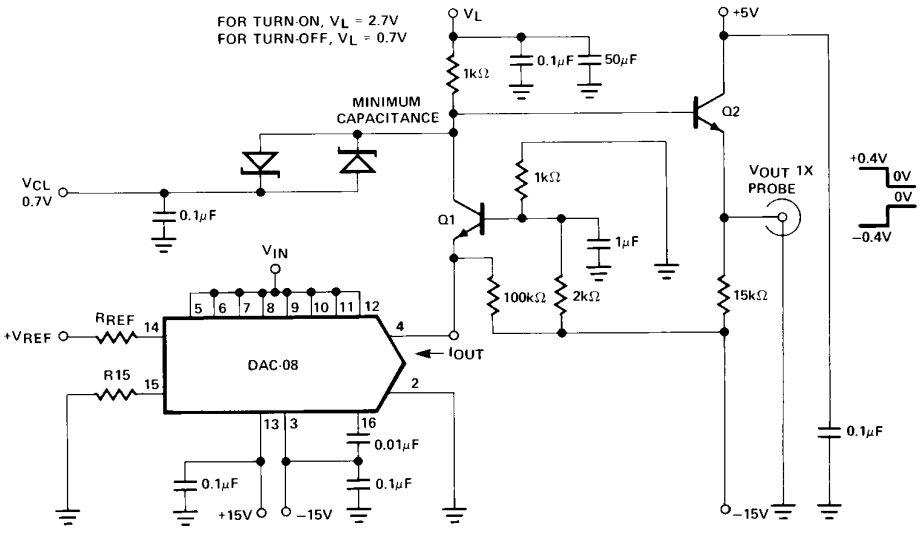
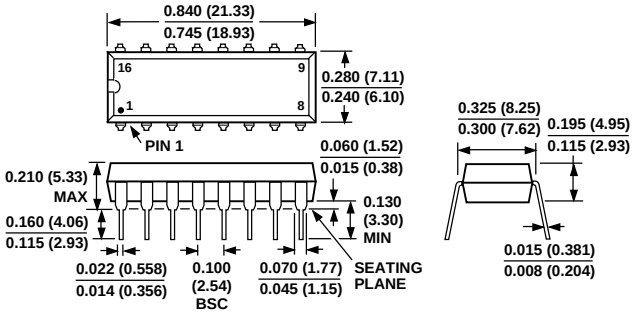


Figure 30. Settling Time Measurement

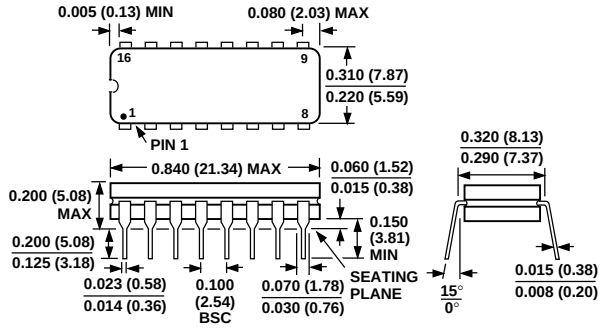
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

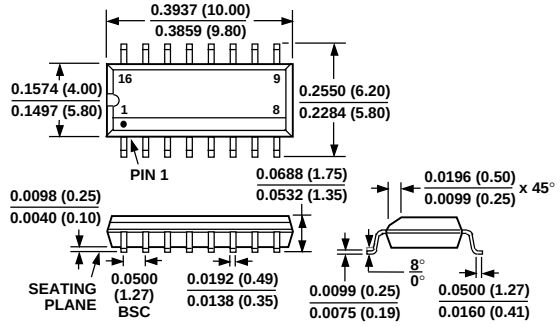
N-16



Q-16



SO-16



E-20