TRANSFERRING ECG SIGNAL BY GSM TECHNOLOGY

BY

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A PROJECT REPORT SUBMITTED IN PARTIAL FULFILMENT OF
REQUREMENTS FOR THE DEGREE OF
BACHLOR OF ENGINEERING
IN
COMMUNICATIONS & ELECTRONICS ENGINEERING

SUPERVISED BY

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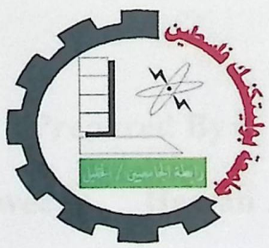

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PALESTINE POLYTECHNIC UNIVERSITY

HEBRON – WEST BANK

PALESTINE

2010-2011

CERTIFICATION

Palestine Polytechnic University (PPU)

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In accordance with the recommendation of the project supervisor, and the acceptance of all examining committee members, this project has been submitted to the Department of Electrical and Computer Engineering in the college of Engineering and Technology in partial fulfillment of the requirements of Department for the degree of Bachelor of Science in Engineering.

Project Supervisors **Department Chairman**

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19/6/2011

الإهداء

إلى شهدائنا الأبرار الذين قدموا أرواحهم رخيصة في سبيل الله

إلى أسرى الحرية القابعين خلف القضبان

إلى كل المرابطين على أرض الإسراء

إلى آبائنا وأمهاتنا وأقاربنا

إليكم جميعا نهدي هذا العمل المتواضع

فريق المشروع

ACKNOWLEDGEMENT

We like to express our thanks and gratitude to Allah who granted us the ability and willing to start and complete this Project. We pray to his greatness to inspire us the right path to his content and enable us to continue the work started in this project to benefits of our country.

We wish to express our deep thanks and gratitude to Palestine Polytechnic University, College of Engineering and Technology, Electrical and Computer Department, and Specialty Communications and Electronics Engineering. We wish to express our thanks to Eng. Ahmad Qudaimat, for a valuable help, encouragement, supervision and guidance in solving the problems that we face from time to time during this project.

We can find no words to express our sincere, appreciation and gratitude to our parents, sisters and brothers, for their endless support and encouragement, we are deeply indebted to you and we hope that we may someday reciprocate it in some way.

Project Team

ABSTRACT

Transferring ECG Signal By GSM Technology

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The Electrocardiography (ECG) is an essential diagnostic tool that measures and records the electrical activity of the heart. A wide range of heart conditions can be detected when interpreting the recorded ECG signals.

The project focuses on the patients who are at risk of having heart problems without keeping them at the hospital.

The project consists of ECG monitor device, PIC microcontroller, GSM /GPRS Module at the telemedicine unit ,GSM /GPRS Module at the base unit and PC. The main objective of this project is to transfer the ECG signal from the ambulance/home to the doctor ,who is in the emergency center in the hospital. To do this, a microcontroller is used and a PIC software is developed to convert and transmit the analog ECG signal from the GSM /GPRS Module at the telemedicine unit to the GSM /GPRS Module at the base unit. Also , it is very important to develop a software to receive the data from the GSM /GPRS Module at the base unit and to display it on the PC.

This is the second part of the documentation and it is concerned with the telecommunication team objectives, components and procedures . The other team (computer team) is concerned with the other objectives and components of this project .

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INTRODUCTION

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INTRODUCTION

1.1 Overview:

The development and diffusion in the massive means of communication, especially the wireless media in recent decades has led to the emergence of many applications and areas of research in all aspects of life, including telemedicine.

The telemedicine research areas are important for more than three decades. Nowadays, it has become for Telemedicine a lot of benefits, applications, and services as a result of the use of modern wireless communication systems such as GSM, GPRS, satellite, and wireless local area networks.

Due to the need of our society on the use of modern technical means, and as a result of the difficult conditions we are experiencing because of the occupation, where the occupation to stop ambulances at checkpoints for hours, despite the presence of a patient inside. For this, our project aims are to move the reference ECG from the ambulance to the doctor in the emergency center in the hospital, the doctor diagnoses the patient's condition and provides guidance to medical personnel on how to deal with the patient and provide initial treatment to him. This method helps to preserve the lives of patients and serious cases in particular.

Through our search for the best way to apply this technique in our country, in terms of quality of service, ease of construction, and lower cost so that our project is subject to the application on the ground we have to favor the use of advanced system of GSM, a system GPRS, where the system provides much higher on the transfer of information between ambulance and hospital, in addition to the wide coverage of this system in all Palestinian areas.

1.2 Importance of the Project:

The importance of our project lies mainly through one of the most important commonly essential tool, it's the ECG signal or the ECG test .

In our project we will transfer the ECG signal automatically from ambulance to the emergency office directly by using high technology; to reduce the time and effort used in transfer ECG signal ,more accurate diagnosis for the ECG tracing, facilitate the work of paramedics, prepare the appropriate section in the hospital for patient before ambulance arrival especially in dangerous situations, to save the human life

and give the patients chance to live through diagnosis the heart condition and it's electrical signal by heart doctors, then they will prepare the best treatment to the patient by analysis the ECG signal.

An ECG is the most commonly, conducted cardiovascular diagnostic procedure and a fundamental tool of clinical practice and first aid. It is indeed considered the "first choice" procedure in the evaluation of patients with chest pain, dizziness, or syncope.

The importance of ECG signal can be expressed from the information that we get through the heart tracing, and these following information can be gained from it:

1. The heart rate .
2. The heart rhythm .
3. Whether there are "conduction abnormalities" (abnormalities in how the electrical impulse spreads across the heart).
4. Whether there has been a prior heart attack .
5. Whether there may be coronary artery disease.
6. Whether the heart muscle has become abnormally thickened.

All of these features are potentially important for giveing the medical officer a quick and easy assessment of the present condition of the heart and also sometimes past damages which have occurred to it. It helps in the differential diagnosis of chest pains and also management and diagnosis of abnormal cardiac rhythms.

On the other hand the important of the project is to open the way for other research to send other information about the status of the patient in the ambulance directly to the Office of Emergency by using the same technology used in this project, and be familiar with this technology .

Finally, from above we described the importance of the project to the humanitarian and scientific research.

1.3 Objectives of the Project:

Our objectives in this project are:

1. To connect The PIC microcontroller with GSM/GPRS module by serial cable.
2. To use the GSM technology in transfer ECG signal.
3. To develop the system for the transfer of data from the base unit to telemedicine unit.

1.4 Literature Review:

Too many projects and scientific papers discussed the idea of telemedicine specially the ECG signal and how to transfer the signal into deferent devices .

For example, development of ECG wireless sensors board for medical healthcare application was done in 2009 .

Other wireless ECG project was done in 2002 in university of Queensland .

Also a mobile device based ECG analysis system , this is a scientific paper for Qiang Fang, Fahim Sufi and Irena Cosic from Rmit university Australia .

And in 2006, Eng . Nadim Shaheen , Syria , invented a device that helps the heart patients to follow up and monitor their health .this device transfers the ECG signal into the communications center . each subscriber patient in this service has a control mechanism and when a patient has a bug then directly the communications center was informed via mobile .

In Dungula,Sudan. There are no sufficient medical staffs and equipments , but in the Sudanese capital Khartoum there are a sufficient medical staffs and equipments, but because the long distance there are so difficulties to help people in Dungula,so the Sudanese government decided in 2007 to do a wireless telemedicine project that allows to benefit from the medical staffs and equipments in Khartoum.

In 2009, the Eng. Mohammad Nadim and Eng. Yaman Kayyal made a wireless telemedicine system but this system depended on the FM modulation in transmission and receiving.

Finally, the idea of ECG wireless system using mobile technology is widely spread, and it grown every day.

1.5 Time Planning:

The project plan follows the time schedule, which includes the related tasks of study and system analysis. The time plan is for the first and second semesters:

Table 1.1: Time planning for first semester

Tasks \ Weeks	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Choose a project idea																
Collect information about the project																
Writing project proposal																
Requirements analysis																
System design																
Documentations																

Table 1.2: Time planning for second semester

Tasks \ Weeks	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Writing project software																
Implementation hardware																
Unit testing																
System testing																
Maintenance and development																
Documentations																
Project delivery																

1.6 Cost Estimations:

Table 1.3: Cost estimation for hardware components

Hardware Component	Required number	Price ($)
PIC Microcontrollers	1	15
ECG monitoring device	1	0
Mobile phones	2	400
PC	1	900
Data SIM cards packages	2	600
Max232	2	25
RS232	2	15
Wires and cables	-	10

Table 1.4: Cost estimation for software components

Software components	Price ($)
Microsoft windows XP professional	199
Microsoft office 2007	300

1.7 Report Contents:

This report consists of a number of chapters. Each discusses a subject related to the project.

Chapter One "**Introduction**" consists of overview, Importance of the Project, Objectives, Literature Review, Time Planning, Cost Estimation and Report Contents.

Chapter Two "**Theoretical Background**" consists of ECG Signal, GSM History, GSM Architecture and Components, GSM Services and Serial Communication Interface.

Chapter Three "**System Design**" consists of System Objectives, General Block-Diagram, System Components and How Does the System Work?.

Chapter Four "**Project Implementation**" consists of Hardware Implementation, Software Implementation and Fixed GSM Architecture.

Chapter Five "**System Testing**" consists of introduction, testing scheduling and testing procedure.

Chapter Six "**Future Work**".

CHAPTER

2

THEORETICAL BACKGROUND

CHAPTER TWO
THORETICAL BACKGROUND

2.1 ECG Signal:

2.1.1 What is meant by ECG?

Electrocardiography (ECG or EKG) is a Tran thoracic interpretation of the electrical activity of the heart over time captured and externally recorded by skin electrodes. It is a noninvasive recording produced by an electrocardiographic device. The etymology of the word is derived from the Greek electro, because it is related to electrical activity, cardio, Greek for heart, and graph, a Greek root meaning "to write".

The ECG works mostly by detecting and amplifying the tiny electrical changes on the skin that are caused when the heart muscle "depolarizes" during each heart beat. At rest, each heart muscle cell has a charge across its outer wall, or cell membrane. Reducing this charge towards zero is called de-polarization, which activates the mechanisms in the cell that cause it to contract. During each heartbeat a healthy heart will have an orderly progression of a wave of depolarization that is triggered by the cells in the senatorial node, spreads out through the atrium, passes through "intrinsic conduction pathways" and then spreads all over the ventricles.

This is detected as tiny rises and falls in the voltage between two electrodes placed either side of the heart which is displayed as a wavy line either on a screen or on paper. This display indicates the overall rhythm of the heart and weaknesses in different parts of the heart muscle. Usually more than 2 electrodes are used and they can be combined into a number of pairs. (For example: Left arm (LA),right arm (RA) and left leg (LL) electrodes form the pairs: LA+RA, LA+LL, RA+LL) The output from each pair is known as a lead. Each lead is said to look at the heart from a different angle. Different types of ECGs can be referred to by the number of leads that are recorded, for example 3-lead, 5-lead or 12-lead ECGs (sometimes simply "a 12-lead"). A 12-lead ECG is one in which 12 different electrical signals are recorded at approximately the same time and will often be used as a one-off recording of an ECG, typically printed out as a paper copy. 3- and 5-lead ECGs tend to be monitored continuously and viewed only on the screen of an appropriate monitoring device, for example during an operation or whilst being transported in an ambulance. There may, or may not be any permanent record of a 3- or 5-lead ECG depending on the equipment used. It is the best way to measure and diagnose abnormal rhythms of the

heart, particularly abnormal rhythms caused by damage to the conductive tissue that carries electrical signals, or abnormal rhythms caused by electrolyte imbalances.

In a myocardial infarction (MI), the ECG can identify if the heart muscle has been damaged in specific areas, though not all areas of the heart are covered. The ECG cannot reliably measure the pumping ability of the heart, for which ultrasound-based (echocardiography) or nuclear medicine tests are used. It is possible to be in cardiac arrest with a normal ECG signal (a condition known as pulse less electrical activity).

The potential created by the heart wall contraction spreads electrical currents from the heart throughout the body. The spreading electrical currents create different potentials at different points on the body. Leads are placed on the body in several pre-determined locations to provide information about heart conditions. The cardiac signal, typically 5 mV peak to peak, is an AC signal with a bandwidth of 0.05 Hz to150 Hz .

2.1.2 ECG Graph Paper:

The output of an ECG recorder is a graph (or sometimes several graphs, representing each of the leads) with time represented on the x-axis and voltage represented on the y-axis. A dedicated ECG machine would usually print onto graph paper which has a background pattern of 1mm squares (often in red or green), with bold divisions every 5mm in both vertical and horizontal directions. It is possible to change the output of most ECG devices but it is standard to represent each mV on the y axis as 1 cm and each second as 25mm on the x-axis (that is a paper speed of 25mm/s). Faster paper speeds can be used - for example to resolve finer detail in the ECG. At a paper speed of 25 mm/s, one small block of ECG paper translates into 40 ms. Five small blocks make up one large block, which translates into 200 ms. Hence, there are five large blocks per second. A calibration signal may be included with a record. A standard signal of 1 mV must move the stylus vertically 1 cm, that is two large squares on ECG paper. The ECG signal is characterized by six peaks and valleys labeled with successive letters of the alphabet P, Q, R, S, and T (Figure 2.1). P wave, a QRS complex, a T wave, and a U wave which is normally visible in 50 to 75% of ECGs. The baseline voltage of the electrocardiogram is known as the isoelectric line. Typically the isoelectric line is measured as the portion of the tracing following the T wave and preceding the next P wave.

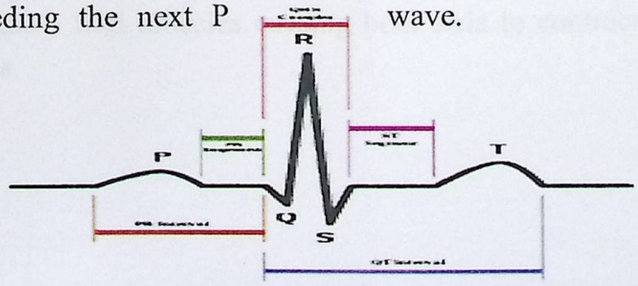


Figure 2.1: Typical ECG waveform

2.1.3 The Activity of the Heart:

The main purpose of the heart is to pump blood throughout the body. The heart is divided into four chambers; the right atrium, right ventricle, left atrium and left ventricle. The right side of the heart delivers deoxygenated (carbonated) blood from the body to the lungs, and the left side of the heart delivers oxygenated blood from the lungs to the body

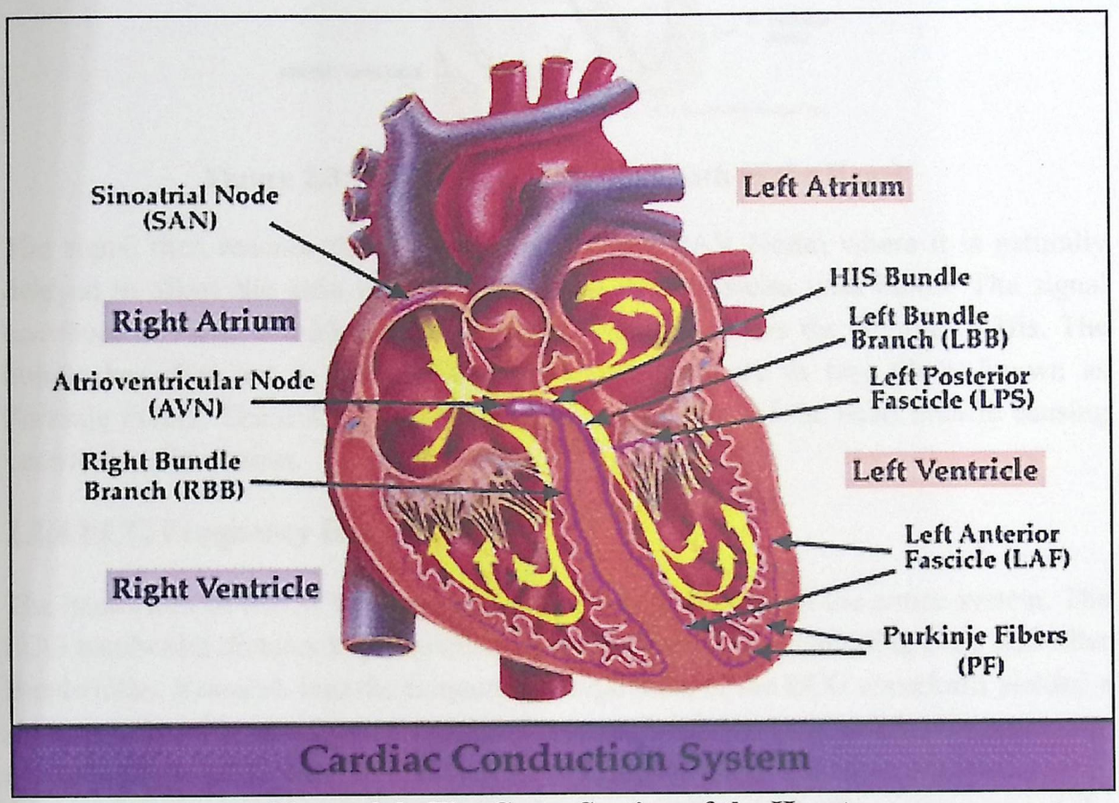


Figure 2.2: The Cross-Section of the Heart

Deoxygenated blood enters the Right Atrium of the heart. The atria contract and push the blood into the Right Ventricle. The ventricles then contract and push the blood out of the heart, and thus to the lungs. The oxygenated blood from the lungs is returned to the Left Atrium. The Atria again contract and push the blood through into the Left Ventricle. The Ventricles again contract and push the blood to all parts of the body. An electrical impulse is necessary to cause the heart to contract. The Sinoatrial Node (SA Node) is responsible for producing these impulses. The impulse from the SA node stimulates the a trial muscles causing both atria to contract and blood to flow into the ventricles.

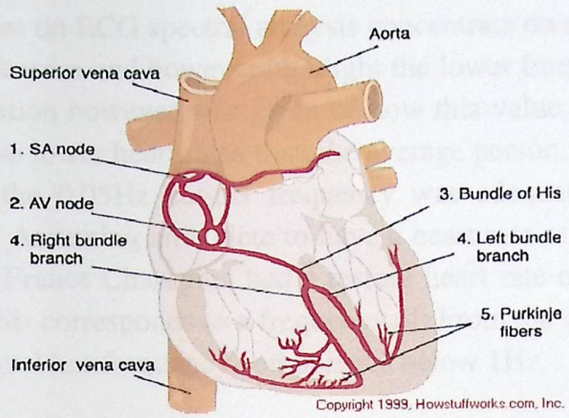


Figure 2.3: Electrical Conduction Path of the Heart

The signal then reaches the Atrioventricular Node (AV Node) where it is naturally delayed to allow the atria to contract and fill the ventricles with blood. The signal continues down to a thick bundle of nerve fibers known as the Bundle of His. The bundle branches out to the left and right and terminate in tiny fibers known as Purkinje Fibers. These distribute the impulse to the cells of the heart muscle causing ventricular stimulation.

2.1.4 ECG Frequency Bandwidth:

The bandwidth of the ECG signal was critical in the Design of the entire system. The ECG bandwidth dictates key implementation aspects such as sampling rates and filter Bandwidths. Research into the frequency components of the ECG waveform yielded a paper published by the Cardiovascular Research Laboratory at NASA on the spectral analysis of the ECG waveform. The paper highlights the frequency components of an ECG signal for healthy adult males aged between 20 and 23. The paper yielded the following information:

- Amplitude information extends only to 200 Hz
- Waveform duration information lies below 60 Hz.

However the paper specified that the data was only valid for healthy males in the specified age group and that the frequency components in children especially, would differ considerably. A second paper labeled 'Minimum Bandwidth Requirements for Recording of Pediatric Electrocardiograms' 9 monitored 200 infants in their study of determining the maximum frequency components of the ECG signal. The study was carried out by passing the raw ECG signal through filters of varying bandwidths while employing a sampling frequency of 1500Hz. The signals were than processed using Matlab. The results of study showed that in 95% of test subjects a 150Hz filter bandwidth was sufficient to adequately represent the ECG. However the optimal filter Bandwidth was selected to be 250Hz (where the filter bandwidth refers to the Low pass filter cut-off frequency).

The majority of studies on ECG spectral analysis concentrate on the higher end of the spectral analysis. Reference and however highlight the lower frequency component to be 0.05Hz. No indication however was given of how this value was obtained. Since Athletes typically have lower heart rates than the average person, a simple calculation was done to see if the 0.05Hz cut-off frequency was adequate in measuring the Athletes ECG signal. Assuming an athlete to have a heart rate of 32beats/min (Lance Armstrong, Tour De France Champion had a resting heart rate of 32beats/min at the peak of his powers) this corresponds to a frequency of: From the above result it can be seen that the ECG signal has frequency components below 1Hz.

2.2 GSM History:

When the acronym GSM was used for the first time in 1982, it stood for Groupe Spéciale Mobile, a committee under the umbrella of Conférence Européenne des Postes et Télécommunications (CEPT), the European standardization organization.

The task of GSM was to define a new standard for mobile communications in the 900 MHz range. It was decided to use digital technology. In the course of time, CEPT evolved into a new organization, the European Telecommunications Standard Institute (ETSI). That, however, did not change the task of GSM. The goal of GSM was to replace the purely national, already overloaded, and thus expensive technologies of the member countries with an international standard.

In 1991, the first GSM systems were ready to be brought into so-called friendly-user operation. The meaning of the acronym GSM was changed that same year to stand for Global System for Mobile Communications. The year

1991 also saw the definition of the first derivative of GSM, the Digital Cellular System 1800 (DCS 1800), which more or less translates the GSM system into the 1800 MHz frequency range.

In the United States, DCS 1800 was adapted to the 1900 MHz band Personal Communication System 1900, or PCS 1900). The next phase, GSM Phase 2, will provide even more end-user features than phase 1 of GSM did. In 1991, only "insiders" believed such a success would be possible because mobile communications could not be considered a mass market in most parts of Europe.

By 1992, many European countries had operational networks, and GSM started to attract interest worldwide. Time has brought substantial technological progress to the GSM hardware. GSM has proved to be a major commercial success for system manufacturers as well as for network operators.

How was such success possible? Particularly today, where Code Division Multiple Access (CDMA), Personal Handy Phone System (PHS), Digital Enhanced Cordless Telecommunications (DECT), and other systems try to mimic the success of GSM, that question comes to mind and is also discussed within the European standardization organizations.

The following factors were major contributors to the success of GSM:

- The liberalization of the monopoly of telecommunications in Europe. during the 1990s and the resulting competition, which consequently lead to lower prices and more "market".
- The knowledge-base and professional approach within the Groupe Spéciale Mobile, together with the active cooperation of the industry.
- The lack of competition: For example, in the United States and Japan, competitive standards for mobile services started being defined only after GSM was already well established.

The future will show which system will prevail as the next generation of mobile communications. ETSI and the Special Mobile Group (SMG), renamed GSM, are currently standardizing the Universal Mobile Telecommunication System (UMTS). Japan is currently improving PHS.

The various satellite communications systems that now push into the market are another, possibly decisive, factor in providing mobile communications on a global basis.

2.3 GSM Architecture and Components:

2.3.1 The System Architecture of GSM: A Network of Cells:

Like all modern mobile networks, GSM utilizes a cellular structure as illustrated in Figure 2.4.

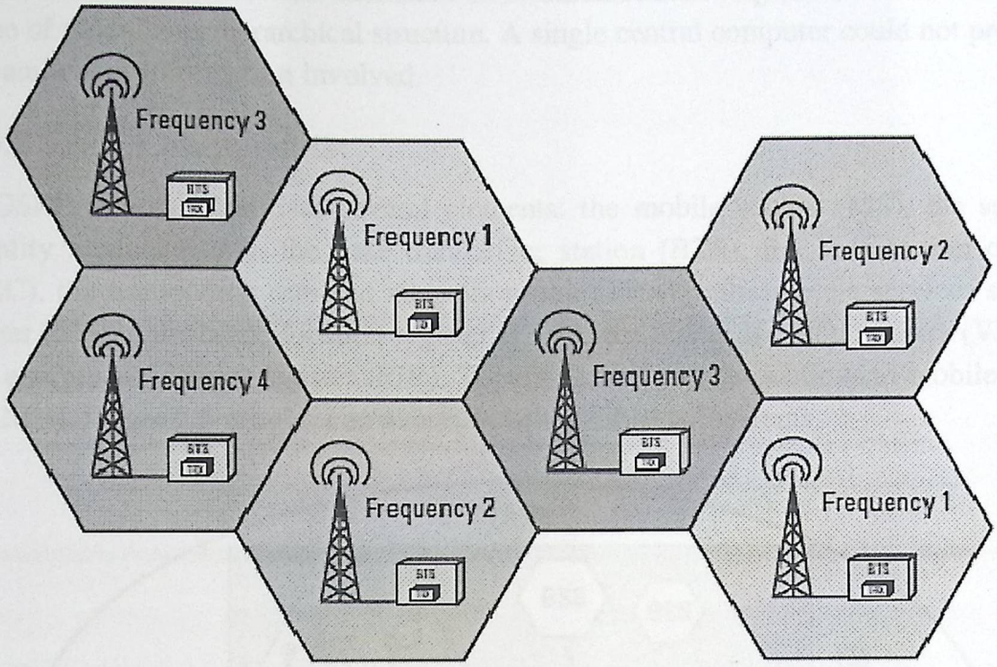


Figure 2.4: The radio coverage of an area by single cell

The basic idea of a cellular network is to partition the available frequency range, to assign only parts of that frequency spectrum to any base transceiver station, and to reduce the range of a base station in order to reuse the scarce frequencies as often as possible. One of the major goals of network planning is to reduce interference between different base stations.

Anyone who starts thinking about possible alternatives should be reminded that current mobile networks operate in frequency ranges where attenuation is substantial. In particular, for mobile stations with low power emission, only small distances (less than 5 km) to a base station are feasible.

Besides the advantage of reusing frequencies, a cellular network also comes with the following disadvantages:

- An increasing number of base stations increases the cost of infrastructure and access lines.
- All cellular networks require that, as the mobile station moves, an active call is handed over from one cell to another, a process known as handover.
- The network has to be kept informed of the approximate location of the mobile station, even without a call in progress, to be able to deliver an incoming call to that mobile station.

The second and third items require extensive communication between the mobile station and the network, as well as between the various network elements. That communication is referred to as signaling and goes far beyond the extent of signaling

that fixed networks use. The extension of communications requires a cellular network to be of modular or hierarchical structure. A single central computer could not process the amount of information involved.

2.3.2 GSM Components:

A GSM network comprises several elements: the mobile station (MS), the subscriber identity module (SIM), the base transceiver station (BTS), the base station controller (BSC), the transcoding rate and adaptation unit (TRAU), the mobile services switching center (MSC), the home location register (HLR), the visitor location register (VLR), and the equipment identity register (EIR). Together, they form a public land mobile network (PLMN). Figure 2.5 provides an overview of the GSM subsystems.

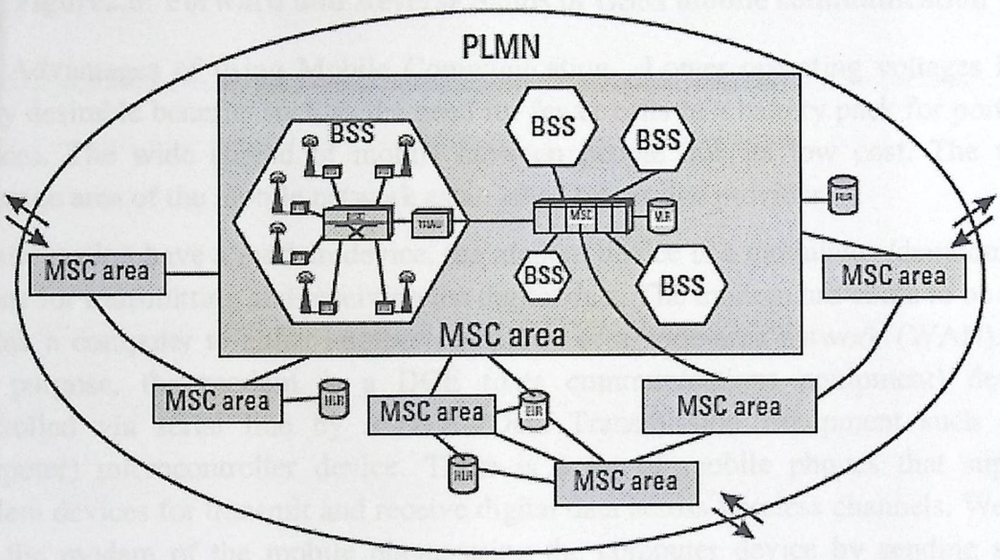


Figure 2.5: The Architecture of a PLMN

2.3.2.1 Mobile Station:

GSM-PLMN contains as many MSs as possible, available in various styles and power classes. In particular, the handheld and portable stations need to be distinguished.

A mobile telephone or cellular telephone is a long-range, portable electronic device used for mobile communication. In addition to the standard voice function of a telephone, current mobile phones can support many additional services such as SMS for text messaging service, email, packet switching for access to the Internet, MMS Multimedia Message Service for sending and receiving photos and videos and data calls. Most current mobile phones connect to a cellular network of base stations (cell sites), which are in turn interconnected to the Public Switched Telephone Network (PSTN). Service Providers employees the Global System for Mobile Communications (GSM) in Palestine, it combines FDMA Frequency Division Multiplexing and TDMA Time Division Multiplexing access schemes and uses two frequency bands around

900 MHz, the first band is dedicated to the reverse link and operates at 890 to 915 MHz and the second band is dedicated to the forward link and operates at 935 to 960 MHz as shown in Figure2.6 , each physical channel has a bandwidth of 200 kHz and consists of 8 time slots, each assigned to an individual user .

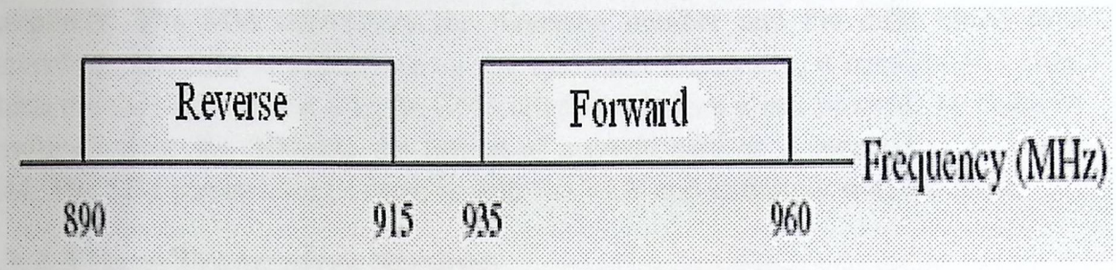


Figure2.6: Forward and Reverse bands of GSM mobile communication

The Advantages of using Mobile Communication , Lower operating voltages have many desirable benefits such as the need for fewer cells in a battery pack for portable devices. The wide spread of mobile between people due its low cost. The wide coverage area of the mobile netwoık established by service provider.

Mobile station have a modem device, the modem device is a modulator /demodulator device for transmitting and receiving the digital data. The modem has come to be used to link a computer to either another computer, or a wide-area network (WAN). For our purpose, the modem is a DCE (data communications equipment) device, controlled via serial line by a DTE (Data Transmission Equipment such as a computer) microcontroller device. There is a lot of mobile phones that support modem devices for transmit and receive digital data across wireless channels. We can test the modem of the mobile phone using the computer device by sending some commands to it and receive the responding from the modem of the mobile. Table 2.1 shows the mobile phones that support for the modem devices and that we can use it for transmit and receive the data.

Table 2.1: Mobile phones types that support modem and data call

Nokia	Sony Ericson	Samsung	Motorola	Alcatel	L G	Siemens
- 5210	- W200i	- A100	- V50	- 1TPro	- 500	- C35
- 6210	- Z520i	- A110	- V66	- 1T700	- 600	- C45
- 6250	- A2628	- A200	- V70	- 1T701		- M35
- 6510	- T28s	- A300	- V100			- ME45
- 7110	- T29	- A400	- V120			- P35
- 8210	- T39m	- N101	- T250			- S25

2.3.2.2 Subscriber Identity Module:

GSM distinguishes between the identity of the subscriber and that of the mobile equipment. The SIM determines the directory number and the calls billed to a subscriber. The SIM is a database on the user side. Physically, it consists of a chip, which the user must insert into the GSM telephone before it can be used. To make its handling easier, the SIM has the format of a credit card or is inserted as a plug-in SIM. The SIM communicates directly with the VLR and indirectly with the HLR.

2.3.2.3 Base Transceiver Station:

A large number of BTSs take care of the radio-related tasks and provide the connectivity between the network and the mobile station via the Air-interface.

2.3.2.4 Base Station Controller :

The BTSs of an area (e.g., the size of a medium-size town) are connected to the BSC via an interface called the Abis-interface. The BSC takes care of all the central functions and the control of the subsystem, referred to as the base station subsystem (BSS). The BSS comprises the BSC itself and the connected BTSs.

2.3.2.5 Transcoding Rate and Adaptation Unit:

One of the most important aspects of a mobile network is the effectiveness with which it uses the available frequency resources. Effectiveness addresses how many calls can be made by using a certain bandwidth, which in turn translates into the necessity to compress data, at least over the Air-interface. In a GSM system, data compression is performed in both the MS and the TRAU. From the architecture perspective, the TRAU is part of the BSS. An appropriate graphical representation of the TRAU is a black box or, more symbolically, a clamp.

2.3.2.6 Mobile Services Switching Center:

A large number of BSCs are connected to the MSC via the A-interface. The MSC is very similar to a regular digital telephone exchange and is accessed by external networks exactly the same way. The major tasks of an MSC are the routing of incoming and outgoing calls and the assignment of user channels on the A-interface.

2.3.2.7 Home Location Register:

The MSC is only one subcenter of a GSM network. Another subcenter is the HLR, a repository that stores the data of a large number of subscribers. An HLR can be regarded as a large database that administers the data of literally hundreds of thousands of subscribers. Every PLMN requires at least one HLR.

2.3.2.8 Visitor Location Register:

The VLR was devised so that the HLR would not be overloaded with inquiries on data about its subscribers. Like the HLR, a VLR contains subscriber data, but only part of the data in the HLR and only while the particular subscriber roams in the area for which the VLR is responsible. When the subscriber moves out of the VLR area, the HLR requests removal of the data related to a subscriber from the VLR. The geographic area of the VLR consists of the total area covered by those BTSs that are related to the MSCs for which the VLR provides its services.

2.3.2.9 Equipment Identity Register:

The theft of GSM mobile telephones seems attractive, since the identities of subscribers and their mobile equipment are separate. Stolen equipment can be reused simply by using any valid SIM. Barring of a subscriber by the operator does not bar the mobile equipment. To prevent that kind of misuse, every GSM terminal equipment contains a unique identifier, the international mobile equipment identity (IMEI). It lies within the realm of responsibilities of a network operator to equip the PLNM with an additional database, the EIR, in which stolen equipment is registered and so can be used to bar fraudulent calls and even, theoretically, to track down a thief (by analyzing the related SIM data).

2.4 GSM Services :

2.4.1 Data Call:

The data call is a service that used to send digital data across a communication channel with baud rate of 9600 kbps. Data call application is a real time application if there is any change in the transmitter the receiver will sense by the same change at the same time. The data call will used to transmit the ECG signal.

With a bearer service the GSM network provides a transmission path between two access points and also a user–network interface.

The network will be responsible to deliver in one network what was received in the other. Interworking attributes may be defined for the support of bearer services over transit networks.

We know that each MSC must have a dedicated GSM Interworking Unit, GIWU, in order to handle a data call. The MSC is always in control of the data call and can execute changes in the resources despite the MS mobility. This is also because no centralized interworking function, IWF, exists in the GSM specification.
Let us take a look at how a data call is performed as shown in Figure 2.7.

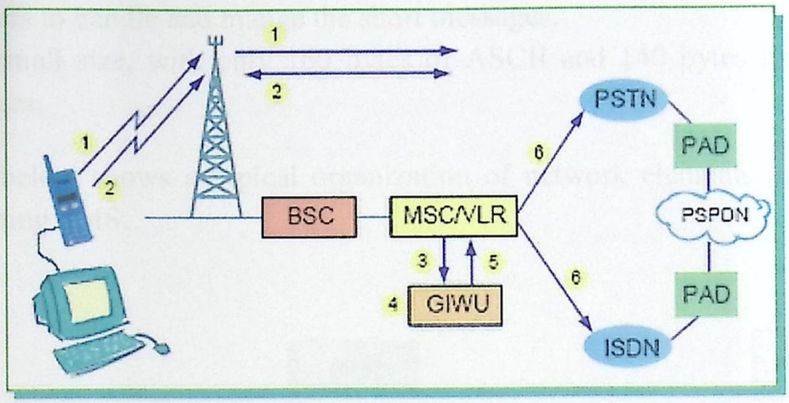


Figure 2.7: Data call architecture

1. MS initiates a data call. In the call setup message the Bearer Capability, BC, is included. The BC tells us which type of bearer service (fax, data) and the transmission rate that is requested.
2. A connection between the MS and the network is set up, as in a normal call, and authentication is performed.
3. MSC analyses the BC, and the B–number and the BC are transferred to the GIWU.
4. GIWU is configured to perform the required service, i.e. rate adaptation Fax or Modem service.
5. GIWU reroutes the call to MSC.
6. MSC routes the call to PSTN or ISDN.

Within the GSM network all connections are circuit switched. This does not, however, prohibit packet services. In order to access a packet switched public data network, PSPDN, a connection to PAD, Packet Assembly Disassembly, is needed. The PAD transforms the bit stream from an asynchronous terminal to data packages.

2.4.2 Short Message Service(SMS):

Abbreviated as SMS, Short Message Service (SMS) is a mobile data service that allows alphanumeric messaging between mobile phones and other equipment such as voice mail systems and email. SMS first appeared in Europe in 1992. It was included in the GSM (Global System for Mobile Communications) standards right at the beginning. Later it was ported to wireless technologies like CDMA and TDMA. The GSM and SMS standards were originally developed by ETSI. ETSI is the abbreviation for European Telecommunications Standards Institute. Now the 3GPP

(Third Generation Partnership Project) is responsible for the development and maintenance of the GSM and SMS standards.
SMS is bidirectional service for sending and receiving short alphanumeric messages. In the real the short massages are not sent directly from sender to receiver, but by SMS center. Each mobile telephone network supports SMS has one or more messaging centers to handle and mange the short messages.
The SMS has small size, with only 160 bytes of ASCII and 140 bytes for binary-encoded messages.

The Figure2.8 below shows a typical organization of network elements in a GSM network supporting SMS.

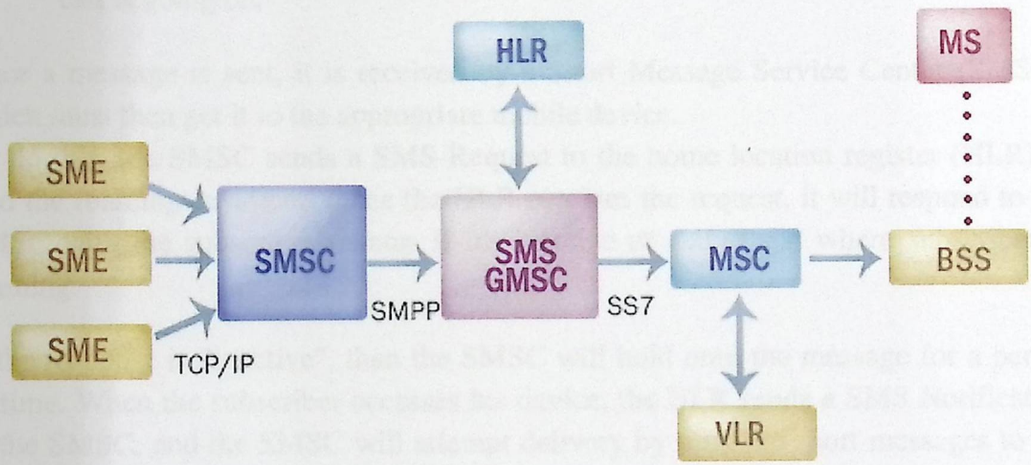


Figure 2.8: SMS architecture

The SMS basic architecture and it's function is :

- The SMC (Short Message Center) is the entity which does the job of store and forward of messages to and from the mobile station. The SME (Short Message Entity) which can be located in the fixed network or a mobile station, receives and sends short messages.
- The SMS GMSC (SMS gateway MSC) is a gateway MSC that can also receive short messages. The gateway MSC is a mobile network's point of contact with other networks. On receiving the short message from the short message center, GMSC uses the SS7 network to interrogate the current position of the mobile station form the HLR, the home location register.
- HLR is the main database in a mobile network. It holds information of the subscription profile of the mobile and also about the routing information for the subscriber, i.e. the area (covered by a MSC) where the mobile is currently situated. The GMSC is thus able to pass on the message to the correct MSC.

- MSC (Mobile Switching Center) is the entity in a GSM network which does the job of switching connections between mobile stations or between mobile stations and the fixed network.
- A VLR (Visitor Location Register) corresponds to each MSC and contains temporary information about the mobile, information like mobile identification and the cell (or a group of cells) where the mobile is currently situated. Using information from the VLR the MSC is able to switch the information (short message) to the corresponding BSS (Base Station System, BSC + BTSs), which transmits the short message to the mobile. The BSS consists of transceivers, which send and receive information over the air interface, to and from the mobile station. This information is passed over the signaling channels so the mobile can receive messages even if a voice or data call is going on.

Once a message is sent, it is received by a Short Message Service Center (SMSC), which must then get it to the appropriate mobile device.
To do this, the SMSC sends a SMS Request to the home location register (HLR) to find the roaming customer. Once the HLR receives the request, it will respond to the SMSC with the subscriber's status if it's inactive or active and where subscriber is roaming.

If the response is "inactive", then the SMSC will hold onto the message for a period of time. When the subscriber accesses his device, the HLR sends a SMS Notification to the SMSC, and the SMSC will attempt delivery by send the short messages to the SMS GMSC.

The SMS GMSC sends the SMS to the MSC (Mobile Switching Centre).Then MSC extracts the receiver information from the VLR (Visitor Location Register) and transfer the SMS to the receiver .
The SMSC receives verification that the message was received by the end user from the MSC, then categorizes the message as "sent" and will not attempt to send it again.

If the SME asks for a confirmation, the SMSC will send back a message for the SME that the message is delivered.

2.5 Serial Communication Interface

2.5.1 Serial communication:

2.5.1.1 Introduction:

In telecommunications and computer science, serial communications is the process of sending data one bit at one time, sequentially, over a communications channel or

computer bus. This is in contrast to parallel communications, where all the bits of each symbol are sent together. Serial communications is used for all long-haul communications and most computer networks, where the cost of cable and synchronization difficulties make parallel communications impractical. Serial computer buses are becoming more common as improved technology enables them to transfer data at higher speeds.

2.5.1.2 Advantages of Using Serial Data Transfer:

1. Serial Cables can be longer than Parallel cables. The serial port transmits a '1' as -3 to -25 volts and a '0' as +3 to +25 volts where as a parallel port transmits a '0' as 0v and a '1' as 5v. Therefore the serial port can have a maximum swing of 50V compared to the parallel port which has a maximum swing of 5 Volts. Therefore cable loss is not going to be a problem for serial cables than they are for parallel.
2. You don't need many wires as in parallel transmission. If your device needs to be mounted a far distance away from the computer then 3 core cable is going to be a lot cheaper that running 19 or 25 core cable. However you must take into account the cost of the interfacing at each end.
3. Many of microcontroller's are built in SCI (Serial Communications Interfaces) which can be used to connect other device to microcontroller's.
4. Serial Communication reduces the number of pin's. Only three pins are commonly used as shown in figure 2.9 , Transmit Data (TXD),Receive Data (RXD) and a reference line for both the input and the output side compared with at least 8 pins if you use a 8 bit Parallel method .

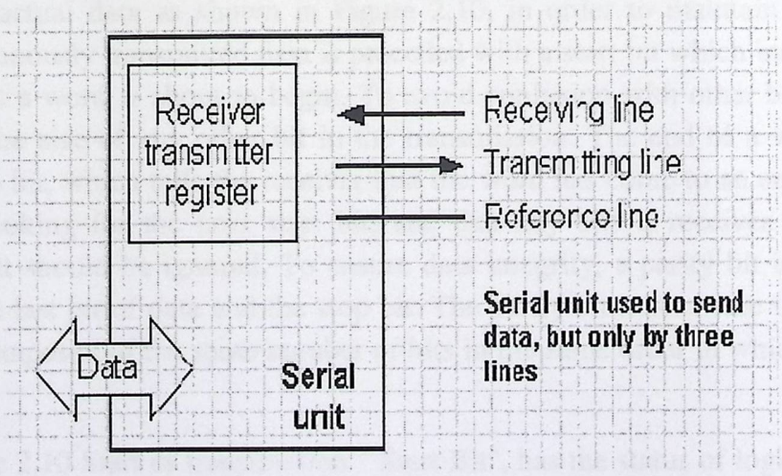


Figure 2.9: Transmitter and receiver for serial unit

2.5.1.3 Synchronous and Asynchronous Serial Transmission:

There are two primary forms of serial transmission, Synchronous and Asynchronous. Depending on the modes that are supported by the hardware, the name of the

communication sub-system will usually include an A if it supports Asynchronous communications, and a S if it supports Synchronous communications. Both forms are described below.

2.5.1.3.1 Synchronous serial transmission:

Synchronous serial transmission requires that the sender and receiver share a clock with one another, or that the sender provide a strobe or other timing signal so that the receiver knows when to "read" the next bit of the data. In most forms of serial Synchronous communication, if there is no data available at a given instant to transmit, a fill character must be sent instead so that data is always being transmitted. Synchronous communication is usually more efficient because only data bits are transmitted between sender and receiver, and synchronous communication can be more costly if extra wiring and circuits are required to share a clock signal between the sender and receiver. A form of Synchronous transmission is used with printers and fixed disk devices in that the data is sent on one set of wires while a clock or strobe is sent on a different wire.

2.5.1.3.2 Asynchronous Serial Transmission:

Most PC serial devices such as mice, keyboards and modems are asynchronous. Asynchronous communication requires nothing more than a transmitter, a receiver and a wire. It is the simplest of serial communication protocols, and the least expensive to implement. As the name implies, asynchronous communication is performed between two (or more) devices which operate on independent clocks.

To solve this timing problem, asynchronous communication requires additional bits to be added around actual data as shown in Figure 2.10, in order to maintain signal integrity. Asynchronously transmitted data is preceded with a start bit which indicates to the receiver that a word is about to begin. To avoid confusion with other bits, the start bit is twice the size of any other bit in the transmission. The end of a word is followed by a stop bit, which tells the receiver that the word has come to an end, that it should begin looking for the next start bit, and that any bits it receives before getting the start bit should be ignored. To ensure data integrity, a parity bit is often added between the last bit of data and the stop bit. The parity bit makes sure that the data received is composed of the same number of bits in the same order in which they were sent.

as shown in Figure 2.10 Start of transmission " Start Bit", has the status of logic zero. The data bits follow the start bit (the first bit is the low significant bit), and after the bits we place the Stop Bit of logic one. The duration of the stop bit 'T' depends on the transmission rate and is adjusted according to the needs of the transmission.

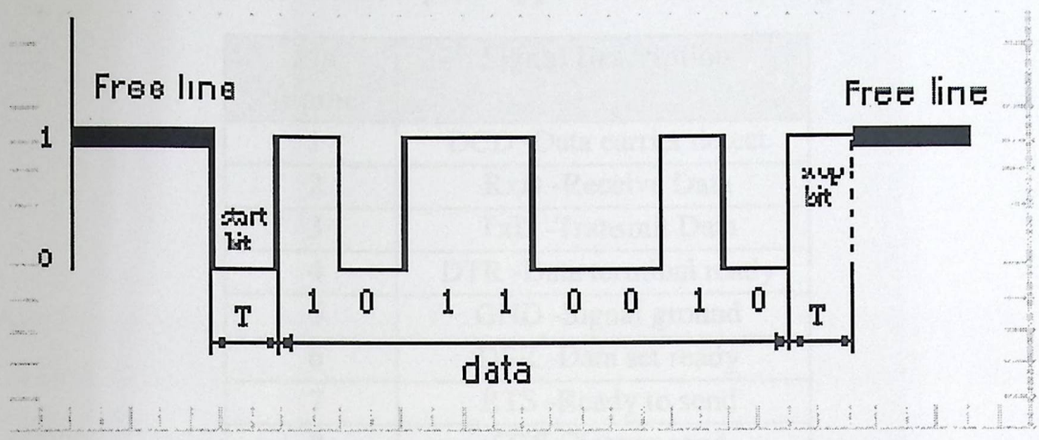


Figure 2.10: Data frame for Asynchronous serial transmission

2.5.2 RS232 :

2.5.2.1 Introduction:

RS-232 (Recommended standard-232) is a standard interface approved by the Electronic Industries Association (EIA) for connecting serial devices. In other words, RS-232 is a long established standard that describes the physical interface and protocol for relatively low-speed serial data communication between computers a related devices.

RS-232 has been around as a standard for decades as an electrical interface between Data Terminal Equipment (DTE) and Data Communications Equipment (DCE) such as modems (DCE) connected to microcontroller (DTE).

RS-232 is the interface that your computer uses to talk to and exchange data with your modem and other serial devices. The serial ports on most computers use a subset of the RS-232C standard.

RS-232 Serial Ports come in two "sizes", There are the D-Type 25 pin connector and the D-Type 9 pin connector both of which are male on the back of the PC, thus you will require a female connector on your device.

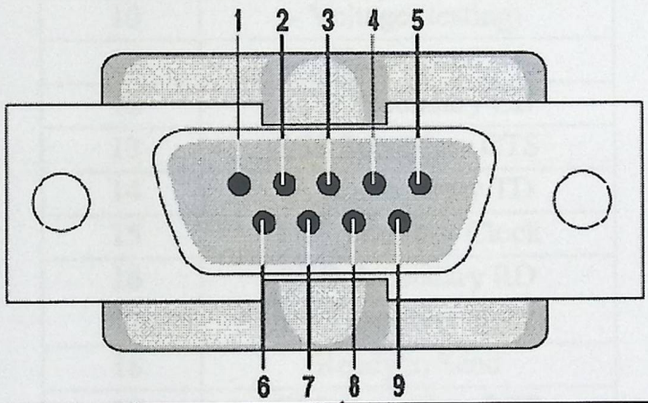
2.5.2.2 RS232 on DB9 (9-pin D-type connector):

There is a standardized pin out for RS-232 on a DB9 connector, as shown in the Table 2.2 below:

Table 2.2: RS232 on 9-pin D-type connector Pin assignment

Pin Number	Signal Description
1	DCD -Data carrier detect
2	RxD -Receive Data
3	TxD -Transmit Data
4	DTR -Data terminal ready
5	GND -Signal ground
6	DSR -Data set ready
7	RTS -Ready to send
8	CTS Clear to send
9	RI Ring Indicator

The pin diagram for RS232 on 9-pin D-type connector is shown in Figure 2.11.



Pin	Signal	Pin	Signal
1	Data Carrier Detect	6	Data Set Ready
2	Received Data	7	Request to Send
3	Transmitted Data	8	Clear to Send
4	Data Terminal Ready	9	Ring Indicator
5	Signal Ground		

Figure 2.11: Pin diagram for RS232 on 9-pin D-type connector

2.5.2.3 RS232 on DB25 (25-pin D-type connector):

In DB-25 connector most of the pins are not needed for normal PC communications, most new PCs are equipped with male D type connectors having only 9 pins. Using a 25-pin DB-25 or 9-pin DB-9 connector, its normal cable limitation of 50 feet can be extended to several hundred feet with high-quality cable.
Standardized pin out for RS-232 on a DB25 connector, as shown in the Table 2.3 below:

Table 2.3: RS232 on 25-pin D-type connector Pin assignment

Pin Number	Signal Description
1	PG - Protective ground
2	TD - Transmitted data
3	RD - Received data
4	RTS - Request to send
5	CTS - Clear to send
6	DSR - Data set ready
7	SG - Signal Ground
8	CD - Carrier detect
9	+ Voltage (testing)
10	- Voltage (testing)
11	Unassigned
12	SCD Secondary CD
13	SCS Secondary CTS
14	STD Secondary TD
15	TC - Transmit Clock
16	SRD Secondary RD
17	RS - Receiver clock
18	Ready to Send
19	SRS Secondary RTS
20	DTR - Data Terminal Ready
21	SQD-Signal Quality Detector
22	RI Ring Indicator
23	DRS - Data rate select
24	XTC - External Clock
25	Unassigned

The pin diagram for RS232 on 25-pin D-type connector is shown in Figure 2.12.

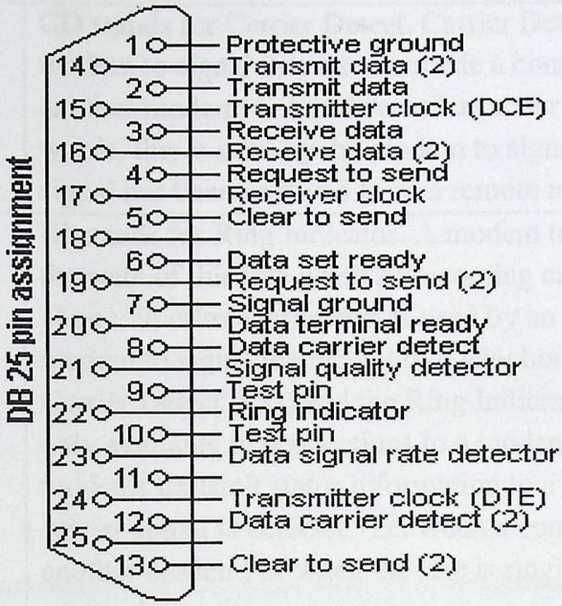


Figure 2.12: Pin diagram for RS232 on 25-pin D-type connector

2.5.2.4 Pin function for RS232:

The pin's signal description and it's function it's shown in the Table 2.4 below:

Table 2.4: Pin's function for RS232

Signal description	Function
TxD	This pin carries data from the computer to the serial device.
RXD	This pin carries data from the serial device to the computer.
DTR signals	DTR is used by the computer to signal that it is ready to communicate with the serial device like modem.
DSR	Similarly to DTR, Data set ready (DSR) is an indication from the Data set that it is ON.
DCD	Data Carrier Detect (DCD) indicates that carrier for the transmit data is ON.
RTS	This pin is used to request clearance to send data to a modem.
CTS	This pin is used by the serial device to acknowledge the computer's RTS Signal. In most situations, RTS and CTS are constantly on throughout the communication session.
Clock signals (TC, RC, and XTC)	The clock signals are only used for synchronous communications. The modem or DSU extracts the clock from the data stream and provides a steady clock signal to the DTE. Note that the transmit and receive clock signals do not have to be the same, or even at the same baud rate.

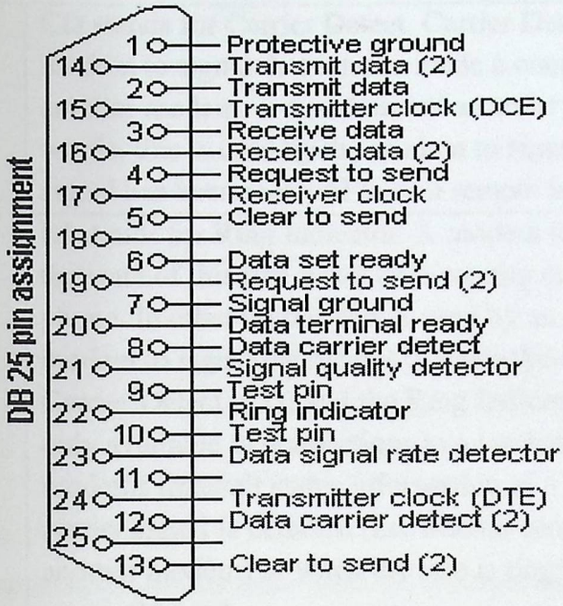


Figure 2.12: Pin diagram for RS232 on 25-pin D-type connector

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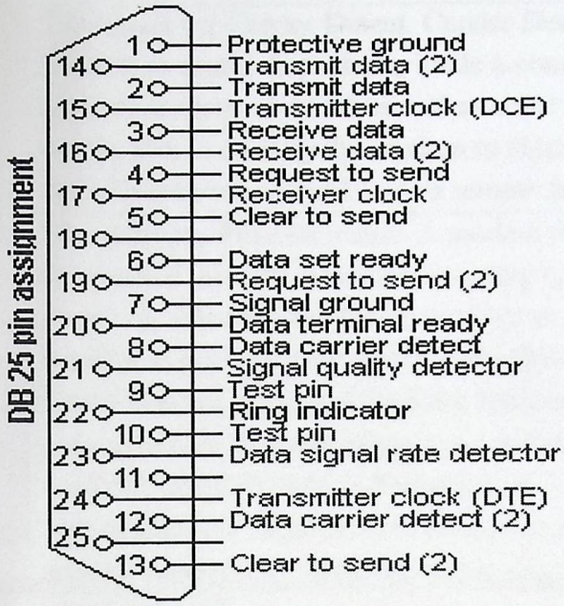

Figure 2.12: Pin diagram for RS232 on 25-pin D-type connector

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CD	CD stands for Carrier Detect. Carrier Detect is used by a modem to signal that it has a made a connection with another modem, or has detected a carrier tone. In other words, this is used by the modem to signal that a carrier signal has been received from a remote modem.
RI	RI stands for Ring Indicator. A modem toggles(keystroke) the state of this line when an incoming call rings your phone. In other words, this is used by an auto answer modem to signal the receipt of a telephone ring signal. The Carrier Detect (CD) and the Ring Indicator (RI) lines are only available in connections to a modem. Because most modems transmit status information to a PC when either a carrier signal is detected (i.e. when a connection is made to another modem) or when the line is ringing, these two lines are rarely used.

2.5.3 Interface between Mobile and Microcontroller:

In order to connect a microcontroller to a serial port on a modem or computer, we need to adjust the level of the signals so communication can take place. The signal level on a PC is +10V for logic zero, and -10V for logic one. Since the signal level on the microcontroller is +5V for logic one and 0V for logic zero, we need an intermediary stage that will convert the levels. One chip specially designed for this task is MAX232. This chip receives signals from +10 to -10V and converts them into 0 and 5V. The circuit for this interface is shown in Figure 2.13.

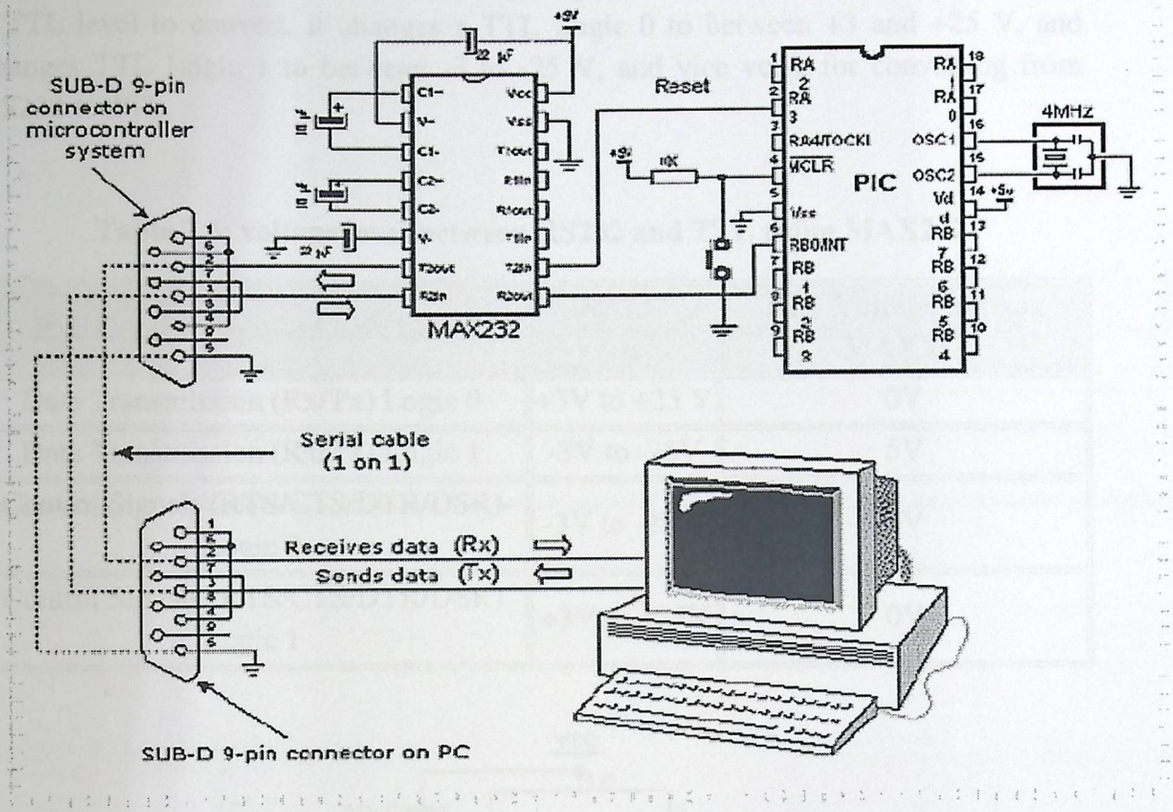


Figure 2.13: Connecting a microcontroller to a PC via a MAX232

2.5.3.1 Introduction of Max 232:

MAX232 is used to interface mobile with microcontroller . The MAX232 is an integrated circuit that converts signals from an RS-232 serial port to signals suitable for use in TTL compatible digital logic circuits. The MAX232 is a dual driver/receiver and typically converts the RX, TX, CTS and RTS signals.

The drivers provide RS-232 voltage level outputs (approx. ± 25 V) from a single + 5 V supply via on-chip charge pumps and external capacitors. This makes it useful for implementing RS-232 in devices that otherwise do not need any voltages outside the 0 V to + 5 V range, as power supply design does not need to be made more complicated just for driving the RS-232 in this case.
The receivers reduce RS-232 inputs (which may be as high as ± 25 V), to standard 5 V TTL levels. These receivers have a typical threshold of 1.3 V, and a typical hysteresis of 0.5 V. The Figure 2.14 shows the circuit of MAX232

In Table 2.5 we show the voltage level between RS232 and TTL using MAX232,it is helpful to understand what occurs to the voltage levels. When a MAX232 IC receives a TTL level to convert, it changes a TTL Logic 0 to between +3 and +25 V, and changes TTL Logic 1 to between -3 to -25 V, and vice versa for converting from RS232 to TTL.

Table 2.5: voltage level between RS232 and TTL using MAX232

RS232 Line Type & Logic Level	RS232 Voltage	TTL Voltage to/from MAX232
Data Transmission (Rx/Tx) Logic 0	+3V to +25 V	0V
Data Transmission (Rx/Tx) Logic 1	-3V to -25V	5V
Control Signals (RTS/CTS/DTR/DSR) Logic 0	-3V to -25 V	5V
Control Signals (RTS/CTS/DTR/DSR) Logic 1	+3V to +25V	0V

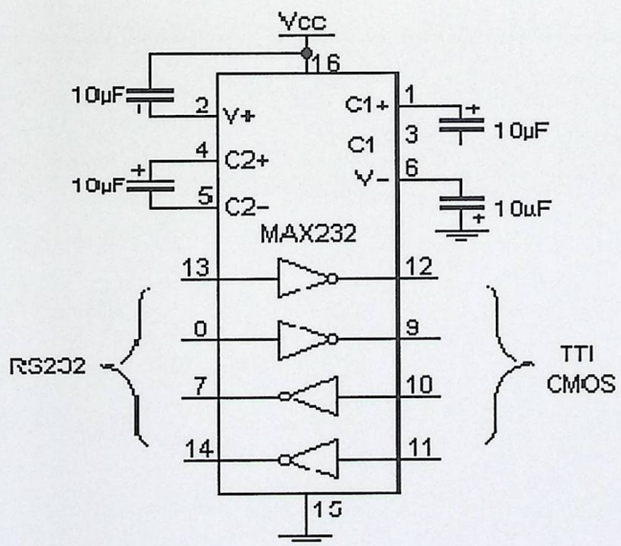


Figure 2.14: MAX232

2.5.3.2 Applications of MAX232:

- Portable Computers .
- Low-Power Modems .
- Interface Translation .
- Battery-Powered RS-232 Systems .
- Multidrop RS-232 Networks .

2.5.3.3 Interfacing Circuit between Microcontroller and Mobile:

Max 232 chip is used to interface mobile with microcontroller as shown in Figure 2.15.

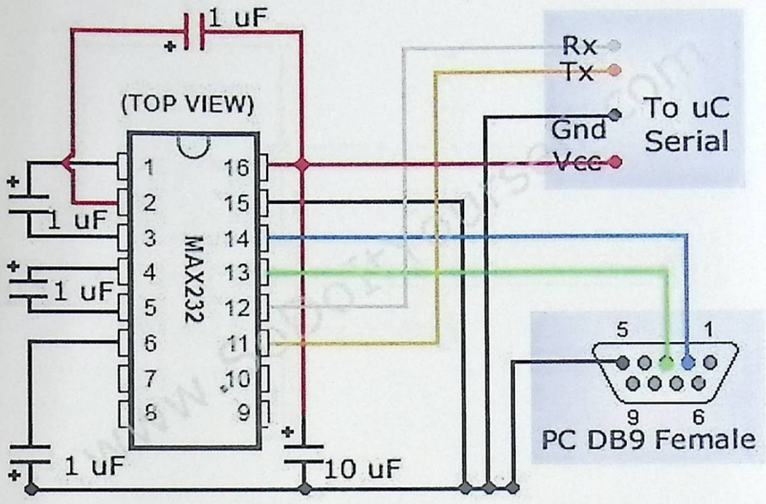


Figure 2.15: Interface circuit

CHAPTER

3

SYSTEM DESIGN

3.1 System Objectives

3.2 General Block-diagram

3.3 System Components

3.4 How does the System Work?

CHAPTER THREE

SYSTEM DESIGN

3.1 System Objectives:

Our objectives in this project are:

- To implement the interface between PIC microcontroller and GSM/GPRS module, by using serial communications .
- To use GSM/GPRS module to receive the data from PIC and to send it by using GSM technology to the base unit .
- To develop the system to transfer data messages from the base unit to telemedicine unit in order to send the proper treatment to the patient.

3.2 General Block-diagram:

The Figure 3.1 illustrates the general block-diagram to the project. It shows two main units in the system: Telemedicine Unit and Base Unit. The Telemedicine Unit position is near the patient ,and it mainly consists of four parts:

- ECG Monitoring Device.
- PIC Microcontroller.
- Serial Communication Interface.
- GSM/GPRS Module.

The Base Unit position is near a doctor in a hospital or anywhere else, it mainly consists of two parts:

- GSM/GPRS Module.
- Personal Computer (PC).

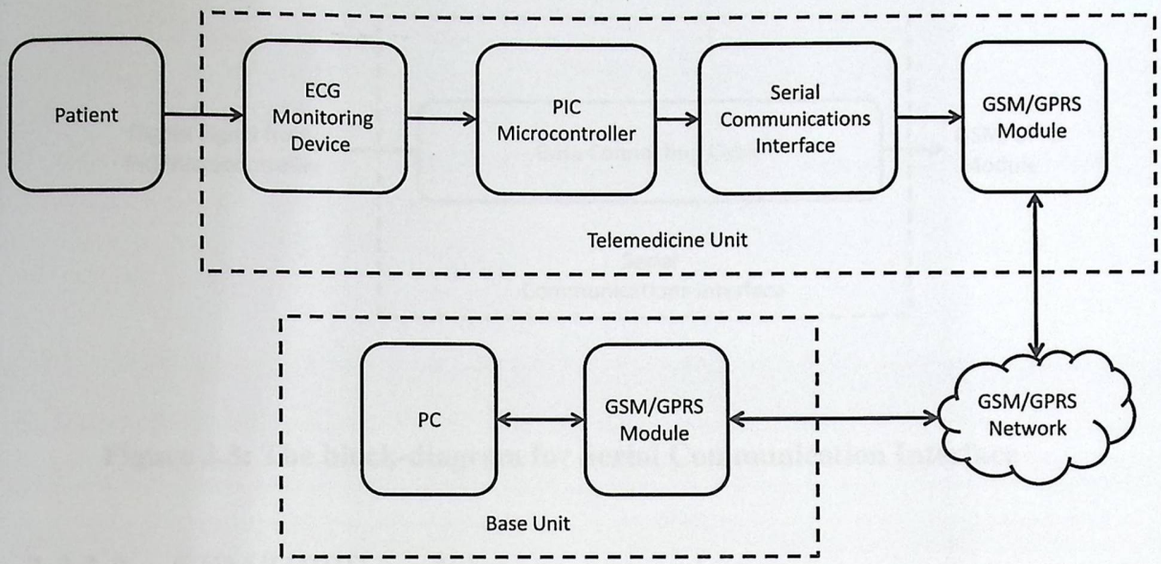


Figure 3.1: The system Block-diagram

3.3 System Components:

3.3.1 Telemedicine Unit:

The Telemedicine Unit is responsible of taking and then processing the ECG signal from a patient. After that, it transfers it to the Base Unit via GSM/GPRS Network, receives and displays the instructions that come from the doctor. From Figure 3.1 the Telemedicine unit consists of:

3.3.1.1 ECG Monitoring Device and PIC Microcontroller:

ECG monitoring device reads measurements of the electrical activity of the patient heart and generates the ECG signal. Then, sends it to PIC Microcontroller, PIC converts the analog signal to digital, and then sends it to serial output. Look at Figure 3.2.

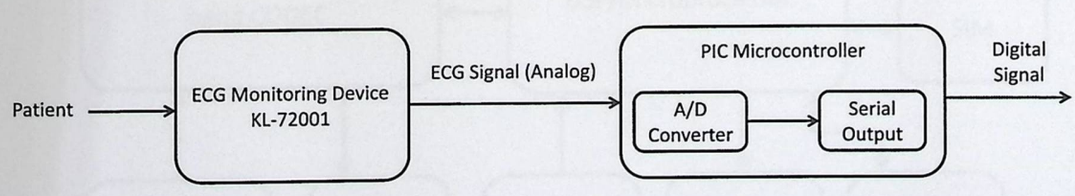


Figure 3.2: ECG Monitoring Device and PIC Microcontroller block-diagram

3.3.1.2 Serial Communication Interface:

Figure 3.3 illustrates the Serial Communication Interface that connects between the PIC microcontroller and GSM modem:

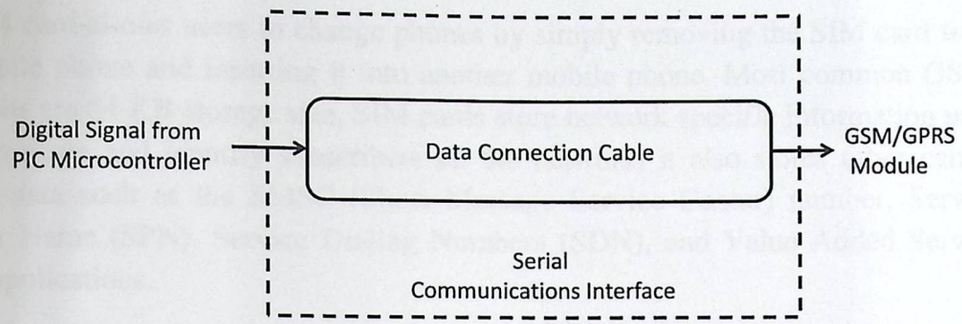


Figure 3.3: The block-diagram for Serial Communication Interface

3.3.1.3 GSM/GPRS module:

The GSM/GPRS module in the Telemedicine Unit receives the data from its serial port, then the DSP/Microprocessor coded the received data (add the destination of the receiver in the Base unit) to be ready to send it over GSM network. Look at Figure 3.4:

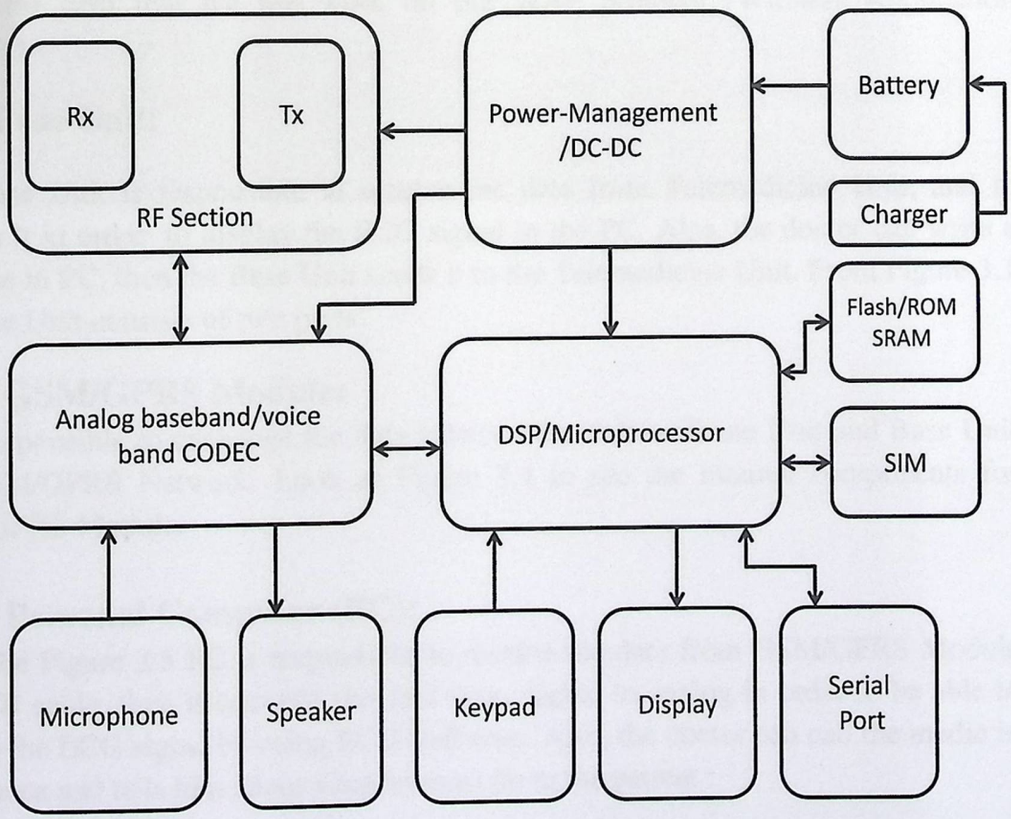


Figure 3.4: The GSM/GPRS module block-diagram

3.3.1.3.1 SIM Card :

A Subscriber Identity Module (SIM) is a removable smart card for mobile phones. SIM cards securely store the service-subscriber key used to identify a mobile phone.

The SIM card allows users to change phones by simply removing the SIM card from one mobile phone and inserting it into another mobile phone. Most common GSM-SIM cards are 64 KB storage size, SIM cards store network specific information used to authenticate and identify subscribers on the network, it also stores other carrier specific data such as the SMSC (Short Message Service Center) number, Service Provider Name (SPN), Service Dialing Numbers (SDN), and Value Added Service (VAS) applications.

There are two types of SIM Card :

a) Voice SIM Card :

Voice SIM card is the SIM card that supports voice communication using the mobile phones.

b) Data SIM Card:

A data SIM is a postpaid SIM card for sending and receiving data. The data SIM can send messages and uses GSM Data services and applications (such as the Desktop SMS solution); also it cannot make phone calls or may support voice call as you like. Data SIM card that we use work on the WAP protocol (Wireless Application Protocol).

3.3.2 Base Unit:

The Base Unit is responsible to receive the data from Telemedicine Unit, and to process it in order to display the ECG signal in the PC. Also, the doctor can write a message in PC, then the Base Unit sends it to the Telemedicine Unit. From Figure 3.1 the Base Unit consists of two parts:

a. GSM/GPRS Module:

It is responsible to exchange the data between the Telemedicine Unit and Base Unit via GSM/GPRS Network. Look at Figure 3.4 to see the internal components for GSM/GPRS Module.

b. Personal Computer (PC):

From the Figure 3.5 PC is responsible to receive the data from GSM/GPRS Module via USB cable, then it converts the data from digital to analog in order to be able to display the ECG signal by using ECG Software. Also, the doctor can call the medic in ambulance and tells him about what he must do to the patient :

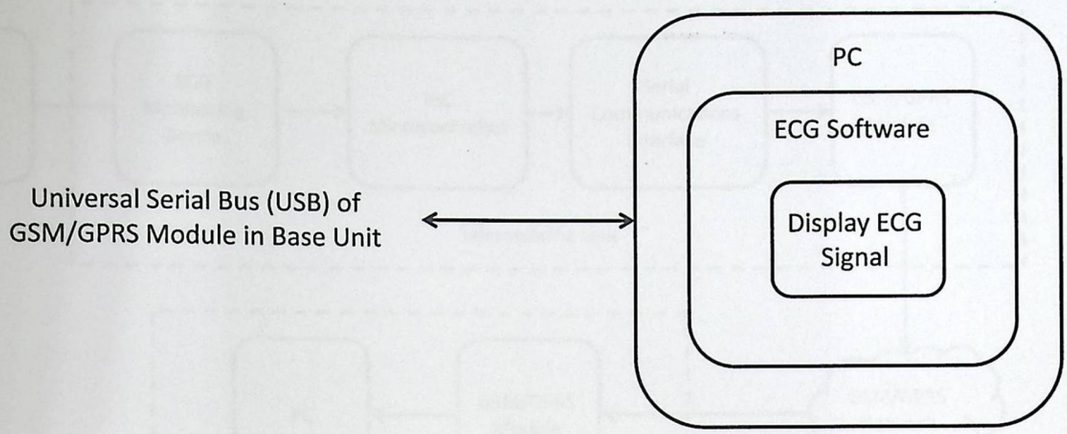


Figure 3.5: The block-diagram for Personal Computer

3.4 How does System Work?

This system is designed to do two main operations, first one is to transfer ECG signal from Telemedicine Unit to Base Unit (forward direction), and the second one is to transfer instructions from Base Unit to Telemedicine Unit (reverse direction).

3.4.1 Transfer ECG Signal:

The system takes the ECG signal by ECG Monitoring Device and sends it to the PIC Microcontroller. PIC Microcontroller converts the signal from analog to digital and transfer it to the GSM/GPRS module via Serial communication Interface. PIC is responsible for the controlling data transmission by GSM/GPRS module via AT command interface. The GSM/GPRS module in Telemedicine Unit sends the data via GSM/GPRS network to the GSM/GPRS module at Base Unit by using data call technology.

GSM/GPRS module at Base Unit receives the data from another GSM/GPRS module and sends it immediately to the personal computer. The personal computer processes and displays the signal by ECG Software. Look for Figure 3.6.

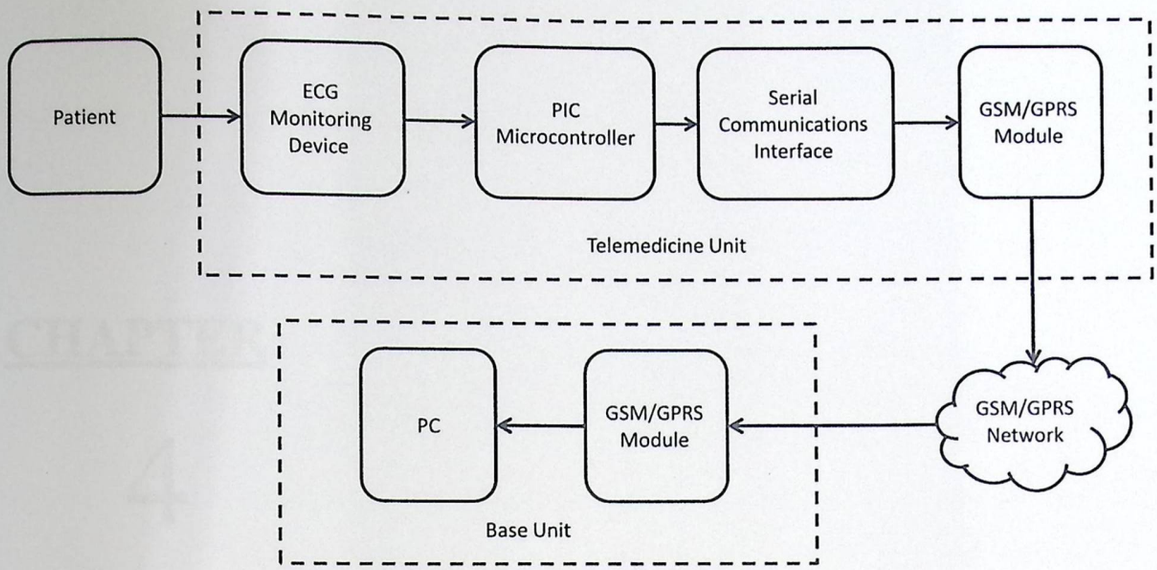


Figure 3.6: General block diagram for the telemedicine and base unit

3.4.2 Transfer Doctor Instructions:

The doctor can use the system to forward prescription for the medic that is near the patient. The doctor calls the medic in the ambulance (telemedicine unit) to tell him about what he must do to the patient.

Look for Figure 3.7:

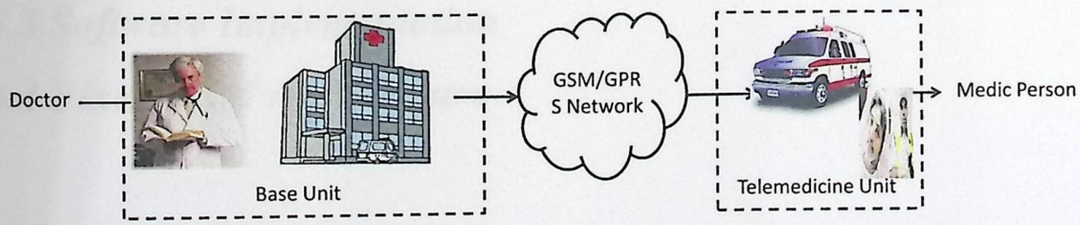


Figure 3.7: call between the doctor in hospital (Base Unit) and the medic in ambulance (Telemedicine Unit)

CHAPTER

4

PROJECT IMPLEMNTATION

CHAPTER FOUR

PROJECT IMPLEMENTATION

4.1 Introduction:

This chapter describes the hardware implementation, software implementation and fixed GSM architecture for our project .In our project we have two main parts as we talked in previous chapter , these parts are the telemedicine unit and the base unit .

Figure 4.1 below shows the general block diagram for the telemedicine and base unit.

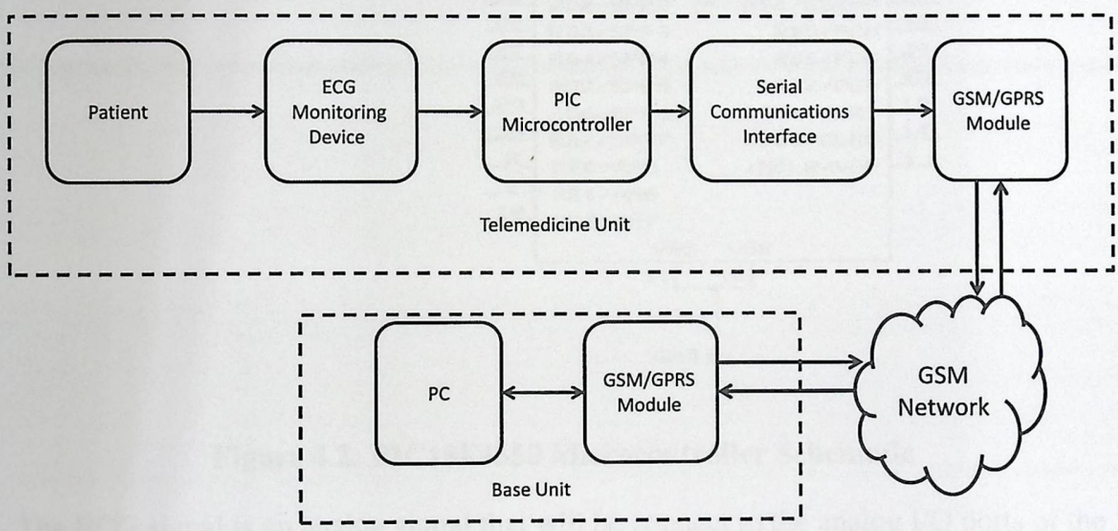


Figure 4.1: General block diagram for the telemedicine and base unit

4.2 Hardware Implementation:

This section converts the general block diagram of the telemedicine and base unit into schematics contain the telemedicine and base unit electrical circuits.

4.2.1 PIC Microcontroller Schematic:

The PIC microcontroller that we want to use it is named by PIC 18F4550 microcontroller with 40 pins .Figure 4.2 shows the schematics circuit for the PIC18F4550 .

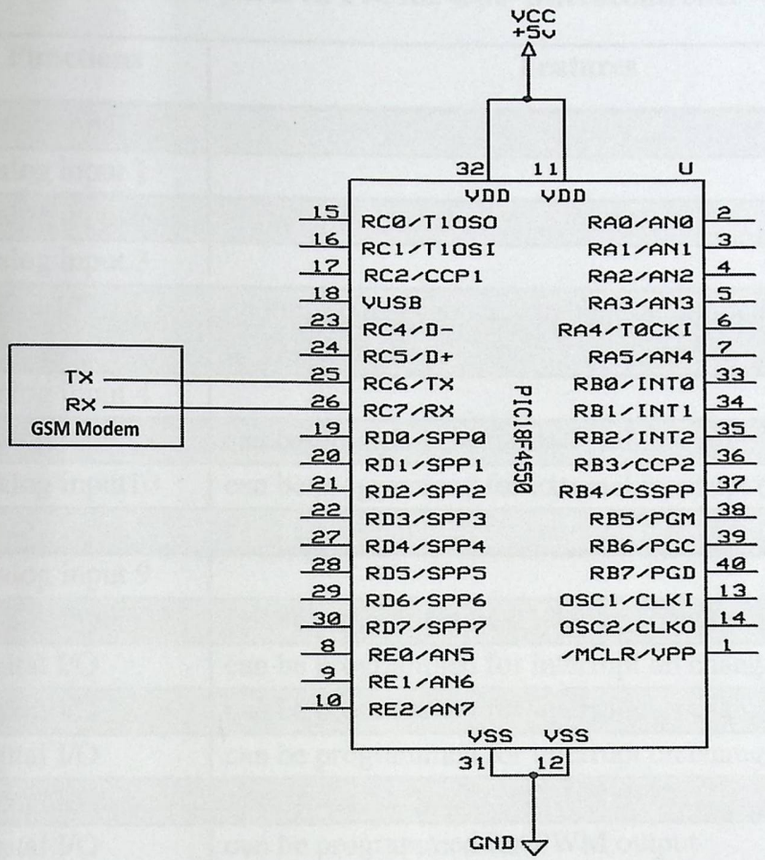


Figure 4.2: PIC18F4550 Microcontroller Schematic

The ECG signal is an analog signal that will be connect to the analog I/O ports of the PIC microcontroller, Table 4.1 shows the summary of I/O ports on PIC18F4550 microcontroller .

Table 4.1: I/O ports on PIC18F4550 Microcontroller

Port	Functions	Features
RA0	Analog input 0	
RA1	Analog input 1	
RA2	Analog input 2	
RA3	Analog input 3	
RA4	Digital I/O	Schmitt Trigger input, can be programmed to be input to TMR0 clock
RA5	Analog input 4	
RB0	Analog input12	can be programmed for external interrupt (INT0)
RB1	Analog input10	can be programmed for external interrupt (INT1)
RB2	Analog input 8	can be programmed for external interrupt (INT2)
RB3	Analog input 9	
RB4	Analog input11	can be programmed for interrupt on change
RB5	Digital I/O	can be programmed for interrupt on change
RB6	Digital I/O	can be programmed for interrupt on change
RB7	Digital I/O	can be programmed for interrupt on change
RC0	Digital I/O	
RC1	Digital I/O	can be programmed for PWM output
RC2	Digital I/O	can be programmed for PWM output
RC6	Digital I/O	can be programmed for UART TX line
RC7	Digital I/O	can be programmed for UART RX line
RD0	Digital I/O	
RD1	Digital I/O	
RD2	Digital I/O	
RD3	Digital I/O	
RD4	Digital I/O	
RD5	Digital I/O	
RD6	Digital I/O	
RD7	Digital I/O	
RE0	Analog input5	
RE1	Analog input6	
RE2	Analog input7	

4.2.2 Serial Adaptor:

Both male serial connectors used to make this adapter cable as shown in Figure 4.3. It is used to give the power to the GSM Modem. Here is the connections:

- Connect pin 2 of male connector on theRS232 –female of PIC side to pin 3 of mobile phone side serial connector and vice versa(test).
- Connect pin 5(ground) of male connector to pin 5 of the phone side serial connector.
- Connect pins 7 and 4 of mobile phone side serial connector to power (+5 Volts).

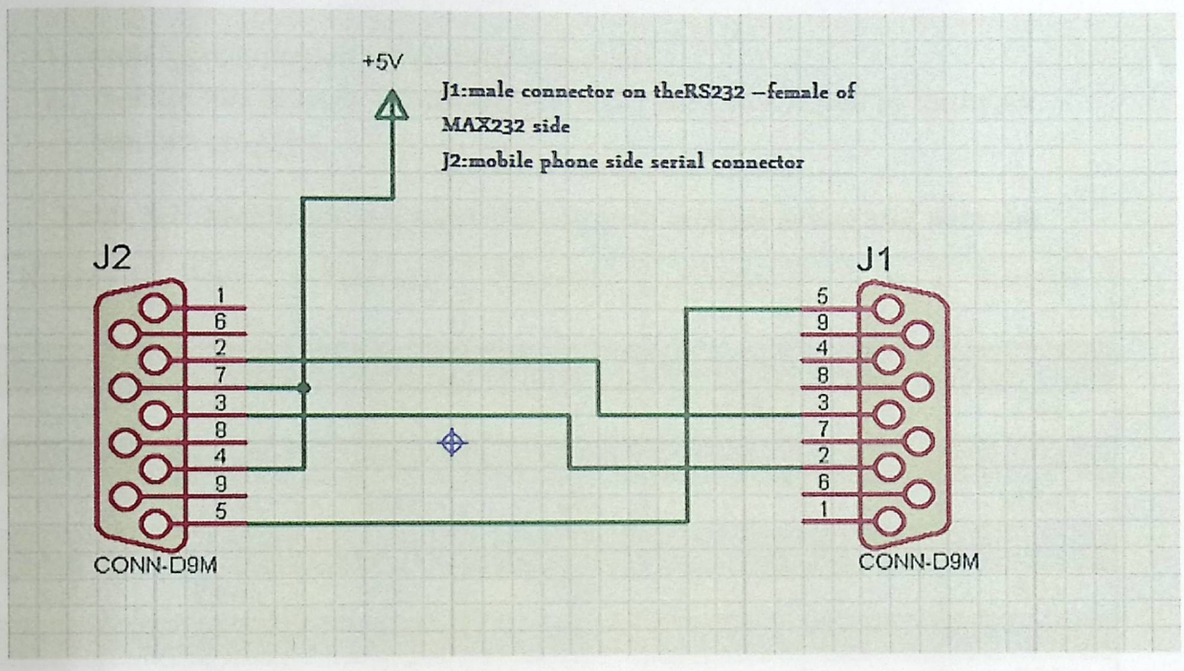


Figure 4.3: Male connection

So the PIC18F4550 with serial interface will be as shown in Figure 4.4:

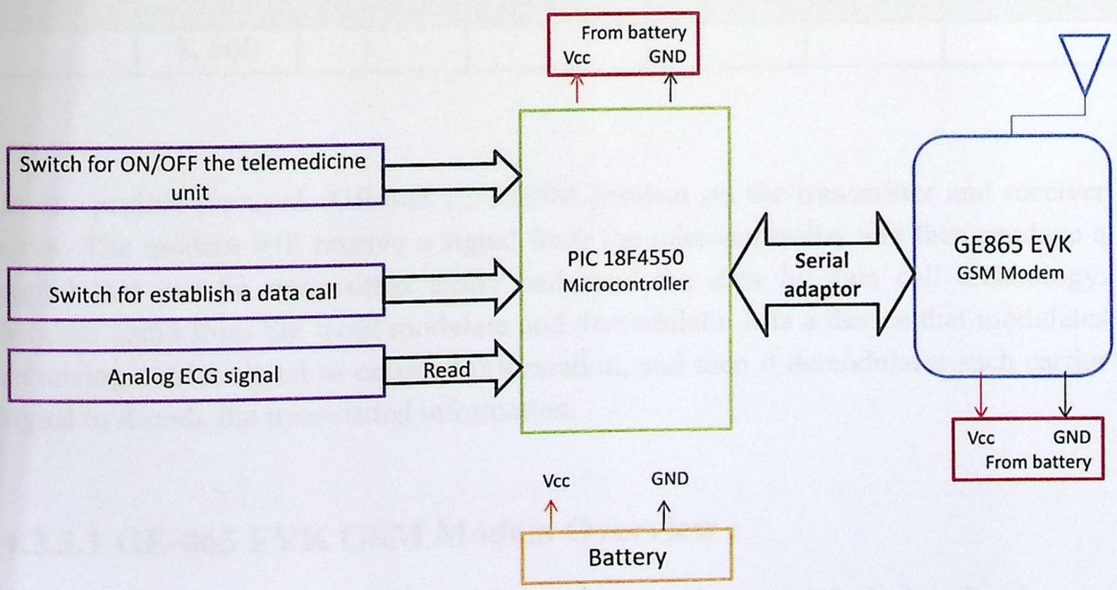


Figure 4.4: PIC18F4550 with serial interface

4.2.3 GSM Modem Side:

There are different types of mobile phones that support modem device, the following Table 4.2 shows the mobile phones that support the modem devices and that we can use it for transmission and receiving the data .

Principles for selecting the mobile phone :

1. mobiles that support serial communications.
2. mobiles that support AT commands and it can be simulated by the hyper terminal program.

Table 4.2: Mobile phones types that support modem device and data call

Nokia	Sony Ericson	Samsung	Motorola	Alcatel	L G	Siemens
- 5210	- W200i	- A100	- V50	- 1TPro	- 500	- C35
- 6210	- Z520i	- A110	- V66	- 1T700	- 600	- C45
- 6250	- A2628	- A200	- V70	- 1T701		- M35
- 6510	- T28s	- A300	- V100			- ME45
- 7110	- T29	- A400	- V120			- P35
- 8210	- T39m	- N101	- T250			- S25
- 8250	- T39	- N188	- T260			- SL25
- 7650	- T66	- N400				- S35
- 8850	- T68m	- Q100				- S40
- 8890	- R280	- R200				- S42
	- R290	- R210				- SL42
	K 300					

In our project we used GE-865 EVKGSM Modem on the transmitter and receiver sides. The modem will receive a signal from the microcontroller and then produce a signal that can be transmitted easily and send the data by data call technology. Modem come from the word modulate and demodulate. It is a device that modulates an analog carrier signal to encoded information, and then it demodulates such carrier signal to decode the transmitted information.

4.2.3.1 GE-865 EVK GSM Modem Overview :

GE-865 EVK GSM Modem is selected in this project because it is designed and developed to provide a low cost that does a many M2M applications like :

- Facility Management.

- Automatic Meter Reading.
- SMS Gateway.
- Mobile Enterprise.
- Data Centre.
- Fire and Security.
- Environmental.
- Traffic Monitoring.

It can always be online the fastest data transmission rates and enable data application and it is not need a large power.

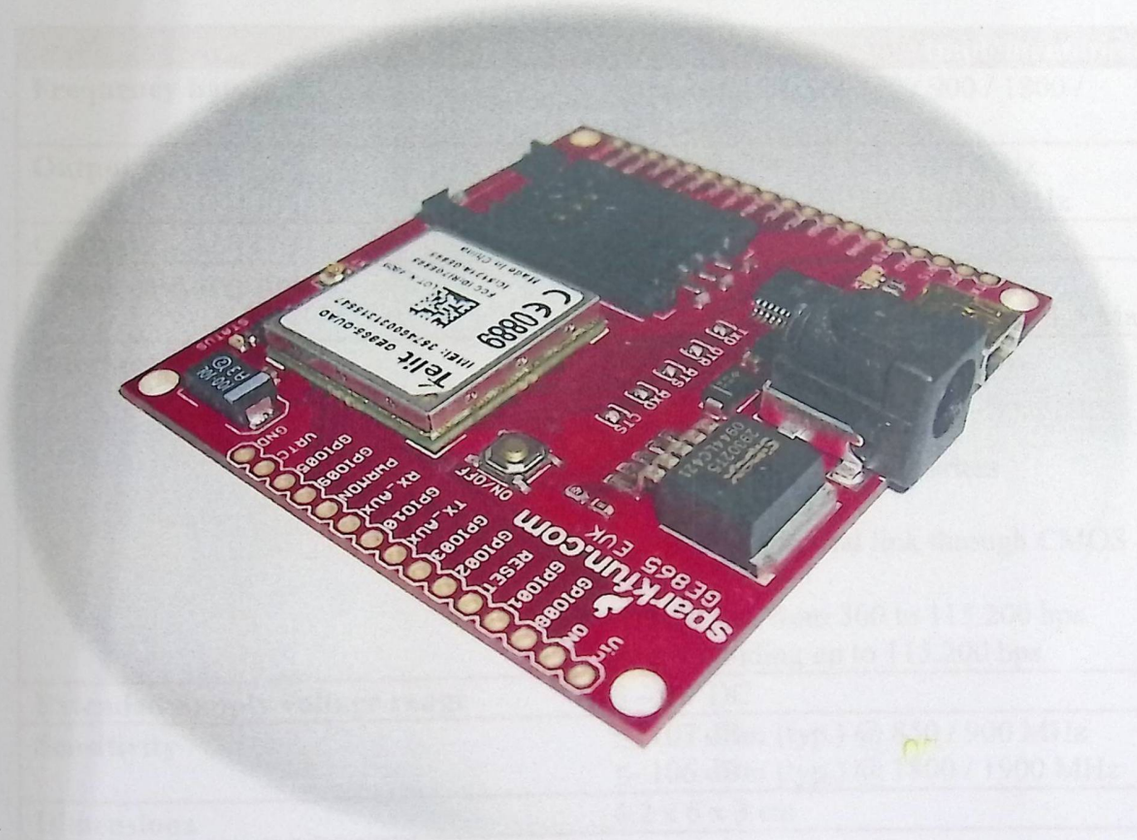


Figure 4.5: overview of GE-865 EVKGSM Modem

The GSM Modem provides the following connectors for power supply, interfacing and antenna figure 4.5:

- 2.1mm DC power connector.
- Serial ports to interface.
- USB port to interface.

- SMA connector for antenna (radio interface).
- SIM Card holder.

The benefits that we will get from GSM Modem:

- Low Cost.
- Reliable and Quality.
- Non proprietary accessories i.e. Standard power adapter and modem cable.
- Compact and nice stylish silver casing.
- Flexible mounting: Rail fixing or side mounting plates.

The features of GSM Modem show in this Table 4.3 :

Table 4.3: Features of GSM Modem

Features	Implementation
Frequency bands	Quad-band EGSM 850 / 900 / 1800 / 1900 MHz
Output power	- Class 4 (2W) @ 850 / 900 MHz - Class 1 (1W) @ 1800 / 1900 MHz
Control	AT commands
Power consumption	- Power off: ‹ 62 uA - Idle (registered, power saving): 1.5 Ma
Interfaces	- 10 I/O ports maximum - Analog audio (balanced) - Digital Voice Interface - 2 A/D plus 1 D/A converters - Buzzer output - ITU-T V.24 serial link through CMOS USART: * Baud rate from 300 to 115.200 bps * Autobauding up to 115.200 bps
Extended Supply voltage range	5 – 9V DC
Sensitivity	≤- 107 dBm (typ.) @ 850 / 900 MHz ≤- 106 dBm (typ.) @ 1800 / 1900 MHz
Dimensions	6.2 x 6 x 3 cm
Weight	76 gram
Extended temperature range	-40°C to +85°C (operational) -40°C to +85°C (storage temperature)
SMS	- Point-to-point mobile originated and mobile terminated SMS - Concatenated SMS supported - SMS cell broadcast - Text and PDU mode - SMS over GPRS
SIM Card	Supported
SMA Antenna connector	Supported

In this project we used the frequency of Jawwal 900 MHz-1900 MHz. also we used data call over GPRS applications.

4.2.3.2 Telit GE865-Quad :

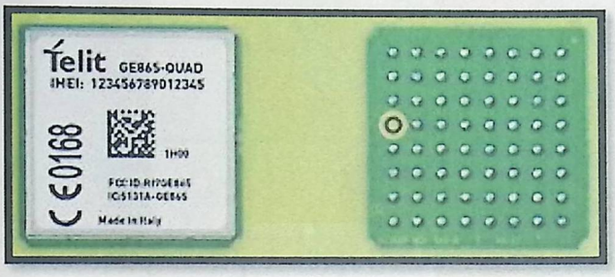


Figure 4.6 Telit GE865-Quad

Figure 4.6shows the Telit GE865-Quad smallest GSM/GPRS modem in worldwide. The Telit is the core of GSM modem that do all process, there are 64 pins in it. Every pin does something shows in Figure 4.7

TOP VIEW

	A	B	C	D	E	F	G	H
1	C105 / RTS	ON_OFF	RESET*	TX_AUX	RX_AUX	VBATT	GND	SERVICE
2	C106/CTS	C107/DSR	GND	GPIO_02 / DVI_RX	PWRMON	VBATT_PA	GPIO_05	VRTC
3	C103_TXD	C108/DTR	-	GPIO_01 / DVI_WA0	GPIO_10	VBATT_PA	GND	GND
4	C104/RXD	C125/RING	-	GPIO_08 / DVI_CLK	GPIO_03 / DVI_TX	GPIO_09	GND	
5	SIMCLK	C109/DCD	-	-	GND	ADC1	GND	ANT
6	SIMIO	-	-	-	-	ADC2	GPIO_07	GND
7	SIMVCC	SIMIN	GND	-	GND	-	DAC	GPIO_04
8	SIMRST	MIC-	MIC-	EAR+	EAR-	-	STATLED	GPIO_06

LEGENDA:

AUDIO	MISCELLANEOUS
SIM CARD	GPIO
ANTENNA	POWER SUPPLY VBATT
UARTS	POWER SUPPLY GND
DAC and ADC	RESERVED

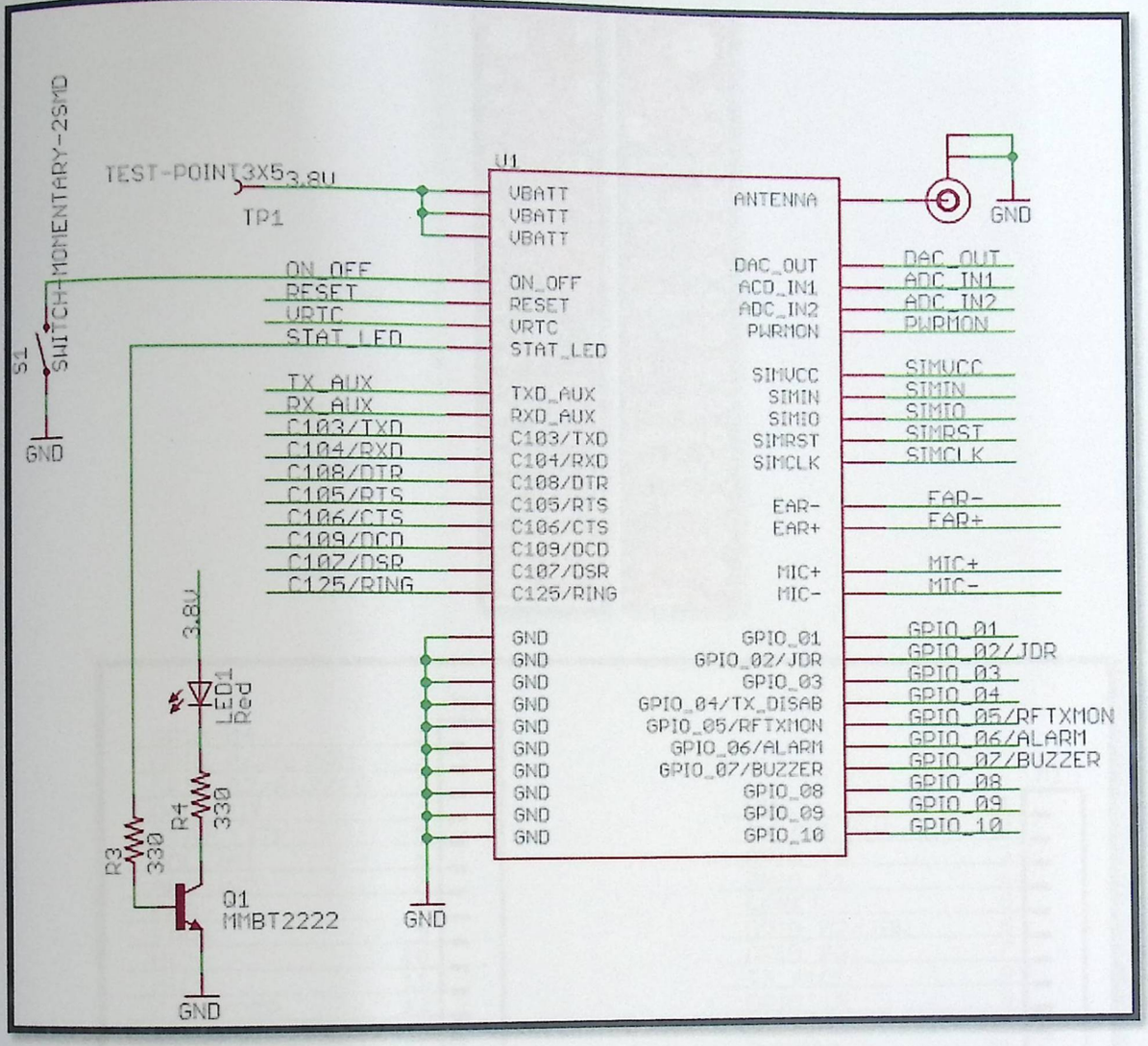


Figure 4.7: Telit GE865-Quad Pins

4.2.3.3 Interfaces :

Via serial interface & USB interface, the host controller controls the GSM Modem and transport data. The Figure 4.8 below shows the pin assignment & circuit design of serial I/O.

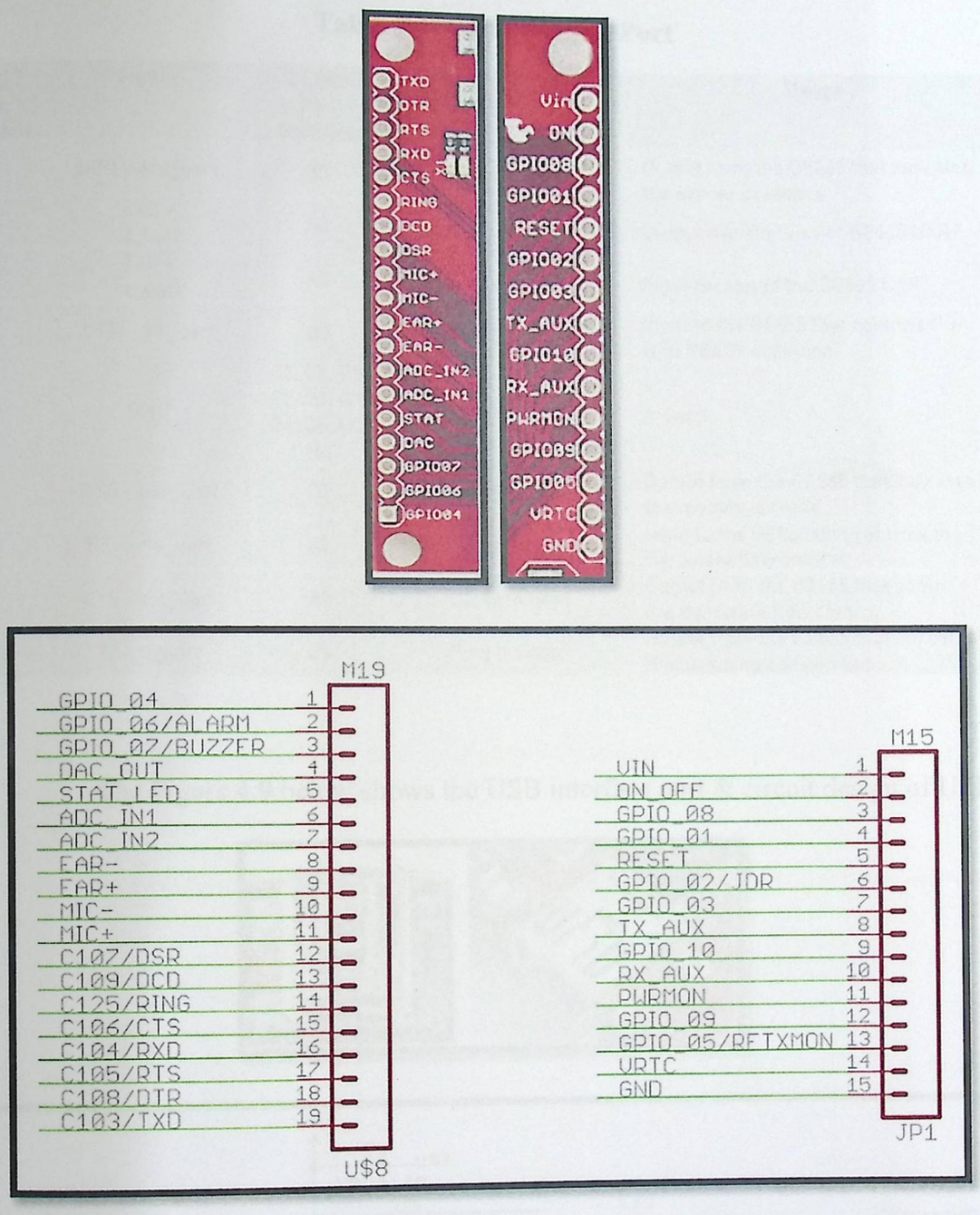


Figure 4.8: Pin assignment

The serial pin that used in the project is RXD and TXD that connect with RX and TX of microcontroller PIC18f4550. The table 4.4explains the serial pins.

Table 4.4: GE865 Serial Port

RS232 Pin Number	Signal	GE865 Pad Number	Name	Usage
1	DCD - dcd_uart	B5	Data Carrier Detect	Output from the GE865 that indicates the carrier presence
2	RXD - tx_uart	A4	Transmit line *see Note	Output transmit line of GE865 UART
3	TXD - rx_uart	A3	Receive line *see Note	Input receive of the GE865 UART
4	DTR - dtr_uart	B3	Data Terminal Ready	Input to the GE865 that controls the DTE READY condition
5	GND	C2, C7, E5, E7, G1, G3, G4, G5, H3, H6	Ground	ground
6	DSR - dsr_uart	B2	Data Set Ready	Output from the GE865 that indicates the module is ready
7	RTS -rts_uart	A1	Request to Send	Input to the GE865 that controls the Hardware flow control
8	CTS - cts_uart	A2	Clear to Send	Output from the GE865 that controls the Hardware flow control
9	RI - ri_uart	B4	Ring Indicator	Output from the GE865 that indicates the incoming call condition

The Figure 4.9 below shows the USB interface port & circuit design of USB:

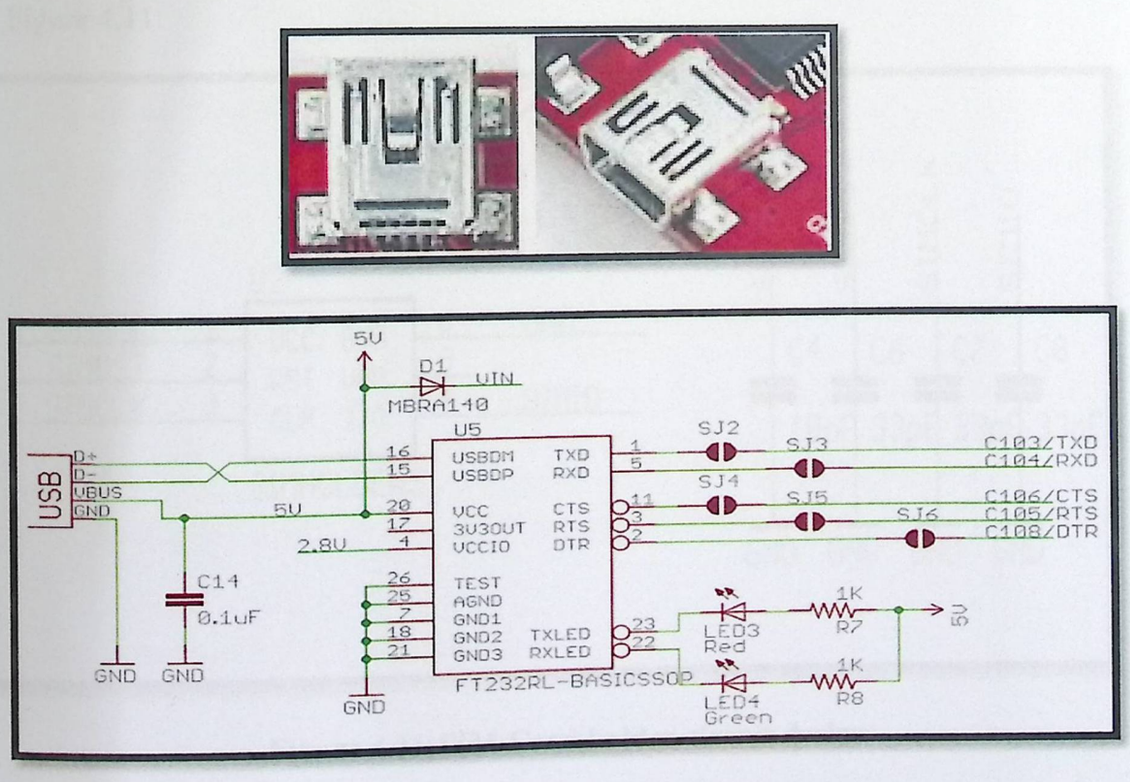


Figure 4.9: USB interface

4.2.3.3.1 SIM Interface :

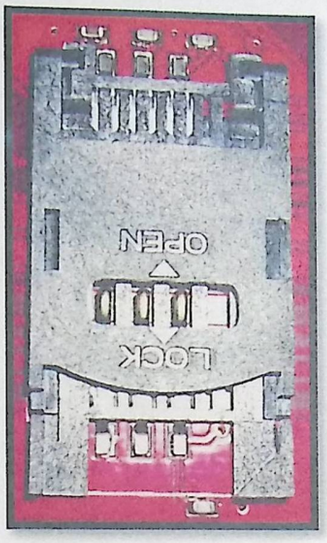


Figure 4.10: SIM Card holder

The SIM interface is where the SIM will be inserting it provides any SIM from any operators show in Figure 4.10 and the circuit design of the SIM Holder show in Figure 4.11:

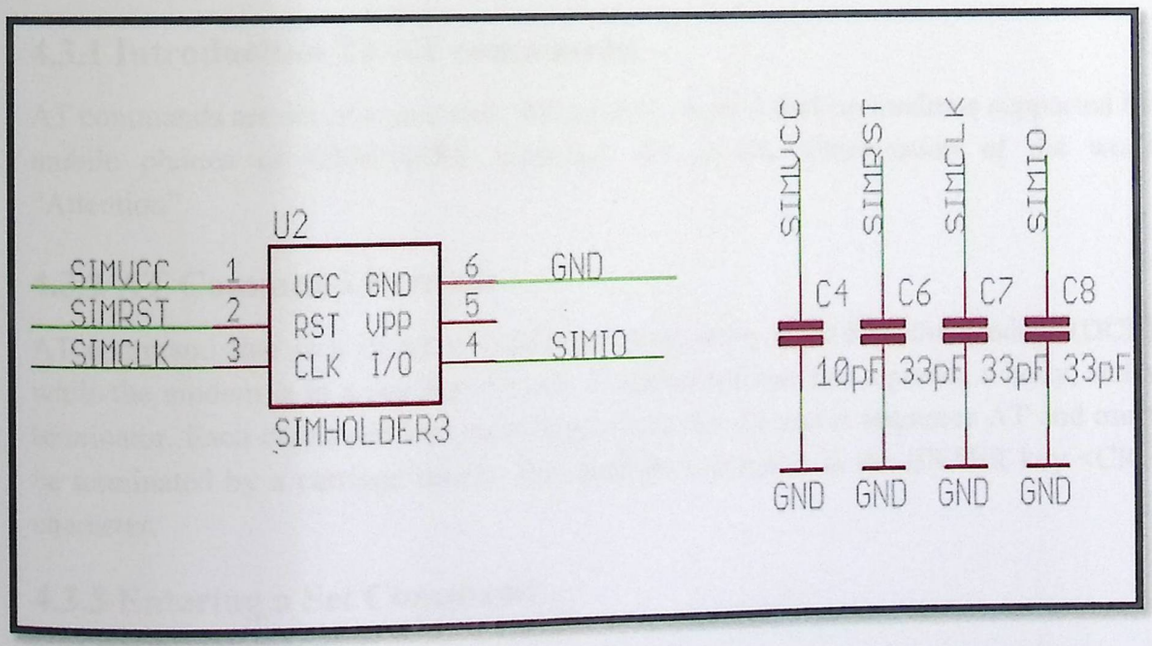


Figure 4.11:SIM Card holder circuit design

4.2.3.3.2 Radio Interface :

An internal RF cable is connected from the antenna reference point to the U.FL (female) connector. To attach the antenna to the GSM Modem, enter the U.FL (male) connector of antenna. Figure 4.12 shows the U.FL-Female connector with male antenna .

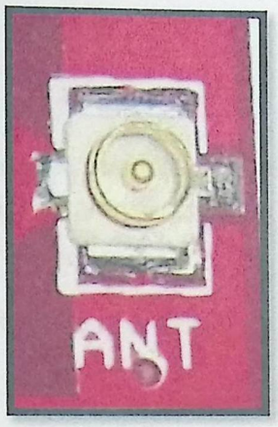


Figure 4.12:U.FL-Female connector

4.3 Software Implementation:

4.3.1 Introduction To AT commands:

AT commands are set of commands that used to control dial-up modems supported by mobile phones or GSM/GPRS modems. AT is the abbreviation of the word "Attention".

4.3.2 AT Command Format:

AT command line is a string of characters sent from a DTE to the modem (DCE) while the modem is in a command state. A command line has a prefix, a body, and a terminator. Each command line must begin with the character sequence AT and must be terminated by a carriage return. The default terminator is the ENTER key <CR> character.

4.3.3 Entering a Set Command:

The standard format for entering a set command is:

AT<command>=<parameters> <CR>

Where:

AT Notifies the modem that a command is being entered.

<Command> the name of the command being entered.

<Parameters> the values to be used by the command.

<CR> All command lines are terminated by pressing the <CR>

(Return or Enter) key.

4.3.4 Basic AT commands Types:

1. Q Command:

Description: Enables or disables the display of result codes. When the result code is disabled, the modem does not issue any final result codes but continues to provide normal text in response to commands.

Set command: Q = [<value>] or Q [<value>]

Options: <value> 0 Enable result codes.

1 Disable result codes.

Default value = 0.

Example: ATQ=1

OK

Read command: Q? Returns the current setting.

Example: ATQ?

Q: 1

OK

Test command: Q=? Always returns (0, 1).

Example: ATQ=?

Q: (0, 1)

OK

2. A (Answer) Command :

Description: Answer and initiate connection to an incoming call.

Execute command: A

Example: ATA

OK

3. H (Hook) control Command :

Description: Terminates a connection.

Execute command: H

Example: ATH

OK

4. D (Dial) Command:

Description: Initiate a phone voice connection (phone number terminated by semicolon). The phone number used to establish the connection will consist of digits and modifiers or a stored number specification.

Execute command: D<n>;

<n> Dial the phone number

; Informs the modem that the number is a voice rather than a fax or data number.

Examples: ATD046193000;

Responses: OK Voice dial

ERROR An unexpected error occurred while trying to establish the connection.

NO DIALTONE The line is busy.

NO CARRIER The mobile phone is not registered

4.3.5 Final result codes from AT commands:

The modem always terminates each response to an AT command with a final result code:

OK means that the command(s) and any specified parameters were valid and the command has complete execution.

ERROR An error has occurred during the command processing. This could arise

Because:

- There is a fault in the command syntax;
- One or more parameters are outside the permitted range.
- The command you issued is not implemented on the modem.
- The command is not appropriate to the service.

Class the modem is operating.

Valid command	AT+CBC=?
Response	+CBC:(0,2),(0-100)
	OK
Invalid command	AT+CBC=?;+FCLASS=3
Response	+CBC:(0,2),(0-100)
	ERROR

4.3.6 Data Call Commands:

4.3.6.1 Introduction

Data call service is one of the most important GPRS applications, data call has become a popular widely because the low cost for sending data, data call feature allows the users to contact a devices (GSM modems) on internet and establish with it a raw data flow over the GPRS and Internet networks.
This feature can be seen as a way to obtain a "virtual" serial connection between the Application Software on the base unit and the telemedicine unit software. This service allow the PIC microcontroller interfaced to the Telit module to send data by data call over GPRS and Internet packets without the need of an internal TCP/IP stack since this function is already embedded inside the module.

4.3.6.2 AT Commands Code For Telemedicine Unit

For design the code of the transmitter side there are set of commands needed for establish data call, the description of these commands as flow :

A. Context parameter setting
   AT+CGDCONT[=<cid>,<PDP_type>,<APN>,<PDP_addr> <cr>
   where:
   <cid> - (PDP Context Identifier) numeric parameter
   which specifies a particular PDP context definition.
   Values:1-6.
   <PDP_type> - (Packet Data Protocol type) a string parameter which specifies the type of packet data protocol.
   Values:
   "IP" - Internet Protocol &PPP" - Point to Point Protocol.
   <APN> - (Access Point Name) a string parameter that represents logical name used to select GGSN or external packet data network.
   <PDP_addr> - a string parameter that identifies the terminal in the address space applicable to the PDP.
B. Request the GPRS context to be activated
   AT#SGACT= <Cntx Id>,<Status>
   where :

- Cntx Id is the context that we want to activate/deactivate.
- Status is the context status (0 means deactivation, 1 activation).

C. Socket Dial

AT#SD = <Conn Id>,<Protocol>, <Remote Port>, <IP address>

Where:

- Conn Id is the connection identifier.
- Protocol is 0 for TCP and 1 for UDP.
- Remote Port is the port of the remote machine.
- IP address is the remote address.

D. close the socket connection.

AT#SH = <conn Id>

where the Conn Id is the connection identifier.

The final code used in the telemedicine unit is shown in table 4.5 and the flow chart of this code is show in Figure4.13.

Table 4.5 Final code used in telemedicine unit

Command	Operation
AT	To define the baud rate between PIC & GSM Modem
AT+CGDCONT=1,IP,static,0.0.0.0	Context parameter setting
AT#SGACT=1,1	Request the GPRS context to be activated
AT#SD=1,0,1080,10.16.2.8	Socket Dial
AT#SH=1	Close the socket connection.

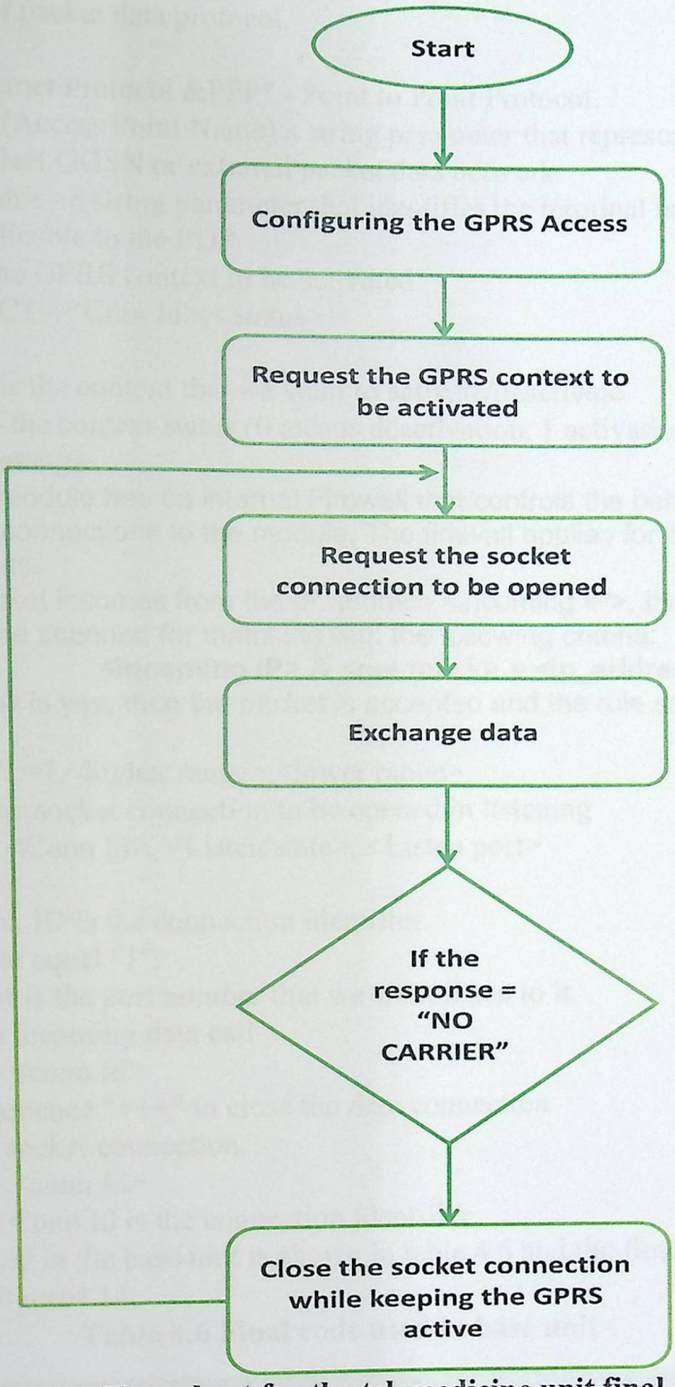


Figure4.13: Flow chart for the telemedicine unit final code.

4.3.6.3 AT Commands Code For Base Unit:

For design the code of the receiver side there are set of commands needed for listening accept data call, the description of these commands as flow :

A. Context parameter setting
   AT+CGDCONT[=<cid>,<PDP_type>,<APN>,<PDP_addr> <cr>
   where:
   <cid> - (PDP Context Identifier) numeric parameter
   which specifies a particular PDP context definition.
   Values:1-6.
   <PDP_type> - (Packet Data Protocol type) a string parameter which specifies

the type of packet data protocol.
Values:
"IP" - Internet Protocol &PPP" - Point to Point Protocol.
<APN> - (Access Point Name) a string parameter that represents logical name used to select GGSN or external packet data network.
<PDP_addr> - a string parameter that identifies the terminal in the address space applicable to the PDP.

B. Request the GPRS context to be activated
AT#SGACT= <Cntx Id>,<Status>
where :
• Cntx Id is the context that we want to activate/deactivate.
• Status is the context status (0 means deactivation, 1 activation).

C. Firewall settings
The Telit module has an internal Firewall that controls the behavior of the incoming connections to the module. The firewall applies for listening connections.
When packet incomes from the IP address <incoming IP>, the firewall chain rules will be scanned for matching with the following criteria:
<incoming IP> & <net mask> = <ip_address>
If the result is yes, then the packet is accepted and the rule scan is finished

AT#FRWL=1,<higher range>,<lower range>

D. Request the socket connection to be opened in listening
AT#SL = <Conn Id>, <Listen state>, <Listen port>
where :
Connection ID is the connection identifier.
Listen state equal "1".
Listen port is the port number that we want listen to it.

E. Accept an incoming data call
AT#SA = <conn Id>

F. Escape sequence "+++" to close the data connection

G. Close the socket connection.
AT#SH = <conn Id>
where the Conn Id is the connection identifier.

The final code used in the base unit is shown in table 4.6 and the flow chart of this code is show in Figure4.14.

Table 4.6 Final code used in base unit

Command	Operation
AT	To define the baud rate between PC & GSM Modem
AT+CGDCONT=1,IP,static,0.0.0.0	Context parameter setting
AT#SGACT=1,1	Request the GPRS context to be activated
AT#FRWL=1,255.255.255.255,0.0.0.0	Firewall settings
AT#SL=1,1,1080	Request the socket connection to be opened in listening
AT#SA =1	Accept an incoming data call
Escape sequence "+++"	close the data connection
AT#SH=1	Close the socket connection.

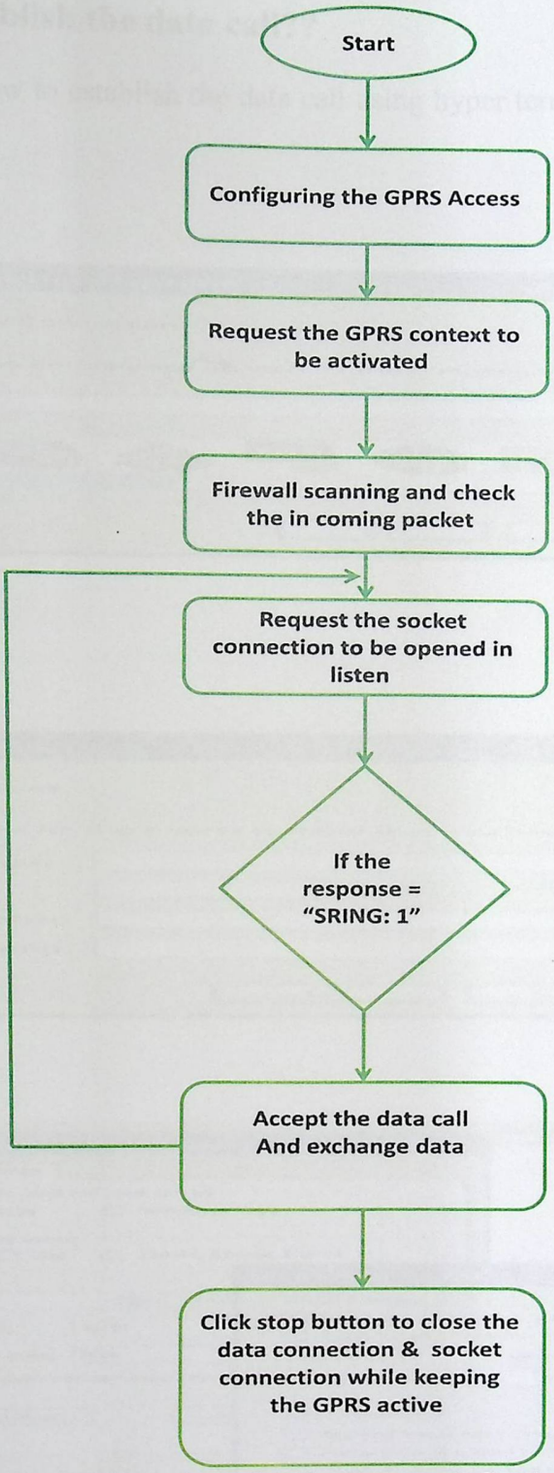


Figure4.14: Flow chart for the base unit final code.

4.3.7 Simulation Using Hyper Terminal:

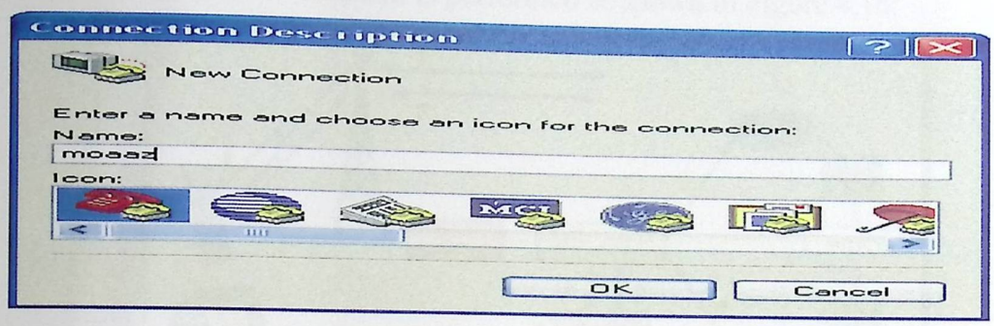
Hyper terminal program is the program that supported by the operating system "OS"

In the XP Operating system you can simulate the usage of the AT commands with the mobile modem. To open the program from>> start menu >> all programs >> accessories >> communication >> hyper terminal. After that choose the name for the connection and identify the com port then choose default setting then connect.

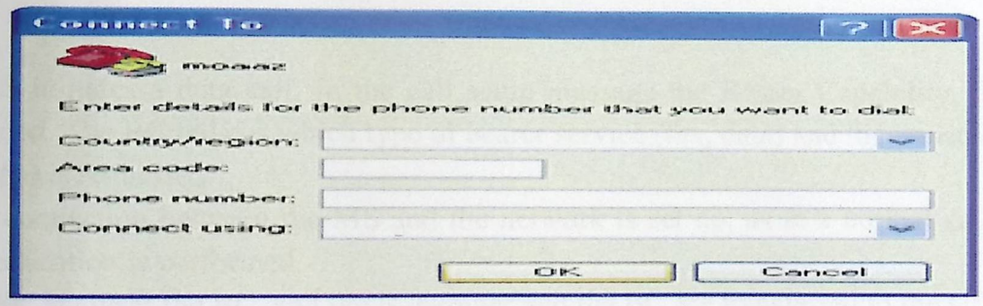
1-How does establish the data call??

Figure 4.15 shows how to establish the data call using hyper terminal communication in windows XP:

a)



b)



c)

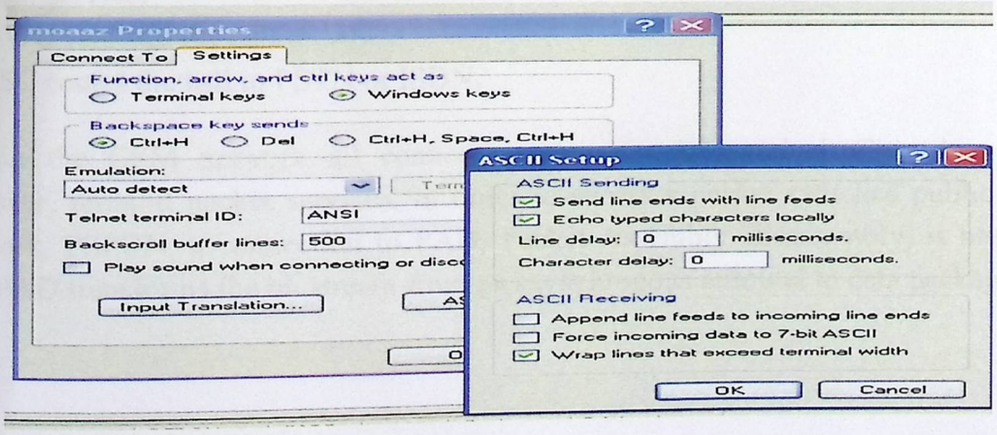


Figure 4.15 (a, b, c): Settings for establish the data call on hyper terminal

4.4 Fixed GSM Architecture:

4.4.1 The Process Of Data Call Service in GSM Network:

Let us take a look at how a data call is performed as shown in Figure 4.16:

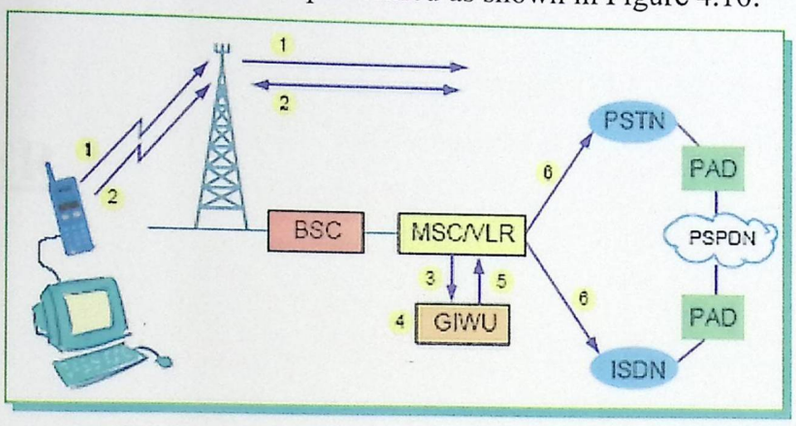


Figure 4.16: Data call architecture

1. MS initiates a data call. In the call setup message the Bearer Capability, BC, is included. The BC tells us which type of bearer service (fax, data) and the transmission rate that is requested.
2. A connection between the MS and the network is set up, as in a normal call, and authentication is performed.
3. MSC analyses the BC, and the B–number and the BC are transferred to the GIWU.
4. GIWU is configured to perform the required service, i.e. rate adaptation Fax or Modem service.
5. GIWU reroutes the call to MSC.
6. MSC routes the call to PSTN or ISDN.

Within the GSM network all connections are circuit switched. This does not, however, prohibit packet services. In order to access a packet switched public data network, PSPDN, a connection to PAD, Packet Assembly Disassembly, is needed. The PAD transforms the bit stream from an asynchronous terminal to data packages.

CHAPTER

5

SYSTEM TESTING

CHAPTER FIVE

SYSTEM TESTING

5.1 Introduction

This chapter covers the testing of the hardware and software of PIC18f4550 and GSM Modem. The purpose of interfacing PIC microcontroller with GSM modem is to send the AT commands by PIC microcontroller to the GSM modem in the telemedicine unit, this commands used for establish data call between the GSM modem on the telemedicine unit and the other GSM modem on the base unit, the other purpose of this interfacing is to send the samples of A\D converter from PIC microcontroller to the PC side over GSM network by using the data channel which is established between the two GSM modems . The testing performed in this section is done to verify each function of the system.

5.2 Testing Scheduling

Table 5.1 Testing Scheduling

Testing Process \ Weeks	21	22	23	24	25	26	27	28	29	30	31	32
Unit Testing	■	■	■	■	■							
Sub-System Testing					■	■	■					
System Testing						■	■	■	■	■	■	■
Acceptance Testing											■	■

5.3 Testing Procedure

5.3.1 Unit Testing

To implement such testing, each unit must be tested, so each task of the project would be tested individually. The GSM Modems , PIC microcontroller and Switches was

tested alone. Additionally, the connecting cables and all the pins were tested. The software code also were tested by using hyper terminal program .

Finally, all parts tested individually and it's work probably and no problem with any part .

5.3.2 Sub-System Testing

The main aim of testing parts is to test the main operations of each sub systems and to ensure it is working properly. There are three operation in the system. The first one is interfacing the GSM Modem with PIC microcontroller and exchanging data between them. The second operation is sending data from the GSM Modem in the telemedicine unit to the GSM Modem in the base unit. The latest one is interfacing the GSM Modem with PC in the base unit side.

1. **First operation test**
   the first operation is interfacing the GSM Modem with PIC microcontroller, we make this test by four step as follows:
   - **A.** The first step : connect one side of max232 to the transmitter and receiver of the PIC microcontroller pins (pin 26 is RX and pin is 25 TX) and the other side to the com port of the PC.
   - **B.** The second step : connect the GSM Modem to PC using USB Port.
   - **C.** The third step : open hyper terminal program on each PC, setup the COM Port number and the speed of Baud Rate were selected to 9600 bps.
   - **D.** The fourth step: turn on the telemedicine unit, now we can see on hyper terminal windows what is the output of the PIC microcontroller and the response of the AT command that returned from the GSM Modem. At the same time we can see on the other window the AT commands that the GSM Modem receive it from PIC microcontroller, AT commands response, and the coded samples of the analog to digital converter. Figure5.1 and Figure5.2 show the both windows of hyper terminal on each PC.

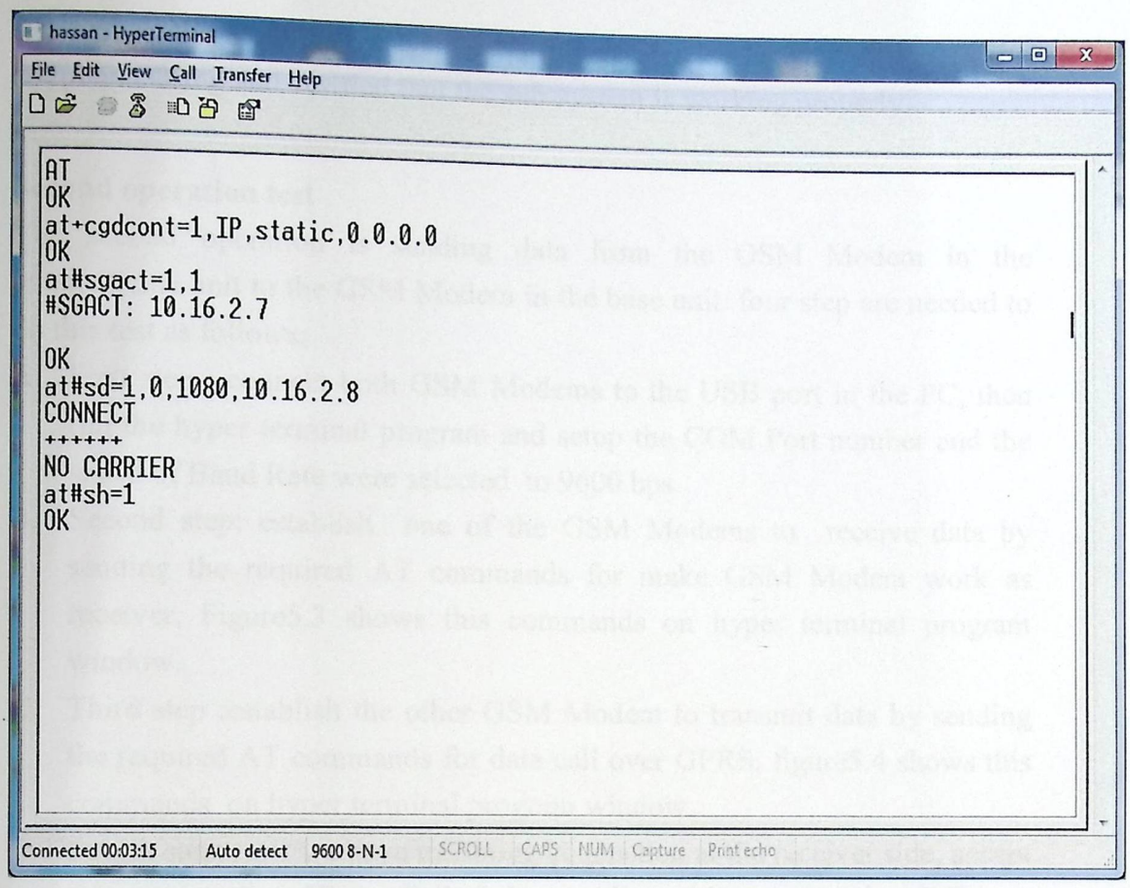


Figure5.1:AT commands and it's responses on hyper terminal for the PIC

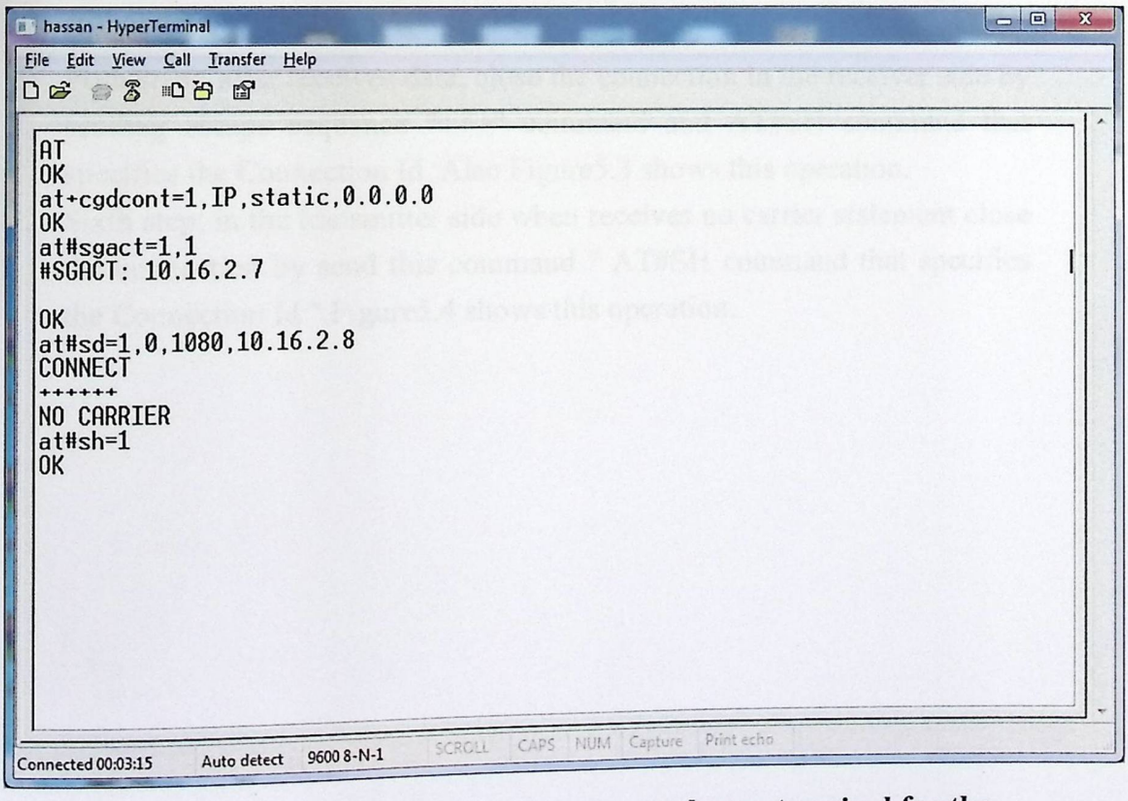


Figure5.2:AT commands and it's responses on hyper terminal for the GSM modem

After doing this steps , we solved the problems of delay between each AT command string and verified that the sub-system is working properly.

2. Second operation test

The second operation is sending data from the GSM Modem in the telemedicine unit to the GSM Modem in the base unit. four step are needed to do this test as follows:

A. First step : connect both GSM Modems to the USB port in the PC, then run the hyper terminal program and setup the COM Port number and the speed of Baud Rate were selected to 9600 bps.

B. Second step: establish one of the GSM Modems to receive data by sending the required AT commands for make GSM Modem work as receiver, Figure5.3 shows this commands on hyper terminal program window.

C. Third step :establish the other GSM Modem to transmit data by sending the required AT commands for data call over GPRS, figure5.4 shows this commands on hyper terminal program window.

D. Fourth step: now we have incoming connection at the receiver side, accept this connection "Data Call " by sending this command AT#SA = <connection Id> , now we can exchange data and receive it .figure5.3 shows this operation.

E. Fifth step: after receives data, close the connection in the receiver side by sending escape sequence "+++" command and AT#SH command that specifies the Connection Id .Also Figure5.3 shows this operation.

F. Sixth step: in the transmitter side when receives no carrier statement close the connection by send this command " AT#SH command that specifies the Connection Id ".Figure5.4 shows this operation.

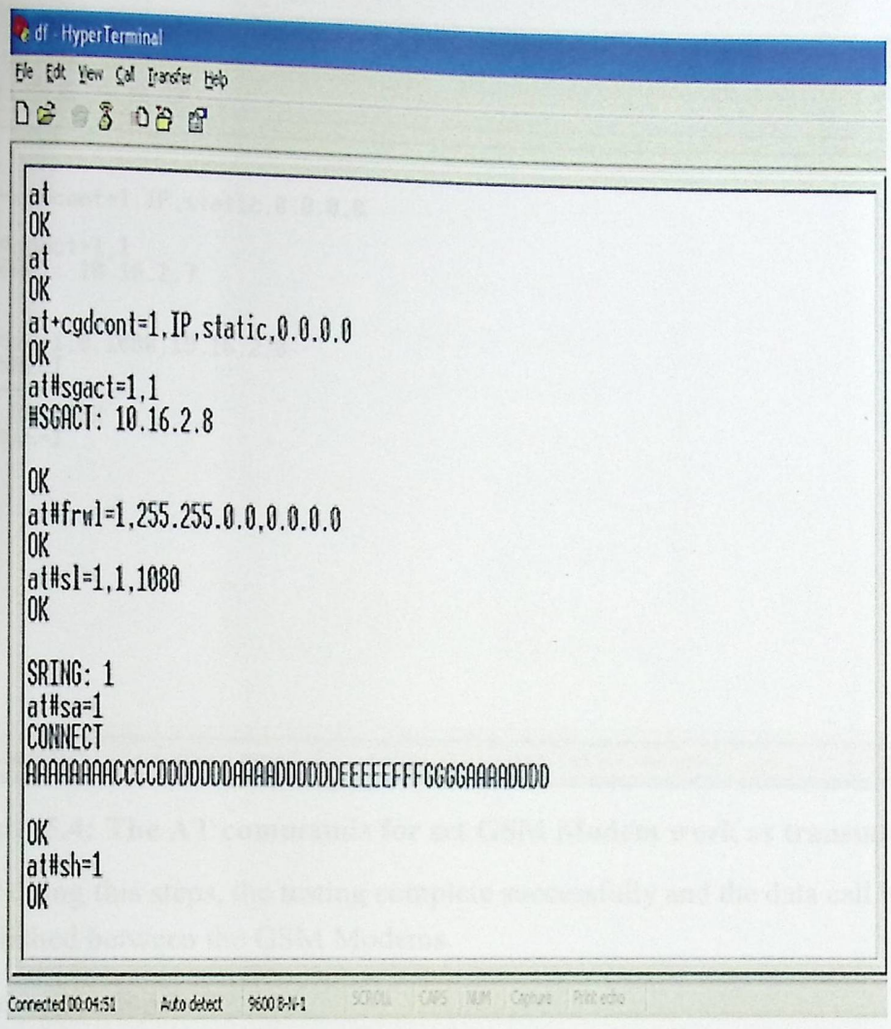


Figure5.3: AT commands for set GSM Modem work as receiver &the sample received

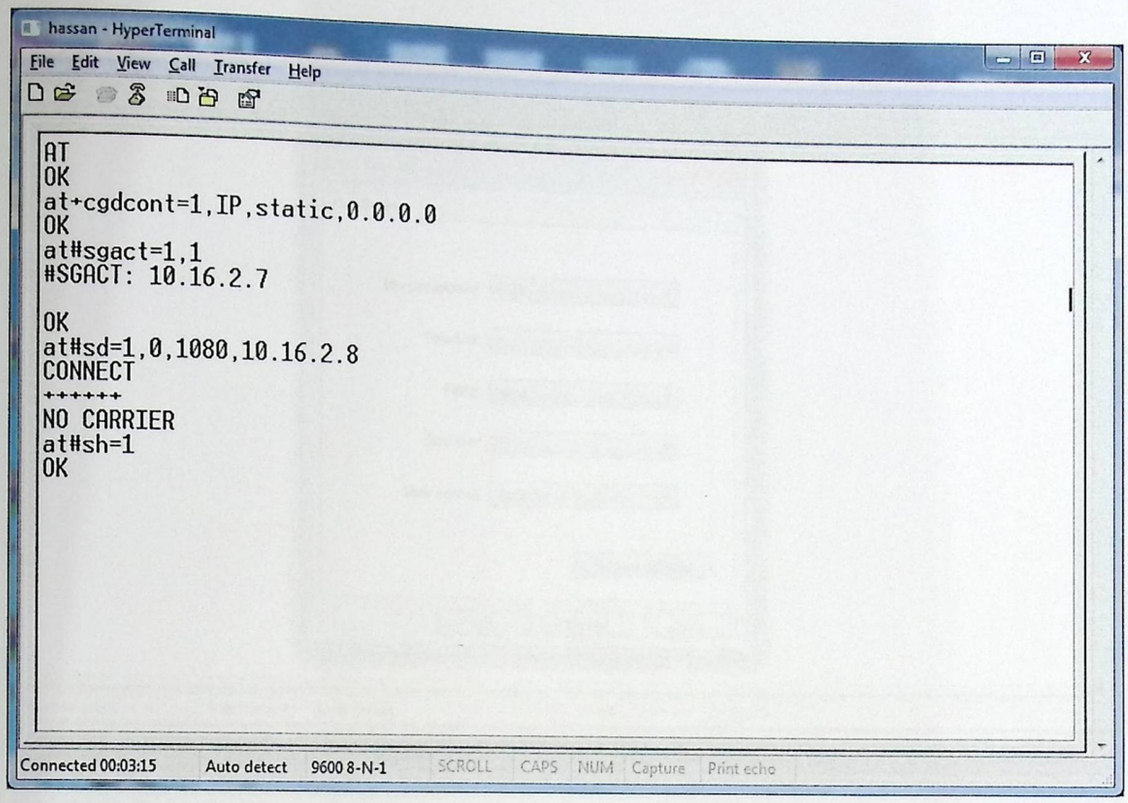


Figure5.4: The AT commands for set GSM Modem work as transmitter

After doing this steps, the testing complete successfully and the data call is established between the GSM Modems.

3. **Third operation test**

The latest one is interfacing the GSM Modem with PC in the base unit side, connect the GSM Modem to PC using USB Port, then run hyper terminal program and setup the COM Port number and the speed of Baud Rate were selected to 9600 bps .finally send at commands to the GSM Modem and wait for it's response,Figure5.5 shows example of this test.

As seen in Figure5.5 the AT commands sent to the GSM Modem from PC and PC receive the response of this commands from the GSM Modem. the testing complete and the interfacing done successfully.

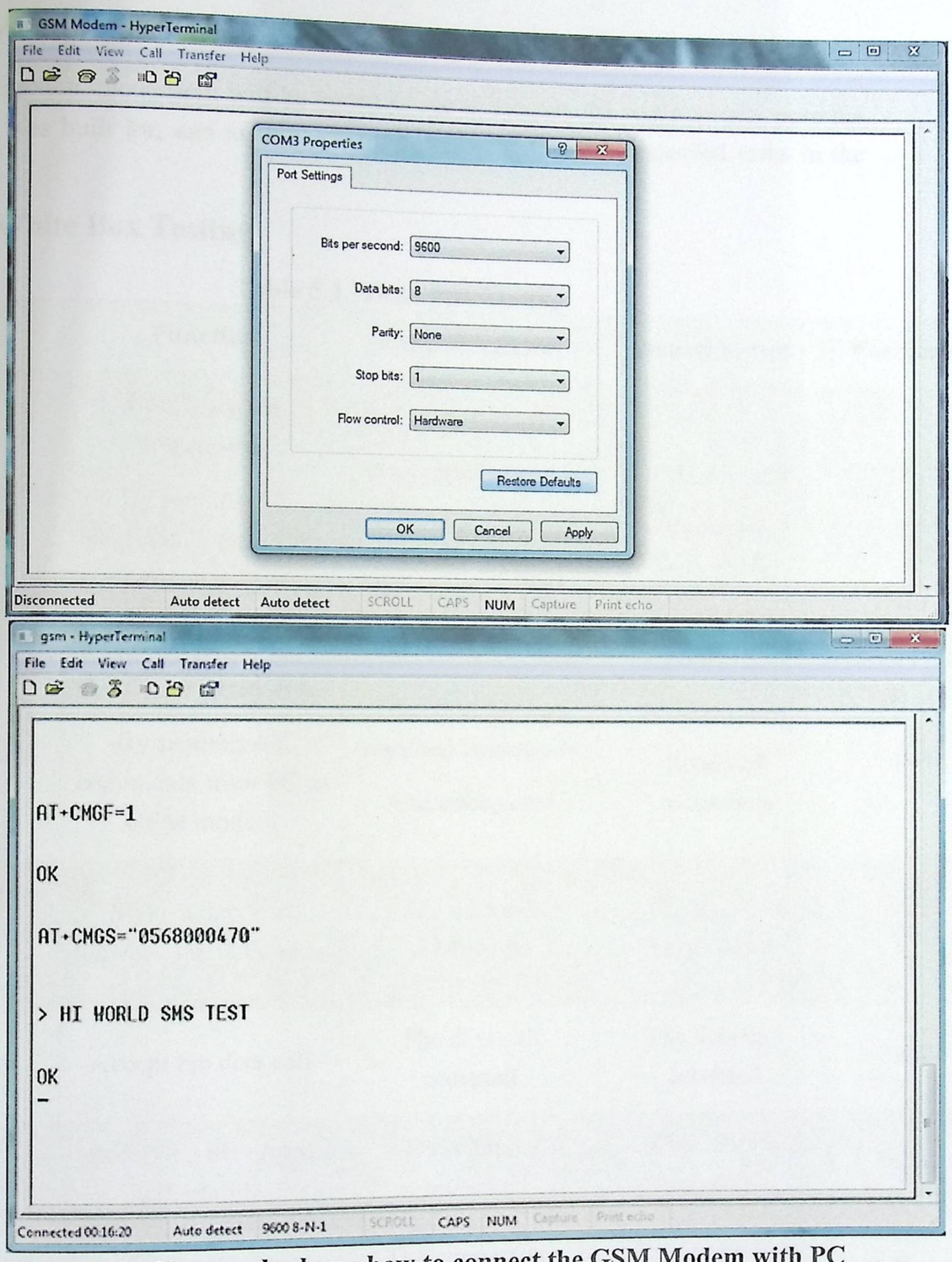


Figure 5.5 AN example shows how to connect the GSM Modem with PC

5.3.3 System Testing

This section explains the system testing. It should be tested by using a complete process of connecting the electrical system components, sending the data call commands from PIC microcontroller to the GSM Modem in the telemedicine unit, sending the required AT commands for establish the receiver from PC to the GSM Modem in the base unit, exchange data between both units, and finally terminate the connection between them. By implementing this process, the system works very well.

5.3.4 Acceptance testing

In this section, the system will be tested to see if it meets the requirements were the system was built for, and at this point the system did meet the needed tasks in the system.

5.3.5 White Box Testing

Table 5.2 White Box Testing

	Unit	Function	Expected Result	Actual Result	Verification
1	Telemedicine Unit	Configure the transmitter By sending AT commands from PIC microcontroller to GSM modem	The GSM Modem received commands and configured	GSM Modem Received commands	pass
2	Base Unit	Configure the receiver By sending AT commands from PC to GSM modem	The GSM Modem received commands And configured	GSM Modem Received commands	pass
3	Telemedicine Unit & Base Unit	Make a data call between the both units	The data call established	The data call established	pass
4	Base Unit	Accept the data call	The data call accepted	The data call accepted	pass
5	Base Unit	Receiving the coded A/D samples	The samples received	The samples received	Pass
6	Base Unit	Terminate the connection	The connection terminated	The connection terminated	Pass
7	Telemedicine Unit	Terminate the connection when receive no carrier statement	The connection terminated	The connection terminated	Pass

5.3.4 Acceptance testing

In this section, the system will be tested to see if it meets the requirements were the system was built for, and at this point the system did meet the needed tasks in the system.

5.3.5 White Box Testing

Table 5.2 White Box Testing

	Unit	Function	Expected Result	Actual Result	Verification
	Telemedicine Unit	Configure the transmitter By sending AT commands from PIC microcontroller to GSM modem	The GSM Modem received commands and configured	GSM Modem Received commands	pass
2	Base Unit	Configure the receiver By sending AT commands from PC to GSM modem	The GSM Modem received commands And configured	GSM Modem Received commands	pass
3	Telemedicine Unit & Base Unit	Make a data call between the both units	The data call established	The data call established	pass
4	Base Unit	Accept the data call	The data call accepted	The data call accepted	pass
5	Base Unit	Receiving the coded A/D samples	The samples received	The samples received	Pass
6	Base Unit	Terminate the connection	The connection terminated	The connection terminated	Pass
7	Telemedicine Unit	Terminate the connection when receive no carrier statement	The connection terminated	The connection terminated	Pass

CHAPTER

6

FUTURE WORK

6.1 Future Work

CHAPTER SIX

FUTURE WORK

6.1 Future work :

Our project can be developed in many fields and parts, we will talk about the most important fields, and these improvements are to make the life easier to the people and to benefit from the growth of communications technology.

The first improvement is to enable this project to work in third generation systems (3G) ,3G will enable to provide more developed and wider services and on other hand will give more data rate in download and upload.

The second improvement is to send not only the ECG signal but also the temperature ,respiratory and blood pressure signals, and this will increase the number of people that benefit from this project because it will become more comprehensive in treatment the patients .

Other improvement that can do in future is to support the ambulance in telemedicine unit with a camera to enable the doctor in order to see the patient in ambulance, and this will provide more accurate treatment .

In conclusion the aim of the project was achieved successfully to operate the wireless tele-ECG systems in our region that works in GSM technology with high data rate for upload and download and worked in real time .

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Appendix A

1. **AT** Attention command
2. **AT*** List all supported AT commands
3. **ATZ** Restore to user profile (ver. 2)
4. **AT&F** Set to factory-defined configuration (ver. 2)
5. **ATI** Identification information (ver. 3)
6. **AT&W** Store user profile
7. **AT+CLAC** List all available AT commands
8. **AT+CGMI** Request manufacturer identification (ver. 1)
9. **AT+CGMM** Request model identification
10. **AT+CGMR** Request revision identification
11. **AT+CGSN** Request product serial number identification
12. **AT+GCAP** Request modem capabilities list
13. **AT+GMI** Request manufacturer information
14. **AT+GMM** Request model identification
15. **AT+GMR** Request revision identification
16. **ATA** Answer incoming call command (ver. 2)
17. **ATH** Hook control (ver. 2)
18. **ATD** Dial command (ver. 5)
19. **ATO** Return to online data mode
20. **AT+CVHU** Voice hangup control
21. **AT+CLCC** List current calls
22. **AT*CPI** Call progress information
23. **ATE** Command echo (ver. 2)
24. **ATSO** Automatic answer control
25. **ATS2** Escape sequence character
26. **ATS3** Command line termination character (ver. 3)
27. **ATS4** Response formatting character (ver. 3)
28. **ATS5** Command line editing character (ver. 3)
29. **ATS7** Completion connection timeout
30. **ATS10** Automatic disconnect delay control
31. **ATQ** Result code suppression (ver. 2)
32. **ATV** DCE response mode (ver. 2)

33. **ATX** Call progress monitoring control
34. **AT&C** Circuit 109 (DCD) control
35. **AT&D** Circuit 108 (DTR) response
36. **AT+IFC** Cable interface DTE-DCE local flow control
37. **AT+ICF** Cable interface character format (ver. 2)
38. **AT+IPR** Cable interface port rate
39. **AT+ILRR** Cable interface local rate reporting
40. **AT+DS** Data compression (ver. 3)
41. **AT+DR** Data compression reporting
42. **AT+WS46** Mode selection
43. **AT+FCLASS** Select mode
44. **AT*ECBP** CHF button pushed (ver. 2)
45. **AT+CMUX** Switch to 07.10 multiplexer (ver. 2)
46. **AT*EINA** Ericsson system interface active
47. **AT*SEAM** Add menu item
48. **AT*SESAF** SEMC show and focus
49. **AT*SELERT** SEMC create alert (information text)
50. **AT*SESTRI** SEMC create string Input
51. **AT*SELIST** SEMC create list
52. **AT*SETICK** SEMC create ticker
53. **AT*SEDATE** SEMC create date field
54. **AT*SEGAUGE** SEMC create gauge (bar graph/progress feedback)
55. **AT*SEGUP** SEMC update gauge (bar graph/ progress feedback)
56. **AT*SEONO** SEMC create on/off input
57. **AT*SEYNQ** SEMC create yes/no question
58. **AT*SEDEL** SEMC GUI delete
59. **AT*SESLE** SEMC soft key label (ver. 1)
60. **AT*SERSK** SEMC remove soft key
61. **AT*SEUIS** SEMC UI session establish/terminate
62. **AT*EIBA** Ericsson Internal Bluetooth address
63. **AT+BINP** Bluetooth input
64. **AT+BLDN** Bluetooth last dialled number
65. **AT+BVRA** Bluetooth voice recognition activation
66. **AT+NREC** Noise reduction and echo cancelling
67. **AT+VGM** Gain of microphone
68. **AT+VGS** Gain of speaker
69. **AT+BRSF** Bluetooth retrieve supported
70. **AT+GCLIP** Graphical caller ID presentation

71. **AT+CSCS** Select TE character set (ver. 3)
72. **AT+CHUP** Hang up call
73. **AT+CRC** Cellular result codes (ver. 2)
74. **AT+CR** Service reporting control
75. **AT+CV120** V.120 rate adaption protocol
76. **AT+VTS** DTMF and tone generation
77. **AT+CBST** Select bearer service type (ver. 3)
78. **AT+CRLP** Radio link protocol (ver. 2)
79. **AT+CEER** Extended error report (ver. 2)
80. **AT+CHSD** HSCSD device parameters (ver. 2)
81. **AT+CHSN** HSCSD non-transparent call configuration (ver. 2)
82. **AT+CHSC** HSCSD current call parameters (ver. 2)
83. **AT+CHSR** HSCSD parameters report (ver. 2)
84. **AT+CHSU** HSCSD automatic user-initiated upgrade
85. **AT+CNUM** Subscriber number (ver. 2)
86. **AT+CREG** Network registration (ver. 2)
87. **AT+COPS** Operator selection (ver. 2)
88. **AT+CLIP** Calling line identification (ver. 2)
89. **AT+CLIR** Calling line identification restriction
90. **AT+CCFC** Calling forwarding number and conditions (ver. 2)
91. **AT+CCWA** Call waiting (ver. 2)
92. **AT+CHLD** Call hold and multiparty (ver. 1)
93. **AT+CSSN** Supplementary service notification (ver. 2)
94. **AT+CAOC** Advice of charge
95. **AT+CACM** Accumulated call meter (ver. 2)
96. **AT+CAMM** Accumulated call meter maximum
97. **AT+CDIP** Called line identification presentation
98. **AT+COLP** Connected line identification presentation
99. **AT+CPOL** Preferred operator list
100. **AT+COPN** Read operator names
101. **AT*EDIF** Divert function (ver. 2)
102. **AT*EIPS** Identify presentation set
103. **AT+CUSD** Unstructured supplementary service data (ver. 2)
104. **AT+CLCK** Facility lock (ver. 5)
105. **AT+CPWD** Change password (Ver. 3)
106. **AT+CFUN** Set phone functionality (ver. 2)
107. **AT+CPAS** Phone activity status (ver. 3)
108. **AT+CPIN** PIN control (ver. 2)

109. **AT+CBC** Battery charge (ver. 2)
110. **AT+CSQ** Signal quality (ver.1)
111. **AT+CKPD** Keypad control (ver. 7)
112. **AT+CIND** Indicator control (ver. 5)
113. **AT+CMAR** Master reset
114. **AT+CMER** Mobile equipment event reporting
115. **AT*ECAM** Ericsson call monitoring (ver. 2)
116. **AT+CLAN** Language
117. **AT*EJAVA** Ericsson Java application function
118. **AT+CSIL** Silence Command
119. **AT*ESKL** Key-lock mode
120. **AT*ESKS** Key sound
121. **AT*EAPP** Application function (ver. 5)
122. **AT+CMEC** Mobile equipment control mode
123. **AT+CRSM** Restricted SIM access
124. **AT*EKSE** Ericsson keystroke send
125. **AT+CRSL** Ringer sound level (ver. 2)
126. **AT+CLVL** Loudspeaker volume level
127. **AT+CMUT** Mute control
128. **AT*EMEM** Ericsson memory management
129. **AT+CRMP** Ring melody playback (ver. 2)
130. **AT*EKEY** Keypad/joystick control (ver. 2)
131. **AT*ECDF** Ericsson change dedicated file
132. **AT*STKC** SIM application toolkit configuration
133. **AT*STKE** SIM application toolkit envelope command send
134. **AT*STKR** SIM application toolkit command response
135. **AT+CMEE** Report mobile equipment error
136. **AT+CSMS** Select message service (ver.2)
137. **AT+CPMS** Preferred message storage (ver. 4)
138. **AT+CMGF** Message format (ver. 1)
139. **AT+CSCA** Service centre address (ver. 2)
140. **AT+CSAS** Save settings
141. **AT+CRES** Restore settings
142. **AT+CNMI** New messages indication to TE (ver. 4)
143. **AT+CMGL** List message (ver. 2)
144. **AT+CMGR** Read message (ver. 2)
145. **AT+CMGS** Send message (ver. 2)
146. **AT+CMSS** Send from storage (ver. 2)

147. **AT+CMGW** Write message to memory (ver. 2)
148. **AT+CMGD** Delete message
149. **AT+CMGC** Send command (ver. 1)
150. **AT+CMMS** More messages to send
151. **AT+CGDCONT** Define PDP context (ver. 1)
152. **AT+CGSMS** Select service for MO SMS messages
153. **AT+CGATT** Packet service attach or detach
154. **AT+CGACT** PDP context activate or deactivate
155. **AT+CGDATA** Enter data state
156. **AT+CGEREP** Packet domain event reporting (ver. 1)
157. **AT+CGREG** Packet domain network registration status
158. **AT+CGPADDR** Show PDP address
159. **AT+CGDSCONT** Define secondary PDP context
160. **AT+CGTFT** Traffic flow template
161. **AT+CGEQREQ** 3G quality of service profile (requested)
162. **AT+CGEQMIN** 3G quality of service profile (minimum acceptable)
163. **AT+CGEQNEG** 3G quality of service profile (negotiated)
164. **AT+CGCMOD** PDP context modify
165. **Extension of ATD** – Request GPRS service
166. **Extension of ATD** – Request packet domain IP service
167. **AT+CPBS** Phonebook storage (ver. 3)
168. **AT+CPBR** Phonebook read (ver. 2)
169. **AT+CPBF** Phonebook find (ver. 2)
170. **AT+CPBW** Phonebook write (ver. 4)
171. **AT+CCLK** Clock (ver. 4)
172. **AT+CALA** Alarm (ver. 3)
173. **AT+CALD** Alarm delete
174. **AT+CAPD** Postpone or dismiss an alarm (ver. 2)
175. **AT*EDST** Ericsson daylight saving time
176. **AT+CIMI** Request international mobile subscriber identity
177. **AT*EPEE** PIN event
178. **AT*EAPS** Active profile set
179. **AT*EAPN** Active profile rename
180. **AT*EBCA** Battery and charging algorithm (ver. 4)
181. **AT*ELIB** Ericsson list Bluetooth devices
182. **AT*EVAA** Voice answer active (ver. 1)
183. **AT*EMWS** Magic word set
184. **AT+CPROT** Enter protocol mode

185. **AT*EWDT** WAP download timeout
186. **AT*EWBA** WAP bookmark add (ver. 2)
187. **AT*EWCT** WAP connection timeout
188. **AT*EIAC** Internet account, create
189. **AT*EIAD** Internet account configuration, delete
190. **AT*EIAW** Internet account configuration, write general parameters
191. **AT*EIAR** Internet account configuration, read general parameters
192. **AT*EIAPSW** Internet account configuration, write PS bearer parameters
193. **AT*EIAPSR** Internet account configuration, read PS bearer parameters
194. **AT*EIAPSSW** Internet account configuration, write secondary PDP context parameters
195. **AT*EIAPSSR** Internet account configuration, read secondary PDP context parameters
196. **AT*EIACSW** Internet account configuration, write CSD bearer parameters
197. **AT*EIACSR** Internet account configuration, read CSD bearer parameters
198. **AT*EIABTW** Internet account configuration, write Bluetooth bearer parameters
199. **AT*EIABTR** Internet account configuration, read Bluetooth bearer parameters
200. **AT*EIAAUW** Internet account configuration, write authentication parameters
201. **AT*EIAAUR** Internet account configuration, read authentication parameters
202. **AT*EIALCPW** Internet account configuration, write PPP parameters – LCP
203. **AT*EIALCPR** Internet account configuration, read PPP parameters – LCP
204. **AT*EIAIPCPW** Internet account configuration, write PPP parameters – IPCP
205. **AT*EIAIPCPR** Internet account configuration, read PPP parameters – IPCP
206. **AT*EIADNSV6W** Internet account configuration, write DNS parameters – IPv6CP
207. **AT*EIADNSV6R** Internet account configuration, read DNS parameters – IPv6CP
208. **AT*EIARUTW** Internet account configuration, write routing table parameters
209. **AT*EIARUTD** Internet account configuration, delete routing table parameters
210. **AT*EIARUTR** Internet account configuration, read routing table parameters
211. **AT*SEACC** Accessory class report
212. **AT*SEACID** Accessory identification

213. **AT*SEACID2** Accessory identification (Bluetooth)
214. **AT*SEAUDIO** Accessory class report
215. **AT*SECHA** Charging control
216. **AT*SELOG** SE read log
217. **AT*SEPING** SE ping command
218. **AT*SEAULS** SE audio line status
219. **AT*SEFUNC** SE functionality status (ver. 2)
220. **AT*SEFIN** SE flash Information
221. **AT*SEFEXP** Flash auto exposure setting from ME
222. **AT*SEMOD** Camera mode indicator to the flash
223. **AT*SEREDI** Red eye reduction indicator to the flash
224. **AT*SEFRY** Ready indicator to the ME
225. **AT*SEAUP** Sony Ericsson audio parameters
226. **AT*SEVOL** Volume level
227. **AT*SEVOLIR** Volume indication request
228. **AT*SEBIC** Status bar icon
229. **AT*SEANT** Antenna identification
230. **AT*SESP** Speaker mode on/off
231. **AT*SETBC** Text to bitmap converter
232. **AT*SEAVRC** Sony Ericsson audio video remote control
233. **AT*SEMMIR** Sony Ericsson multimedia information request
234. **AT*SEAPP** Sony Ericsson application
235. **AT*SEAPPIR** Sony Ericsson application indication request
236. **AT*SEJCOMM** Sony Ericsson Java comm.
237. **AT*SEDUC** Sony Ericsson disable USB charge
238. **AT*SEABS** Sony Ericsson accessory battery status
239. **AT*SEAVRCIR** Sony Ericsson audio video remote control indication request
240. **AT*SEGPSA** Sony Ericsson global positioning system accessory
241. **AT*SEAUDIO** Accessory class report
242. **AT*SEGPSA** Sony Ericsson global positioning system accessory
243. **AT*SEAUDIO** Accessory Class Report
244. **AT*SEGPSA** Sony Ericsson global positioning system accessory
245. **AT*SETIR** Sony Ericsson time information request
246. **AT*SEMCM** Sony Ericsson memory card management
247. **AT*SEAUDIO** Accessory Class Report

Appendix B

PIC18F2455/2550/4455/4550
Data Sheet

28/40/44-Pin, High-Performance, Enhanced Flash, USB Microcontrollers with nanoWatt Technology

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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ISO/TS 16949:2002

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MICROCHIP PIC18F2455/2550/4455/4550

28/40/44-Pin, High-Performance, Enhanced Flash, USB Microcontrollers with nanoWatt Technology

Universal Serial Bus Features:

- USB V2.0 Compliant
- Low Speed (1.5 Mb/s) and Full Speed (12 Mb/s)
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- Supports up to 32 Endpoints (16 bidirectional)
- 1-Kbyte Dual Access RAM for USB
- On-Chip USB Transceiver with On-Chip Voltage Regulator
- Interface for Off-Chip USB Transceiver
- Streaming Parallel Port (SPP) for USB streaming transfers (40/44-pin devices only)

Power-Managed Modes:

- Run: CPU on, peripherals on
- Idle: CPU off, peripherals on
- Sleep: CPU off, peripherals off
- Idle mode currents down to 5.8 μA typical
- Sleep mode currents down to 0.1 μA typical
- Timer1 Oscillator: 1.1 μA typical, 32 kHz, 2V
- Watchdog Timer: 2.1 μA typical
- Two-Speed Oscillator Start-up

Flexible Oscillator Structure:

- Four Crystal modes, including High Precision PLL for USB
- Two External Clock modes, up to 48 MHz
- Internal Oscillator Block:
  - 8 user-selectable frequencies, from 31 kHz to 8 MHz
  - User-tunable to compensate for frequency drift
- Secondary Oscillator using Timer1 @ 32 kHz
- Dual Oscillator options allow microcontroller and USB module to run at different clock speeds
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if any clock stops

Peripheral Highlights:

- High-Current Sink/Source: 25 mA/25 mA
- Three External Interrupts
- Four Timer modules (Timer0 to Timer3)
- Up to 2 Capture/Compare/PWM (CCP) modules:
  - Capture is 16-bit, max. resolution 5.2 ns (TCY/16)
  - Compare is 16-bit, max. resolution 83.3 ns (TCY)
  - PWM output: PWM resolution is 1 to 10-bit
- Enhanced Capture/Compare/PWM (ECCP) module:
  - Multiple output modes
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart
- Enhanced USART module:
  - LIN bus support
- Master Synchronous Serial Port (MSSP) module supporting 3-wire SPI (all 4 modes) and I^2C™ Master and Slave modes
- 10-bit, up to 13-channel Analog-to-Digital Converter module (A/D) with Programmable Acquisition Time
- Dual Analog Comparators with Input Multiplexing

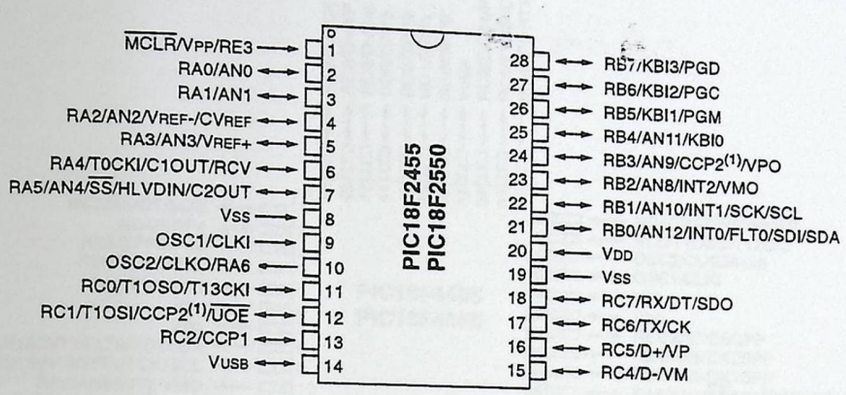
Special Microcontroller Features:

- C Compiler Optimized Architecture with optional Extended Instruction Set
- 100,000 Erase/Write Cycle Enhanced Flash Program Memory typical
- 1,000,000 Erase/Write Cycle Data EEPROM Memory typical
- Flash/Data EEPROM Retention: > 40 years
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 41 ms to 131s
- Programmable Code Protection
- Single-Supply 5V In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug (ICD) via two pins
- Optional dedicated ICD/ICSP port (44-pin devices only)
- Wide Operating Voltage Range (2.0V to 5.5V)

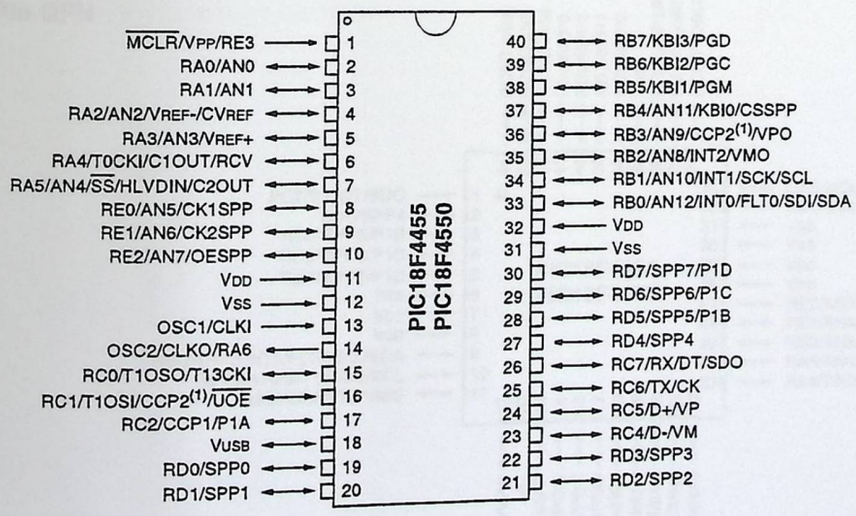
Device	Program Memory		Data Memory		I/O	10-Bit A/D (ch)	CCP/ECCP (PWM)	SPP	MSSP		EAUSART	Comparators	Timers 8/16-Bit
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)					SPI	Master I^2C™			
PIC18F2455	24K	12288	2048	256	24	10	2/0	No	Y	Y	1	2	1/3
PIC18F2550	32K	16384	2048	256	24	10	2/0	No	Y	Y	1	2	1/3
PIC18F4455	24K	12288	2048	256	35	13	1/1	Yes	Y	Y	1	2	1/3
PIC18F4550	32K	16384	2048	256	35	13	1/1	Yes	Y	Y	1	2	1/3

Pin Diagrams

28-Pin PDIP, SOIC



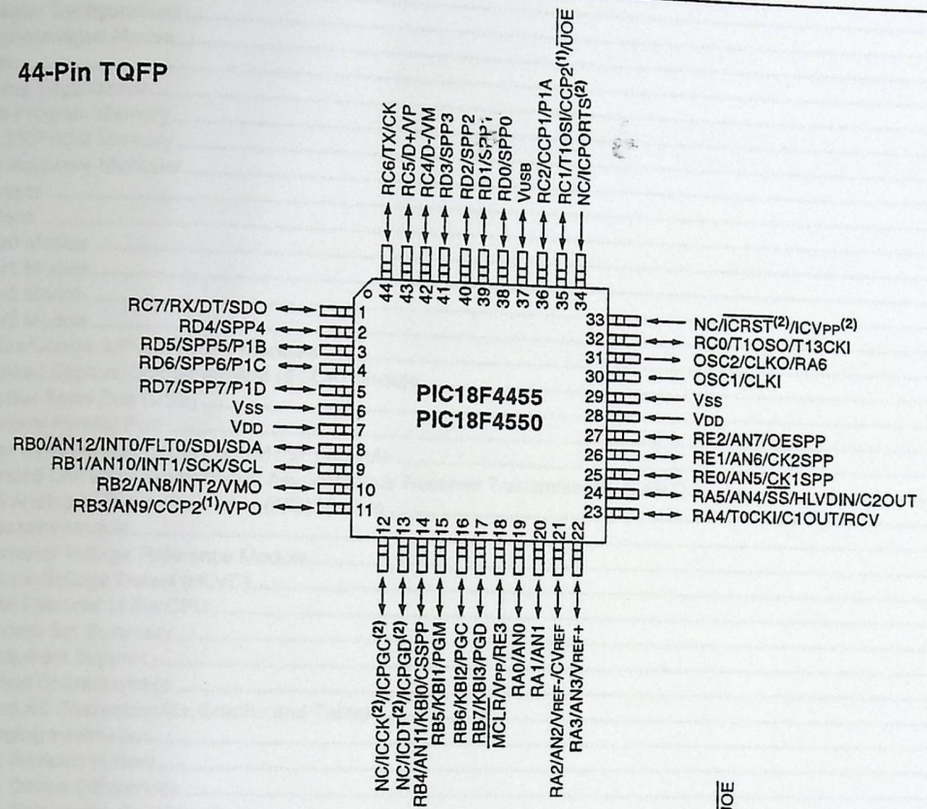
40-Pin PDIP



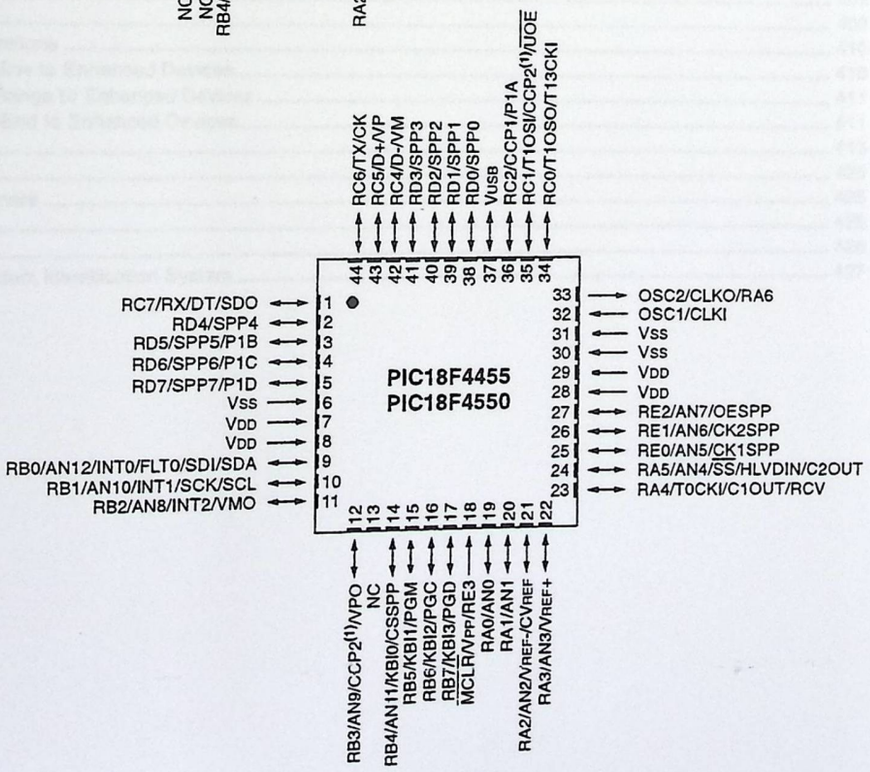
Note 1: RB3 is the alternate pin for CCP2 multiplexing.

Pin Diagrams (Continued)

44-Pin TQFP



44-Pin QFN



Note 1: RB3 is the alternate pin for CCP2 multiplexing.

2: Special ICPORTS features available in select circumstances. See **Section 25.9 "Special ICPORT Features (Designated Packages Only)"** for more information.

Table of Contents

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An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

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NOTES:

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F2455
- PIC18F2550
- PIC18F4455
- PIC18F4550
- PIC18LF2455
- PIC18LF2550
- PIC18LF4455
- PIC18LF4550

This family of devices offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high endurance, Enhanced Flash program memory. In addition to these features, the PIC18F2455/2550/4455/4550 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power sensitive applications.

1.1 New Core Features

1.1.1 nanoWatt TECHNOLOGY

All of the devices in the PIC18F2455/2550/4455/4550 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **Alternate Run Modes:** By clocking the controller from the Timer1 source or the internal oscillator block, power consumption during code execution can be reduced by as much as 90%.
- **Multiple Idle Modes:** The controller can also run with its CPU core disabled but the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operation requirements.
- **On-the-Fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.
- **Low Consumption in Key Modules:** The power requirements for both Timer1 and the Watchdog Timer are minimized. See **Section 28.0 "Electrical Characteristics"** for values.

1.1.2 UNIVERSAL SERIAL BUS (USB)

Devices in the PIC18F2455/2550/4455/4550 family incorporate a fully featured Universal Serial Bus communications module that is compliant with the USB Specification Revision 2.0. The module supports both low-speed and full-speed communication for all supported data transfer types. It also incorporates its own on-chip transceiver and 3.3V regulator and supports the use of external transceivers and voltage regulators.

1.1.3 MULTIPLE OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18F2455/2550/4455/4550 family offer twelve different oscillator options, allowing users a wide range of choices in developing application hardware. These include:

- Four Crystal modes using crystals or ceramic resonators.
- Four External Clock modes, offering the option of using two pins (oscillator input and a divide-by-4 clock output) or one pin (oscillator input, with the second pin reassigned as general I/O).
- An internal oscillator block which provides an 8 MHz clock (±2% accuracy) and an INTRC source (approximately 31 kHz, stable over temperature and V_{DD}), as well as a range of 6 user-selectable clock frequencies, between 125 kHz to 4 MHz, for a total of 8 clock frequencies. This option frees an oscillator pin for use as an additional general purpose I/O.
- A Phase Lock Loop (PLL) frequency multiplier, available to both the High-Speed Crystal and External Oscillator modes, which allows a wide range of clock speeds from 4 MHz to 48 MHz.
- Asynchronous dual clock operation, allowing the USB module to run from a high-frequency oscillator while the rest of the microcontroller is clocked from an internal low-power oscillator.

Besides its availability as a clock source, the internal oscillator block provides a stable reference source that gives the family additional features for robust operation:

- **Fail-Safe Clock Monitor:** This option constantly monitors the main clock source against a reference signal provided by the internal oscillator. If a clock failure occurs, the controller is switched to the internal oscillator block, allowing for continued low-speed operation or a safe application shutdown.
- **Two-Speed Start-up:** This option allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available.

1.2 Other Special Features

- **Memory Endurance:** The Enhanced Flash cells for both program memory and data EEPROM are rated to last for many thousands of erase/write cycles – up to 100,000 for program memory and 1,000,000 for EEPROM. Data retention without refresh is conservatively estimated to be greater than 40 years.
- **Self-Programmability:** These devices can write to their own program memory spaces under internal software control. By using a bootloader routine, located in the protected Boot Block at the top of program memory, it becomes possible to create an application that can update itself in the field.
- **Extended Instruction Set:** The PIC18F2455/2550/4455/4550 family introduces an optional extension to the PIC18 instruction set, which adds 8 new instructions and an Indexed Literal Offset Addressing mode. This extension, enabled as a device configuration option, has been specifically designed to optimize re-entrant application code originally developed in high-level languages such as C.
- **Enhanced CCP Module:** In PWM mode, this module provides 1, 2 or 4 modulated outputs for controlling half-bridge and full-bridge drivers. Other features include auto-shutdown for disabling PWM outputs on interrupt or other select conditions and auto-restart to reactivate outputs once the condition has cleared.
- **Enhanced Addressable USART:** This serial communication module is capable of standard RS-232 operation and provides support for the LIN bus protocol. Other enhancements include Automatic Baud Rate Detection and a 16-bit Baud Rate Generator for improved resolution. When the microcontroller is using the internal oscillator block, the EUSART provides stable operation for applications that talk to the outside world without using an external crystal (or its accompanying power requirement).
- **10-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated, without waiting for a sampling period and thus, reducing code overhead.
- **Dedicated ICD/ICSP Port:** These devices introduce the use of debugger and programming pins that are not multiplexed with other microcontroller features. Offered as an option in select packages, this feature allows users to develop I/O intensive applications while retaining the ability to program and debug in the circuit.

1.3 Details on Individual Family Members

Devices in the PIC18F2455/2550/4455/4550 family are available in 28-pin and 40/44-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in six ways:

1. Flash program memory (24 Kbytes for PIC18FX455 devices, 32 Kbytes for PIC18FX550).
2. A/D channels (10 for 28-pin devices, 13 for 40/44-pin devices).
3. I/O ports (3 bidirectional ports and 1 input only port on 28-pin devices, 5 bidirectional ports on 40/44-pin devices).
4. CCP and Enhanced CCP implementation (28-pin devices have two standard CCP modules, 40/44-pin devices have one standard CCP module and one ECCP module).
5. Streaming Parallel Port (present only on 40/44-pin devices).

All other features for devices in this family are identical. These are summarized in Table 1-1.

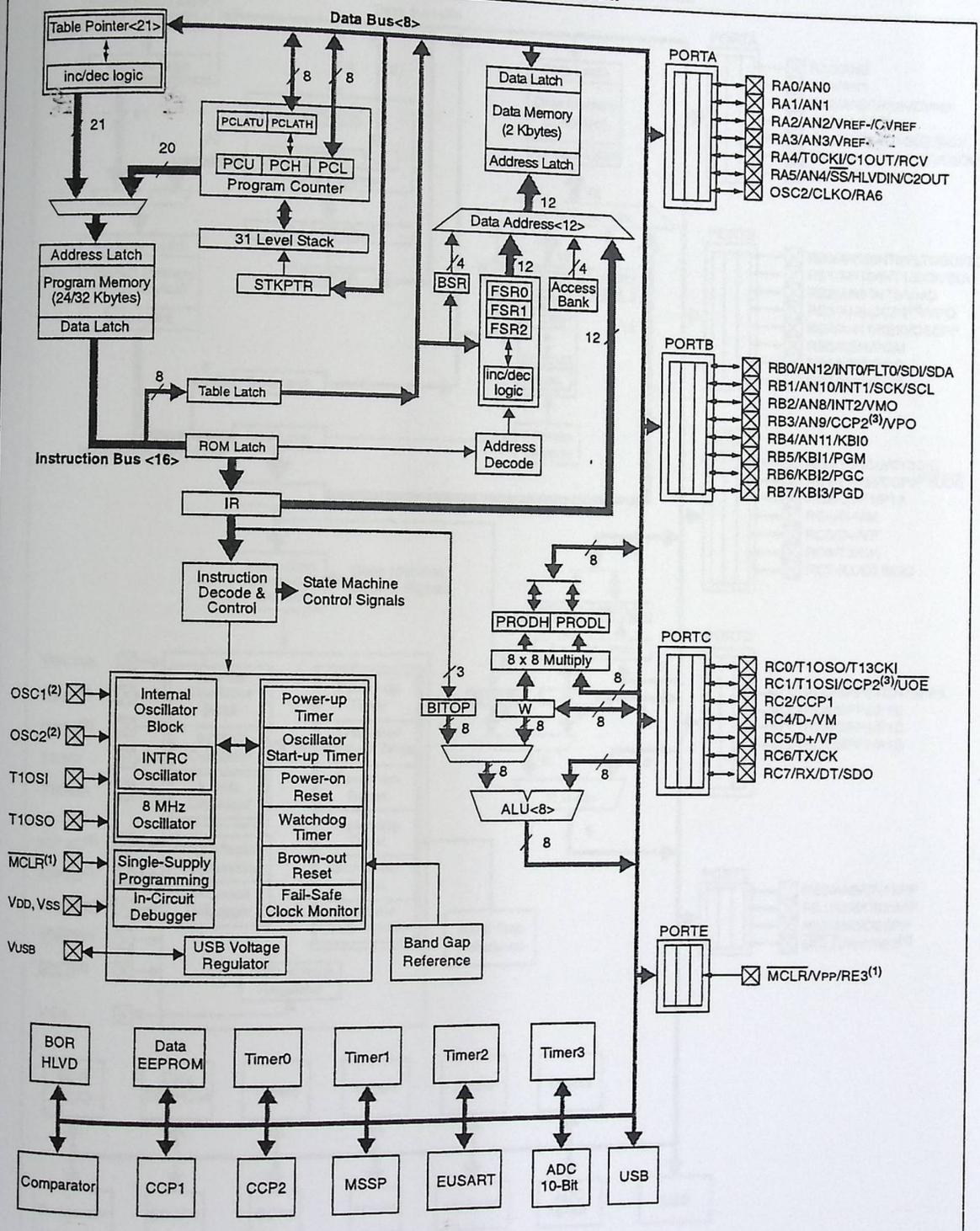
The pinouts for all devices are listed in Table 1-2 and Table 1-3.

Like all Microchip PIC18 devices, members of the PIC18F2455/2550/4455/4550 family are available as both standard and low-voltage devices. Standard devices with Enhanced Flash memory, designated with an "F" in the part number (such as PIC18F2550), accommodate an operating V_{DD} range of 4.2V to 5.5V. Low-voltage parts, designated by "LF" (such as PIC18LF2550), function over an extended V_{DD} range of 2.0V to 5.5V.

TABLE 1-1: DEVICE FEATURES

Features	PIC18F2455	PIC18F2550	PIC18F4455	PIC18F4550
Operating Frequency	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz
Program Memory (Bytes)	24576	32768	24576	32768
Program Memory (Instructions)	12288	16384	12288	16384
Data Memory (Bytes)	2048	2048	2048	2048
Data EEPROM Memory (Bytes)	256	256	256	256
Interrupt Sources	19	19	20	20
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E
Timers	4	4	4	4
Capture/Compare/PWM Modules	2	2	1	1
Enhanced Capture/ Compare/PWM Modules	0	0	1	1
Serial Communications	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART
Universal Serial Bus (USB) Module	1	1	1	1
Streaming Parallel Port (SPP)	No	No	Yes	Yes
10-Bit Analog-to-Digital Module	10 Input Channels	10 Input Channels	13 Input Channels	13 Input Channels
Comparators	2	2	2	2
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), $\overline{MCLR}$ (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), $\overline{MCLR}$ (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), $\overline{MCLR}$ (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), $\overline{MCLR}$ (optional), WDT
Programmable Low-Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled
Packages	28-pin PDIP 28-pin SOIC	28-pin PDIP 28-pin SOIC	40-pin PDIP 44-pin QFN 44-pin TQFP	40-pin PDIP 44-pin QFN 44-pin TQFP

FIGURE 1-1: PIC18F2455/2550 (28-PIN) BLOCK DIAGRAM

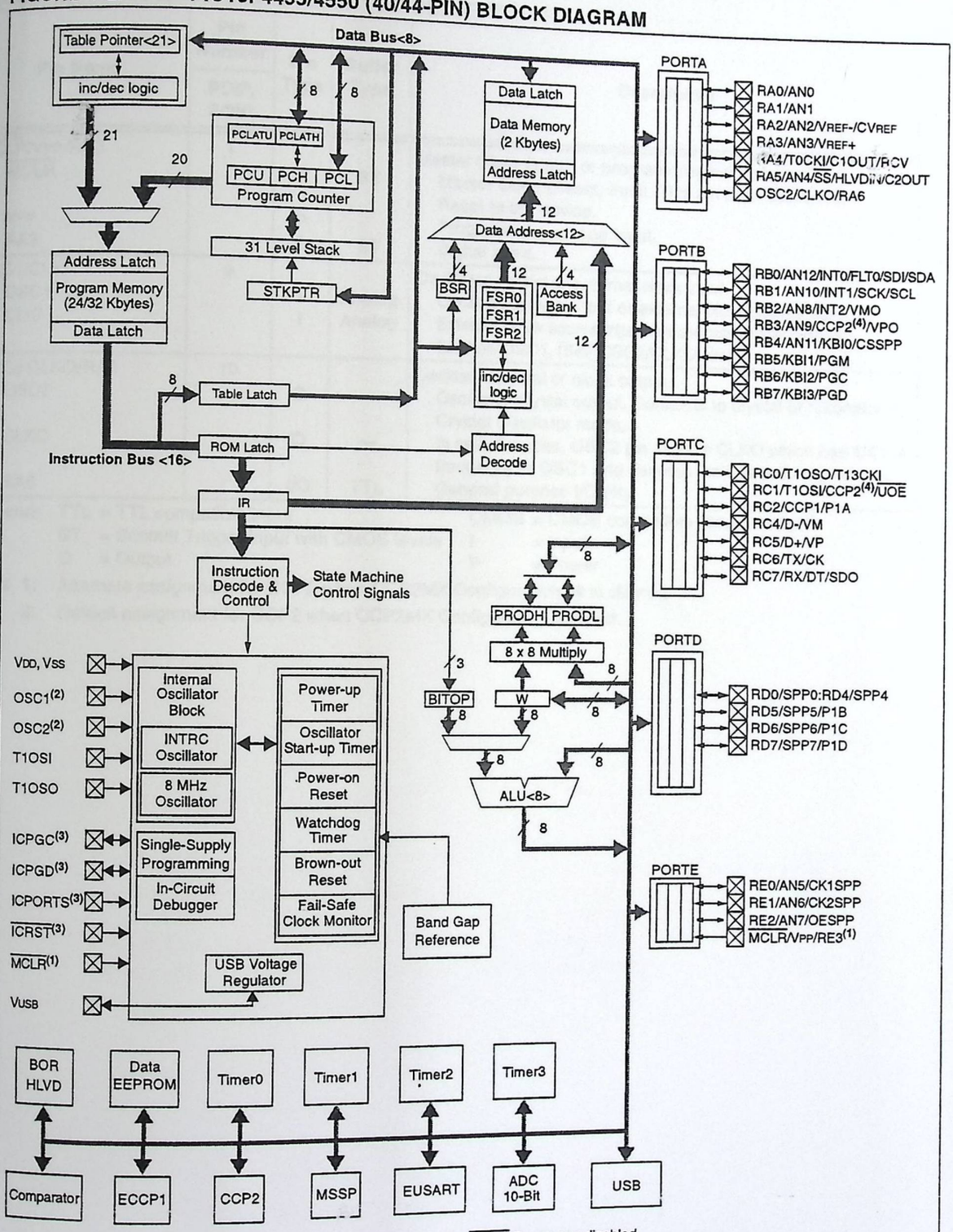


Note 1: RE3 is multiplexed with $\overline{MCLR}$ and is only available when the $\overline{MCLR}$ Resets are disabled.

2: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. Refer to **Section 2.0 "Oscillator Configurations"** for additional information.

3: RB3 is the alternate pin for CCP2 multiplexing.

FIGURE 1-2: PIC18F4455/4550 (40/44-PIN) BLOCK DIAGRAM



Note 1: RE3 is multiplexed with $\overline{MCLR}$ and is only available when the $\overline{MCLR}$ Resets are disabled.

2: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. Refer to **Section 2.0 "Oscillator Configurations"** for additional information.

3: These pins are only available on 44-pin TQFP packages under certain conditions. Refer to **Section 25.9 "Special ICPORT Features (Designated Packages Only)"** for additional information.

4: RB3 is the alternate pin for CCP2 multiplexing.

TABLE 1-2: PIC18F2455/2550 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	PDIP, SOIC			
MCLR/VPP/RE3	1			Master Clear (input) or programming voltage (input).
MCLR		I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP		P		Programming voltage input.
RE3		I	ST	Digital input.
OSC1/CLKI	9			Oscillator crystal or external clock input.
OSC1		I	Analog	Oscillator crystal input or external clock source input.
CLKI		I	Analog	External clock source input. Always associated with pin function OSC1. (See OSC2/CLKO pin.)
OSC2/CLKO/RA6	10			Oscillator crystal or clock output.
OSC2		O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO		O	—	In select modes, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6		I/O	TTL	General purpose I/O pin.

Legend: TTL = TTL compatible input
CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
I = Input
O = Output
P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

TABLE 1-2: PIC18F2455/2550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	PDIP, SOIC			
RA0/AN0	2			PORTA is a bidirectional I/O port.
RA0		I/O	TTL	Digital I/O.
AN0		I	Analog	Analog input 0.
RA1/AN1	3			
RA1		I/O	TTL	Digital I/O.
AN1		I	Analog	Analog input 1.
RA2/AN2/VREF-/CVREF	4			
RA2		I/O	TTL	Digital I/O.
AN2		I	Analog	Analog input 2.
VREF-		I	Analog	A/D reference voltage (low) input.
CVREF		O	Analog	Analog comparator reference output.
RA3/AN3/VREF+	5			
RA3		I/O	TTL	Digital I/O.
AN3		I	Analog	Analog input 3.
VREF+		I	Analog	A/D reference voltage (high) input.
RA4/T0CKI/C1OUT/RCV	6			
RA4		I/O	ST	Digital I/O.
T0CKI		I	ST	Timer0 external clock input.
C1OUT		O	—	Comparator 1 output.
RCV		I	TTL	External USB transceiver RCV input.
RA5/AN4/$\overline{SS}$/ HLVDIN/C2OUT	7			
RA5		I/O	TTL	Digital I/O.
AN4		I	Analog	Analog input 4.
$\overline{SS}$		I	TTL	SPI slave select input.
HLVDIN		I	Analog	High/Low-Voltage Detect input.
C2OUT		O	—	Comparator 2 output.
RA6	—	—	—	See the OSC2/CLKO/RA6 pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

TABLE 1-2: PIC18F2455/2550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	PDIP, SOIC			
RB0/AN12/INT0/FLT0/ SDI/SDA	21			PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0		I/O	TTL	Digital I/O.
AN12		I	Analog	Analog input 12.
INT0		I	ST	External interrupt 0.
FLT0		I	ST	PWM Fault input (CCP1 module).
SDI		I	ST	SPI data in.
SDA		I/O	ST	I^2C™ data I/O.
RB1/AN10/INT1/SCK/ SCL	22			
RB1		I/O	TTL	Digital I/O.
AN10		I	Analog	Analog input 10.
INT1		I	ST	External interrupt 1.
SCK		I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL		I/O	ST	Synchronous serial clock input/output for I^2C mode.
RB2/AN8/INT2/VMO	23			
RB2		I/O	TTL	Digital I/O.
AN8		I	Analog	Analog input 8.
INT2		I	ST	External interrupt 2.
VMO		O	—	External USB transceiver VMO output.
RB3/AN9/CCP2/VPO	24			
RB3		I/O	TTL	Digital I/O.
AN9		I	Analog	Analog input 9.
CCP2(1)		I/O	ST	Capture 2 input/Compare 2 output/PWM 2 output.
VPO		O	—	External USB transceiver VPO output.
RB4/AN11/KBI0	25			
RB4		I/O	TTL	Digital I/O.
AN11		I	Analog	Analog input 11.
KBI0		I	TTL	Interrupt-on-change pin.
RB5/KBI1/PGM	26			
RB5		I/O	TTL	Digital I/O.
KBI1		I	TTL	Interrupt-on-change pin.
PGM		I/O	ST	Low-Voltage ICSP™ Programming enable pin.
RB6/KBI2/PGC	27			
RB6		I/O	TTL	Digital I/O.
KBI2		I	TTL	Interrupt-on-change pin.
PGC		I/O	ST	In-Circuit Debugger and ICSP programming clock pin.
RB7/KBI3/PGD	28			
RB7		I/O	TTL	Digital I/O.
KBI3		I	TTL	Interrupt-on-change pin.
PGD		I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input
CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
I = Input
O = Output
P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.
2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

TABLE 1-2: PIC18F2455/2550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	PDIP, SOIC			
RC0/T1OSO/T13CKI	11			PORTC is a bidirectional I/O port.
RC0		I/O	ST	Digital I/O.
T1OSO		O	—	Timer1 oscillator output.
T13CKI		I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2/$\overline{UOE}$	12			
RC1		I/O	ST	Digital I/O.
T1OSI		I	CMOS	Timer1 oscillator input.
CCP2(2)		I/O	ST	Capture 2 input/Compare 2 output/PWM 2 output.
$\overline{UOE}$		—	—	External USB transceiver $\overline{OE}$ output.
RC2/CCP1	13			
RC2		I/O	ST	Digital I/O.
CCP1		I/O	ST	Capture 1 input/Compare 1 output/PWM 1 output.
RC4/D-/VM	15			
RC4		I	TTL	Digital input.
D-		I/O	—	USB differential minus line (input/output).
VM		I	TTL	External USB transceiver VM input.
RC5/D+/VP	16			
RC5		I	TTL	Digital input.
D+		I/O	—	USB differential plus line (input/output).
VP		O	TTL	External USB transceiver VP input.
RC6/TX/CK	17			
RC6		I/O	ST	Digital I/O.
TX		O	—	EUSART asynchronous transmit.
CK		I/O	ST	EUSART synchronous clock (see RX/DT).
RC7/RX/DT/SDO	18			
RC7		I/O	ST	Digital I/O.
RX		I	ST	EUSART asynchronous receive.
DT		I/O	ST	EUSART synchronous data (see TX/CK).
SDO		O	—	SPI data out.
RE3	—	—	—	See $\overline{MCLR}$/VPP/RE3 pin.
VUSB	14	O	—	Internal USB 3.3V voltage regulator.
VSS	8, 19	P	—	Ground reference for logic and I/O pins.
VDD	20	P	—	Positive supply for logic and I/O pins.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

PIC18F2455/2550/4455/4550
Data Sheet

28/40/44-Pin, High-Performance, Enhanced Flash, USB Microcontrollers with nanoWatt Technology

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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ISO/TS 16949:2002

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MICROCHIP PIC18F2455/2550/4455/4550

28/40/44-Pin, High-Performance, Enhanced Flash, USB Microcontrollers with nanoWatt Technology

Universal Serial Bus Features:

- USB V2.0 Compliant
- Low Speed (1.5 Mb/s) and Full Speed (12 Mb/s)
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- Supports up to 32 Endpoints (16 bidirectional)
- 1-Kbyte Dual Access RAM for USB
- On-Chip USB Transceiver with On-Chip Voltage Regulator
- Interface for Off-Chip USB Transceiver
- Streaming Parallel Port (SPP) for USB streaming transfers (40/44-pin devices only)

Power-Managed Modes:

- Run: CPU on, peripherals on
- Idle: CPU off, peripherals on
- Sleep: CPU off, peripherals off
- Idle mode currents down to 5.8 μA typical
- Sleep mode currents down to 0.1 μA typical
- Timer1 Oscillator: 1.1 μA typical, 32 kHz, 2V
- Watchdog Timer: 2.1 μA typical
- Two-Speed Oscillator Start-up

Flexible Oscillator Structure:

- Four Crystal modes, including High Precision PLL for USB
- Two External Clock modes, up to 48 MHz
- Internal Oscillator Block:
  - 8 user-selectable frequencies, from 31 kHz to 8 MHz
  - User-tunable to compensate for frequency drift
- Secondary Oscillator using Timer1 @ 32 kHz
- Dual Oscillator options allow microcontroller and USB module to run at different clock speeds
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if any clock stops

Peripheral Highlights:

- High-Current Sink/Source: 25 mA/25 mA
- Three External Interrupts
- Four Timer modules (Timer0 to Timer3)
- Up to 2 Capture/Compare/PWM (CCP) modules:
  - Capture is 16-bit, max. resolution 5.2 ns (TCY/16)
  - Compare is 16-bit, max. resolution 83.3 ns (TCY)
  - PWM output: PWM resolution is 1 to 10-bit
- Enhanced Capture/Compare/PWM (ECCP) module:
  - Multiple output modes
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart
- Enhanced USART module:
  - LIN bus support
- Master Synchronous Serial Port (MSSP) module supporting 3-wire SPI (all 4 modes) and I²C™ Master and Slave modes
- 10-bit, up to 13-channel Analog-to-Digital Converter module (A/D) with Programmable Acquisition Time
- Dual Analog Comparators with Input Multiplexing

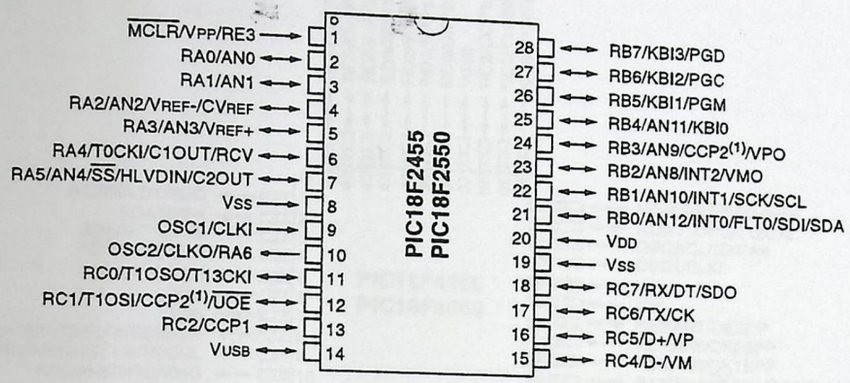
Special Microcontroller Features:

- C Compiler Optimized Architecture with optional Extended Instruction Set
- 100,000 Erase/Write Cycle Enhanced Flash Program Memory typical
- 1,000,000 Erase/Write Cycle Data EEPROM Memory typical
- Flash/Data EEPROM Retention: > 40 years
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 41 ms to 131s
- Programmable Code Protection
- Single-Supply 5V In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug (ICD) via two pins
- Optional dedicated ICD/ICSP port (44-pin devices only)
- Wide Operating Voltage Range (2.0V to 5.5V)

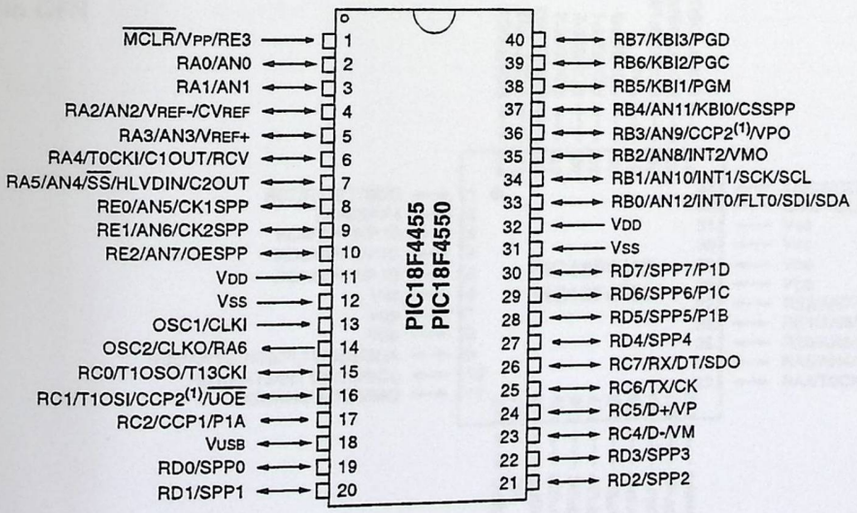
Device	Program Memory		Data Memory		I/O	10-Bit A/D (ch)	CCP/ECCP (PWM)	SPP	MSSP		EAUSART	Comparators	Timers 8/16-Bit
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)					SPI	Master I²C™			
PIC18F2455	24K	12288	2048	256	24	10	2/0	No	Y	Y	1	2	1/3
PIC18F2550	32K	16384	2048	256	24	10	2/0	No	Y	Y	1	2	1/3
PIC18F4455	24K	12288	2048	256	35	13	1/1	Yes	Y	Y	1	2	1/3
PIC18F4550	32K	16384	2048	256	35	13	1/1	Yes	Y	Y	1	2	1/3

Pin Diagrams

28-Pin PDIP, SOIC



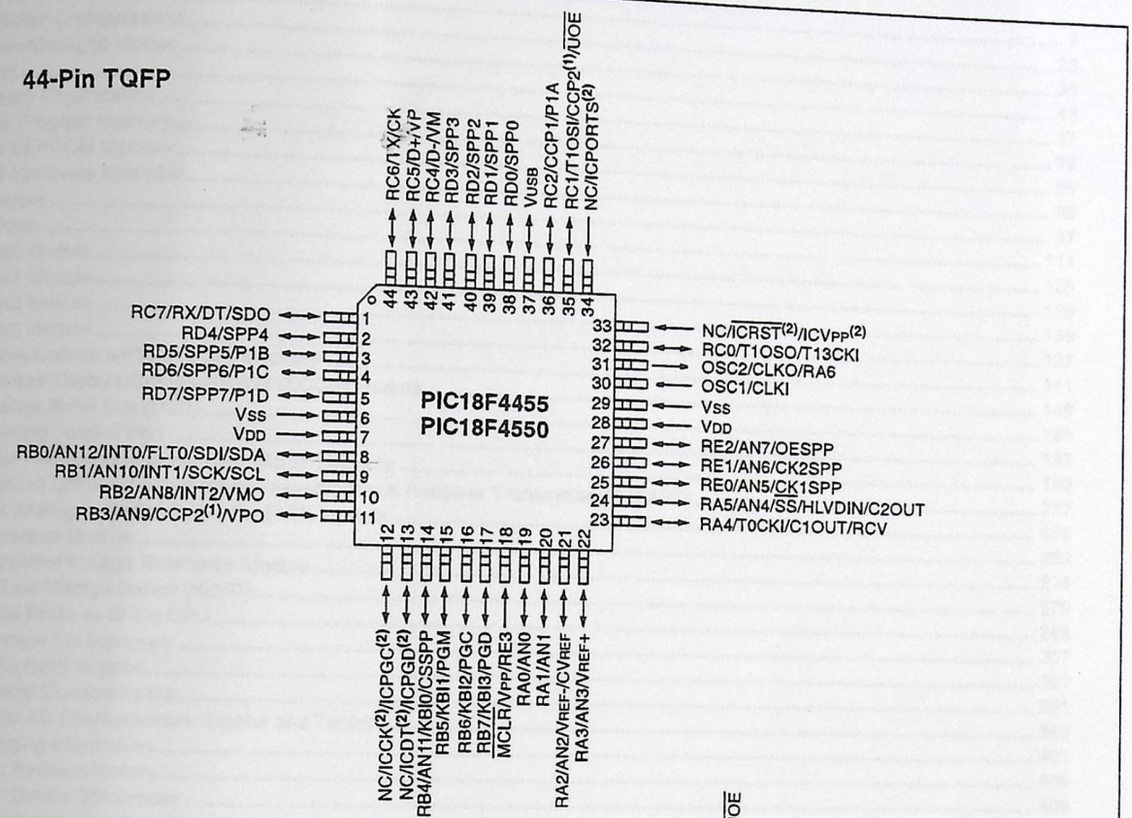
40-Pin PDIP



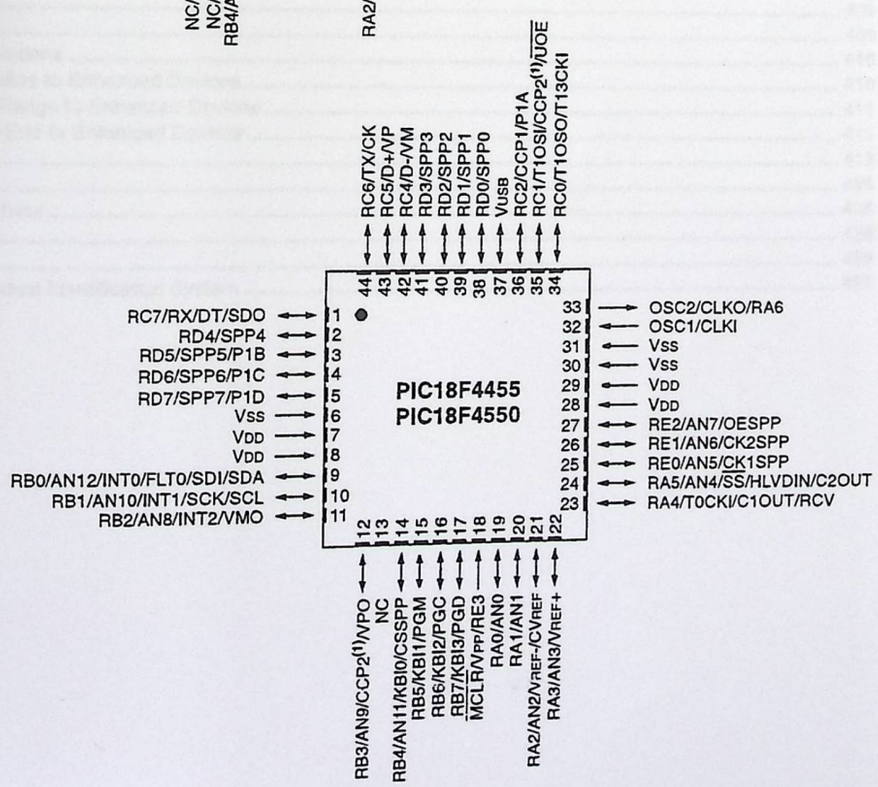
Note 1: RB3 is the alternate pin for CCP2 multiplexing.

Pin Diagrams (Continued)

44-Pin TQFP



44-Pin QFN



Note 1: RB3 is the alternate pin for CCP2 multiplexing.

2: Special ICPORTS features available in select circumstances. See **Section 25.9 "Special ICPORT Features (Designated Packages Only)"** for more information.

Table of Contents

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NOTES:

1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F2455
- PIC18F2550
- PIC18F4455
- PIC18F4550
- PIC18LF2455
- PIC18LF2550
- PIC18LF4455
- PIC18LF4550

This family of devices offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high endurance, Enhanced Flash program memory. In addition to these features, the PIC18F2455/2550/4455/4550 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power sensitive applications.

1.1 New Core Features

1.1.1 nanoWatt TECHNOLOGY

All of the devices in the PIC18F2455/2550/4455/4550 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **Alternate Run Modes:** By clocking the controller from the Timer1 source or the internal oscillator block, power consumption during code execution can be reduced by as much as 90%.
- **Multiple Idle Modes:** The controller can also run with its CPU core disabled but the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operation requirements.
- **On-the-Fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.
- **Low Consumption in Key Modules:** The power requirements for both Timer1 and the Watchdog Timer are minimized. See **Section 28.0 "Electrical Characteristics"** for values.

1.1.2 UNIVERSAL SERIAL BUS (USB)

Devices in the PIC18F2455/2550/4455/4550 family incorporate a fully featured Universal Serial Bus communications module that is compliant with the USB Specification Revision 2.0. The module supports both low-speed and full-speed communication for all supported data transfer types. It also incorporates its own on-chip transceiver and 3.3V regulator and supports the use of external transceivers and voltage regulators.

1.1.3 MULTIPLE OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18F2455/2550/4455/4550 family offer twelve different oscillator options, allowing users a wide range of choices in developing application hardware. These include:

- Four Crystal modes using crystals or ceramic resonators.
- Four External Clock modes, offering the option of using two pins (oscillator input and a divide-by-4 clock output) or one pin (oscillator input, with the second pin reassigned as general I/O).
- An internal oscillator block which provides an 8 MHz clock (±2% accuracy) and an INTRC source (approximately 31 kHz, stable over temperature and V_{DD}), as well as a range of 6 user-selectable clock frequencies, between 125 kHz to 4 MHz, for a total of 8 clock frequencies. This option frees an oscillator pin for use as an additional general purpose I/O.
- A Phase Lock Loop (PLL) frequency multiplier, available to both the High-Speed Crystal and External Oscillator modes, which allows a wide range of clock speeds from 4 MHz to 48 MHz.
- Asynchronous dual clock operation, allowing the USB module to run from a high-frequency oscillator while the rest of the microcontroller is clocked from an internal low-power oscillator.

Besides its availability as a clock source, the internal oscillator block provides a stable reference source that gives the family additional features for robust operation:

- **Fail-Safe Clock Monitor:** This option constantly monitors the main clock source against a reference signal provided by the internal oscillator. If a clock failure occurs, the controller is switched to the internal oscillator block, allowing for continued low-speed operation or a safe application shutdown.
- **Two-Speed Start-up:** This option allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available.

1.2 Other Special Features

- **Memory Endurance:** The Enhanced Flash cells for both program memory and data EEPROM are rated to last for many thousands of erase/write cycles – up to 100,000 for program memory and 1,000,000 for EEPROM. Data retention without refresh is conservatively estimated to be greater than 40 years.
- **Self-Programmability:** These devices can write to their own program memory spaces under internal software control. By using a bootloader routine, located in the protected Boot Block at the top of program memory, it becomes possible to create an application that can update itself in the field.
- **Extended Instruction Set:** The PIC18F2455/2550/4455/4550 family introduces an optional extension to the PIC18 instruction set, which adds 8 new instructions and an Indexed Literal Offset Addressing mode. This extension, enabled as a device configuration option, has been specifically designed to optimize re-entrant application code originally developed in high-level languages such as C.
- **Enhanced CCP Module:** In PWM mode, this module provides 1, 2 or 4 modulated outputs for controlling half-bridge and full-bridge drivers. Other features include auto-shutdown for disabling PWM outputs on interrupt or other select conditions and auto-restart to reactivate outputs once the condition has cleared.
- **Enhanced Addressable USART:** This serial communication module is capable of standard RS-232 operation and provides support for the LIN bus protocol. Other enhancements include Automatic Baud Rate Detection and a 16-bit Baud Rate Generator for improved resolution. When the microcontroller is using the internal oscillator block, the EUSART provides stable operation for applications that talk to the outside world without using an external crystal (or its accompanying power requirement).
- **10-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated, without waiting for a sampling period and thus, reducing code overhead.
- **Dedicated ICD/ICSP Port:** These devices introduce the use of debugger and programming pins that are not multiplexed with other microcontroller features. Offered as an option in select packages, this feature allows users to develop I/O intensive applications while retaining the ability to program and debug in the circuit.

1.3 Details on Individual Family Members

Devices in the PIC18F2455/2550/4455/4550 family are available in 28-pin and 40/44-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in six ways:

1. Flash program memory (24 Kbytes for PIC18FX455 devices, 32 Kbytes for PIC18FX550).
2. A/D channels (10 for 28-pin devices, 13 for 40/44-pin devices).
3. I/O ports (3 bidirectional ports and 1 input only port on 28-pin devices, 5 bidirectional ports on 40/44-pin devices).
4. CCP and Enhanced CCP implementation (28-pin devices have two standard CCP modules, 40/44-pin devices have one standard CCP module and one ECCP module).
5. Streaming Parallel Port (present only on 40/44-pin devices).

All other features for devices in this family are identical. These are summarized in Table 1-1.

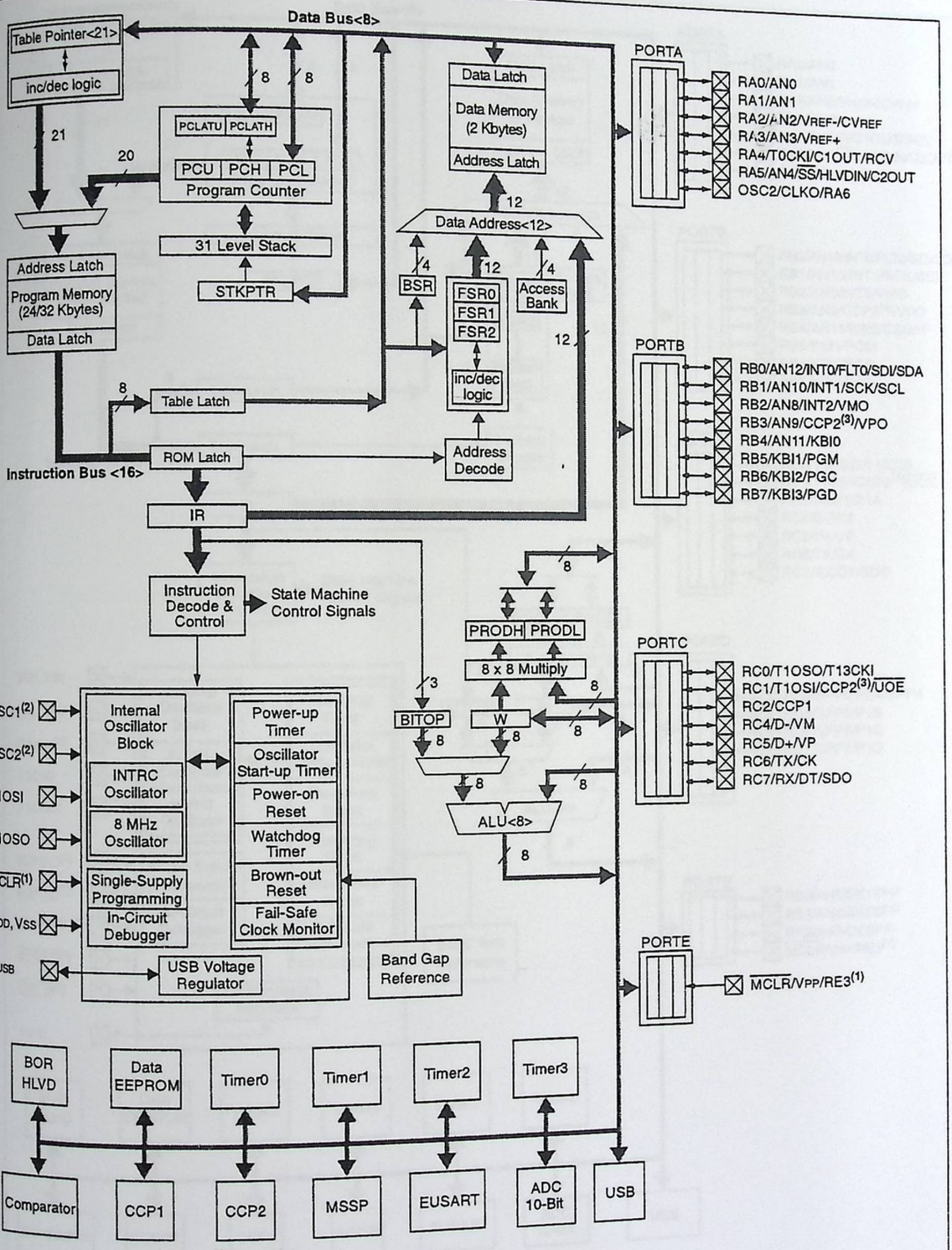
The pinouts for all devices are listed in Table 1-2 and Table 1-3.

Like all Microchip PIC18 devices, members of the PIC18F2455/2550/4455/4550 family are available as both standard and low-voltage devices. Standard devices with Enhanced Flash memory, designated with an "F" in the part number (such as PIC18F2550), accommodate an operating V_{DD} range of 4.2V to 5.5V. Low-voltage parts, designated by "LF" (such as PIC18LF2550), function over an extended V_{DD} range of 2.0V to 5.5V.

TABLE 1-1: DEVICE FEATURES

Features	PIC18F2455	PIC18F2550	PIC18F4455	PIC18F4550
Operating Frequency	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz
Program Memory (Bytes)	24576	32768	24576	32768
Program Memory (Instructions)	12288	16384	12288	16384
Data Memory (Bytes)	2048	2048	2048	2048
Data EEPROM Memory (Bytes)	256	256	256	256
Interrupt Sources	19	19	20	20
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E
Timers	4	4	4	4
Capture/Compare/PWM Modules	2	2	1	1
Enhanced Capture/ Compare/PWM Modules	0	0	1	1
Serial Communications	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART
Universal Serial Bus (USB) Module	1	1	1	1
Streaming Parallel Port (SPP)	No	No	Yes	Yes
10-Bit Analog-to-Digital Module	10 Input Channels	10 Input Channels	13 Input Channels	13 Input Channels
Comparators	2	2	2	2
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), $\overline{MCLR}$ (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), $\overline{MCLR}$ (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), $\overline{MCLR}$ (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), $\overline{MCLR}$ (optional), WDT
Programmable Low-Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled
Packages	28-pin PDIP 28-pin SOIC	28-pin PDIP 28-pin SOIC	40-pin PDIP 44-pin QFN 44-pin TQFP	40-pin PDIP 44-pin QFN 44-pin TQFP

FIGURE 1-1: PIC18F2455/2550 (28-PIN) BLOCK DIAGRAM

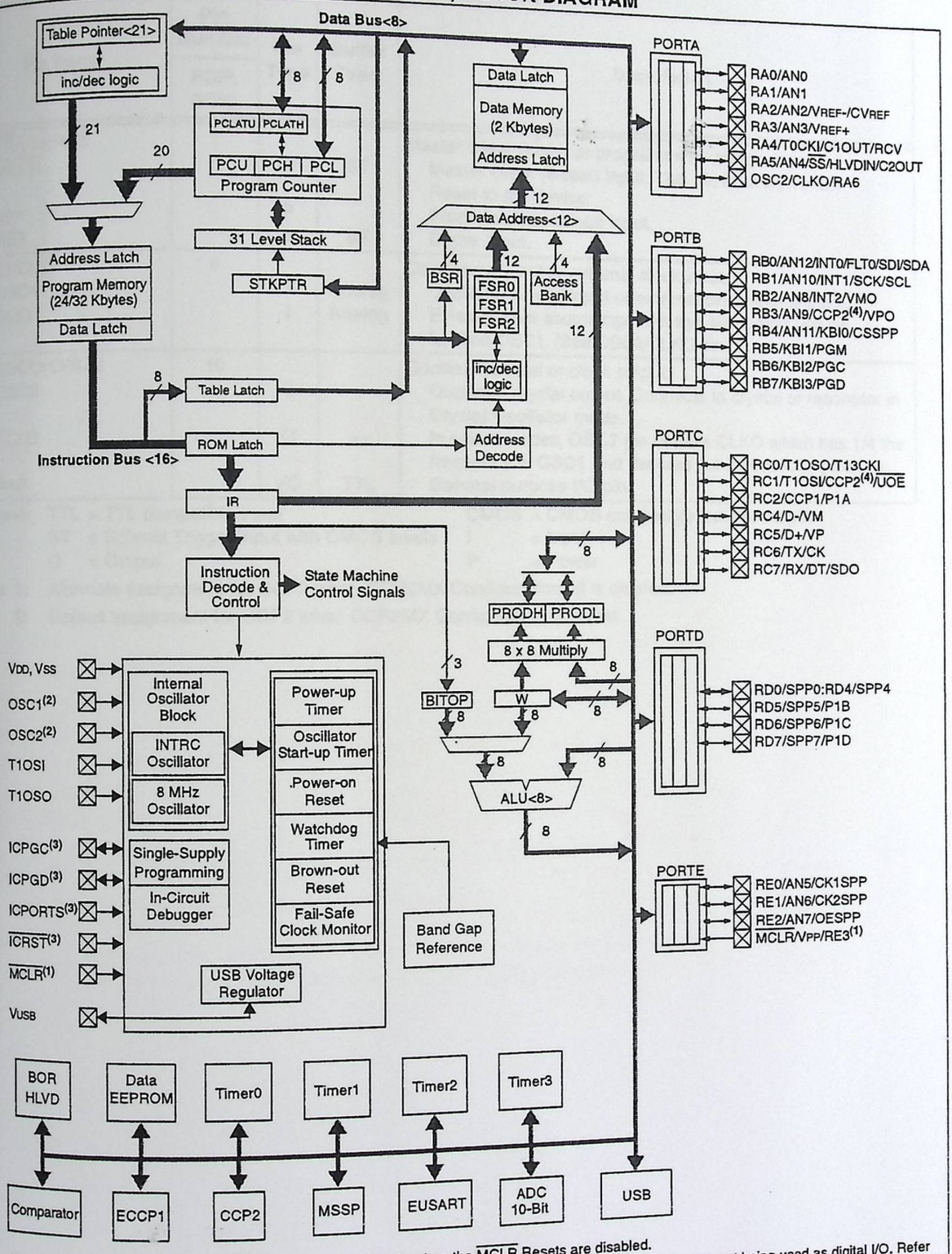


Note 1: RE3 is multiplexed with $\overline{MCLR}$ and is only available when the $\overline{MCLR}$ Resets are disabled.

2: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. Refer to **Section 2.0 "Oscillator Configurations"** for additional information.

3: RB3 is the alternate pin for CCP2 multiplexing.

FIGURE 1-2: PIC18F4455/4550 (40/44-PIN) BLOCK DIAGRAM



Note 1: RE3 is multiplexed with $\overline{\text{MCLR}}$ and is only available when the $\overline{\text{MCLR}}$ Resets are disabled.

2: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. Refer to **Section 2.0 "Oscillator Configurations"** for additional information.

3: These pins are only available on 44-pin TQFP packages under certain conditions. Refer to **Section 25.9 "Special ICPORT Features (Designated Packages Only)"** for additional information.

4: RB3 is the alternate pin for CCP2 multiplexing.

TABLE 1-2: PIC18F2455/2550 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	PDIP, SOIC			
MCLR/VPP/RE3	1			Master Clear (input) or programming voltage (input).
MCLR		I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP		P		Programming voltage input.
RE3		I	ST	Digital input.
OSC1/CLKI	9			Oscillator crystal or external clock input.
OSC1		I	Analog	Oscillator crystal input or external clock source input.
CLKI		I	Analog	External clock source input. Always associated with pin function OSC1. (See OSC2/CLKO pin.)
OSC2/CLKO/RA6	10			Oscillator crystal or clock output.
OSC2		O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO		O	—	In select modes, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6		I/O	TTL	General purpose I/O pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

TABLE 1-2: PIC18F2455/2550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	PDIP, SOIC			
				PORTA is a bidirectional I/O port.
RA0/AN0	2			
RA0		I/O	TTL	Digital I/O.
AN0		I	Analog	Analog input 0.
RA1/AN1	3			
RA1		I/O	TTL	Digital I/O.
AN1		I	Analog	Analog input 1.
RA2/AN2/VREF-/CVREF	4			
RA2		I/O	TTL	Digital I/O.
AN2		I	Analog	Analog input 2.
VREF-		I	Analog	A/D reference voltage (low) input.
CVREF		O	Analog	Analog comparator reference output.
RA3/AN3/VREF+	5			
RA3		I/O	TTL	Digital I/O.
AN3		I	Analog	Analog input 3.
VREF+		I	Analog	A/D reference voltage (high) input.
RA4/T0CKI/C1OUT/RCV	6			
RA4		I/O	ST	Digital I/O.
T0CKI		I	ST	Timer0 external clock input.
C1OUT		O	—	Comparator 1 output.
RCV		I	TTL	External USB transceiver RCV input.
RA5/AN4/$\overline{SS}$/ HLVDIN/C2OUT	7			
RA5		I/O	TTL	Digital I/O.
AN4		I	Analog	Analog input 4.
$\overline{SS}$		I	TTL	SPI slave select input.
HLVDIN		I	Analog	High/Low-Voltage Detect input.
C2OUT		O	—	Comparator 2 output.
RA6	—	—	—	See the OSC2/CLKO/RA6 pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

TABLE 1-2: PIC18F2455/2550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number: PDIP, SOIC	Pin Type	Buffer Type	Description
				PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/AN12/INT0/FLT0/SDI/SDA	21			
RB0		I/O	TTL	Digital I/O.
AN12		I	Analog	Analog input 12.
INT0		I	ST	External interrupt 0.
FLT0		I	ST	PWM Fault input (CCP1 module).
SDI		I	ST	SPI data in.
SDA		I/O	ST	I^2C™ data I/O.
RB1/AN10/INT1/SCK/SCL	22			
RB1		I/O	TTL	Digital I/O.
AN10		I	Analog	Analog input 10.
INT1		I	ST	External interrupt 1.
SCK		I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL		I/O	ST	Synchronous serial clock input/output for I^2C mode.
RB2/AN8/INT2/VMO	23			
RB2		I/O	TTL	Digital I/O.
AN8		I	Analog	Analog input 8.
INT2		I	ST	External interrupt 2.
VMO		O	—	External USB transceiver VMO output.
RB3/AN9/CCP2/VPO	24			
RB3		I/O	TTL	Digital I/O.
AN9		I	Analog	Analog input 9.
CCP2(1)		I/O	ST	Capture 2 input/Compare 2 output/PWM 2 output.
VPO		O	—	External USB transceiver VPO output.
RB4/AN11/KBI0	25			
RB4		I/O	TTL	Digital I/O.
AN11		I	Analog	Analog input 11.
KBI0		I	TTL	Interrupt-on-change pin.
RB5/KBI1/PGM	26			
RB5		I/O	TTL	Digital I/O.
KBI1		I	TTL	Interrupt-on-change pin.
PGM		I/O	ST	Low-Voltage ICSP™ Programming enable pin.
RB6/KBI2/PGC	27			
RB6		I/O	TTL	Digital I/O.
KBI2		I	TTL	Interrupt-on-change pin.
PGC		I/O	ST	In-Circuit Debugger and ICSP programming clock pin.
RB7/KBI3/PGD	28			
RB7		I/O	TTL	Digital I/O.
KBI3		I	TTL	Interrupt-on-change pin.
PGD		I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

TABLE 1-2: PIC18F2455/2550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	PDIP, SOIC			
				PORTC is a bidirectional I/O port.
RC0/T1OSO/T13CKI	11			
RC0		I/O	ST	Digital I/O.
T1OSO		O	—	Timer1 oscillator output.
T13CKI		I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2/$\overline{UOE}$	12			
RC1		I/O	ST	Digital I/O.
T1OSI		I	CMOS	Timer1 oscillator input.
CCP2(2)		I/O	ST	Capture 2 input/Compare 2 output/PWM 2 output.
$\overline{UOE}$		—	—	External USB transceiver $\overline{OE}$ output.
RC2/CCP1	13			
RC2		I/O	ST	Digital I/O.
CCP1		I/O	ST	Capture 1 input/Compare 1 output/PWM 1 output.
RC4/D-/VM	15			
RC4		I	TTL	Digital input.
D-		I/O	—	USB differential minus line (input/output).
VM		I	TTL	External USB transceiver VM input.
RC5/D+/VP	16			
RC5		I	TTL	Digital input.
D+		I/O	—	USB differential plus line (input/output).
VP		O	TTL	External USB transceiver VP input.
RC6/TX/CK	17			
RC6		I/O	ST	Digital I/O.
TX		O	—	EUSART asynchronous transmit.
CK		I/O	ST	EUSART synchronous clock (see RX/DT).
RC7/RX/DT/SDO	18			
RC7		I/O	ST	Digital I/O.
RX		I	ST	EUSART asynchronous receive.
DT		I/O	ST	EUSART synchronous data (see TX/CK).
SDO		O	—	SPI data out.
RE3	—	—	—	See $\overline{MCLR}$/VPP/RE3 pin.
VUSB	14	O	—	Internal USB 3.3V voltage regulator.
VSS	8, 19	P	—	Ground reference for logic and I/O pins.
VDD	20	P	—	Positive supply for logic and I/O pins.

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
O = Output
CMOS = CMOS compatible input or output
I = Input
P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.
2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

National Semiconductor

May 2000

LM78XX
Series Voltage Regulators

General Description

The LM78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expanded to make the LM78XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

Features

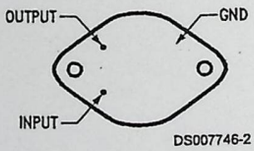
- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

Voltage Range

LM7805C	5V
LM7812C	12V
LM7815C	15V

Connection Diagrams

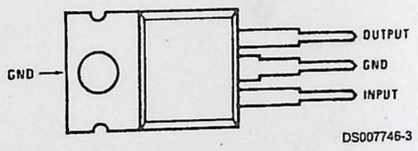
Metal Can Package
TO-3 (K)
Aluminum



DS007746-2

Bottom View
Order Number LM7805CK,
LM7812CK or LM7815CK
See NS Package Number KC02A

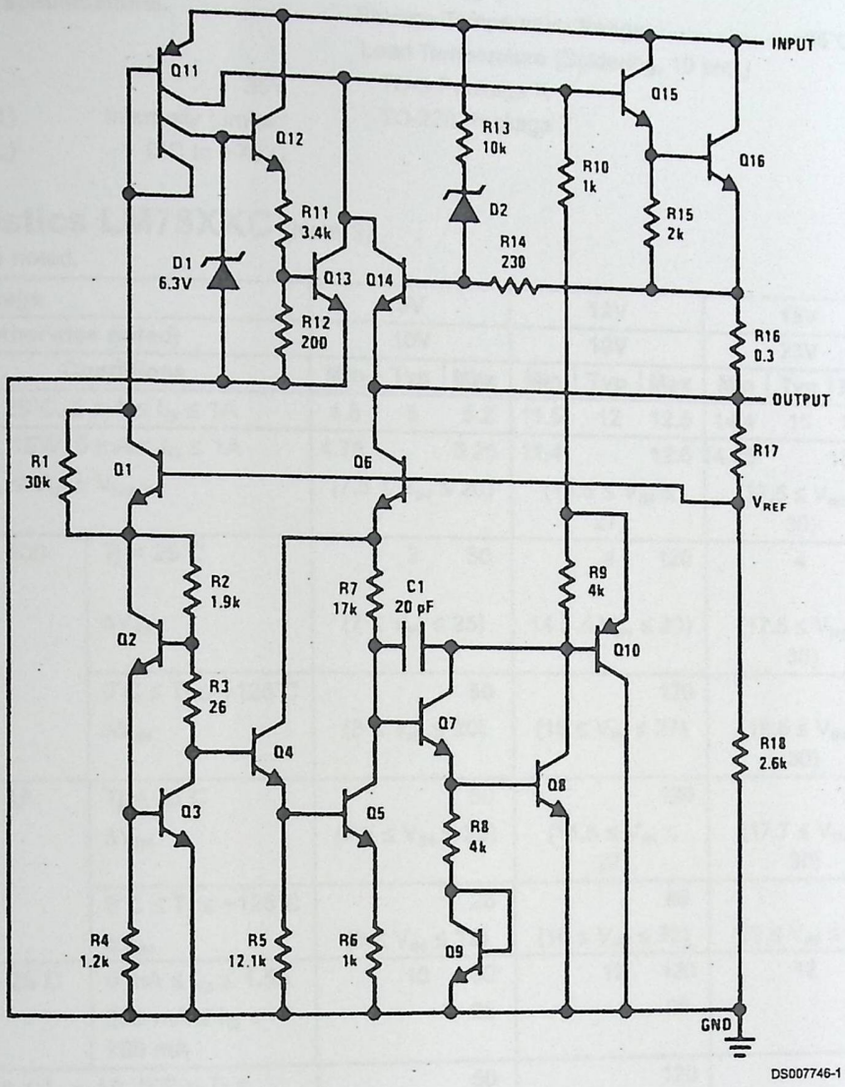
Plastic Package
TO-220 (T)



DS007746-3

Top View
Order Number LM7805CT,
LM7812CT or LM7815CT
See NS Package Number T03B

Schematic


INPUT
Q11
Q12
Q15
Q16
R13
10k
R10
1k
R15
2k
D2
R14
230
R11
3.4k
D1
6.3V
Q13
Q14
R12
200
R16
0.3
OUTPUT
R17
R1
30k
Q1
Q6
VREF
R2
1.9k
R7
17k
C1
20 pF
R9
4k
Q2
Q10
R3
26
Q7
R18
2.6k
Q4
Q8
Q3
Q5
R8
4k
R4
1.2k
R5
12.1k
R6
1k
Q9
GND
DS007746-1

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Voltage (V_O = 5V, 12V and 15V)	35V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range (T_A)	0°C to +70°C
Maximum Junction Temperature	
(K Package)	150°C
(T Package)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	
TO-3 Package K	300°C
TO-220 Package T	230°C

Electrical Characteristics LM78XXC (Note 2)

0°C ≤ T_J ≤ 125°C unless otherwise noted.

Output Voltage				5V			12V			15V			Units
Input Voltage (unless otherwise noted)				10V			19V			23V			
Symbol	Parameter	Conditions		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_O	Output Voltage	Tj = 25°C, 5 mA ≤ I_O ≤ 1A		4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		P_D ≤ 15W, 5 mA ≤ I_O ≤ 1A, V_{MIN} ≤ V_{IN} ≤ V_{MAX}		4.75 (7.5 ≤ V_{IN} ≤ 20)		5.25	11.4 (14.5 ≤ V_{IN} ≤ 27)		12.6	14.25 (17.5 ≤ V_{IN} ≤ 30)		15.75	V V
ΔV_O	Line Regulation	I_O = 500 mA	Tj = 25°C		3	50		4	120		4	150	mV
			ΔV_{IN}	(7 ≤ V_{IN} ≤ 25)			14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			V
			0°C ≤ Tj ≤ +125°C ΔV_{IN}	(8 ≤ V_{IN} ≤ 20)		50	(15 ≤ V_{IN} ≤ 27)		120	(18.5 ≤ V_{IN} ≤ 30)		150	mV V
		I_O ≤ 1A	Tj = 25°C ΔV_{IN}	(7.5 ≤ V_{IN} ≤ 20)		50	(14.6 ≤ V_{IN} ≤ 27)		120	(17.7 ≤ V_{IN} ≤ 30)		150	mV V
			0°C ≤ Tj ≤ +125°C ΔV_{IN}	(8 ≤ V_{IN} ≤ 12)		25	(16 ≤ V_{IN} ≤ 22)		60	(20 ≤ V_{IN} ≤ 26)		75	mV V
ΔV_O	Load Regulation	Tj = 25°C	5 mA ≤ I_O ≤ 1.5A		10	50		12	120		12	150	mV
			250 mA ≤ I_O ≤ 750 mA			25			60			75	mV
		5 mA ≤ I_O ≤ 1A, 0°C ≤ Tj ≤ +125°C				50			120			150	mV
I_Q	Quiescent Current	I_O ≤ 1A	Tj = 25°C			8			8			8	mA
			0°C ≤ Tj ≤ +125°C			8.5			8.5			8.5	mA
ΔI_Q	Quiescent Current Change	5 mA ≤ I_O ≤ 1A				0.5			0.5			0.5	mA
		Tj = 25°C, I_O ≤ 1A, V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7.5 ≤ V_{IN} ≤ 20)		1.0	(14.8 ≤ V_{IN}≤ 27)		1.0	(17.9 ≤ V_{IN} ≤ 30)		1.0	mA V
		I_O ≤ 500 mA, 0°C ≤ Tj ≤ +125°C, V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7 ≤ V_{IN} ≤ 25)		1.0	(14.5 ≤ V_{IN}≤ 30)		1.0	(17.5 ≤ V_{IN} ≤ 30)		1.0	mA V
V_N	Output Noise Voltage	T_A =25°C, 10 Hz ≤ f ≤ 100 kHz			40			75			90		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz	I_O ≤ 1A, Tj = 25°C or	62	80		55	72		54	70		dB
			I_O ≤ 500 mA 0°C ≤ Tj ≤ +125°C	62			55			54			dB
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(8 ≤ V_{IN} ≤ 18)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)			V
R_O	Dropout Voltage	Tj = 25°C, I_{OUT} = 1A			2.0			2.0			2.0		V
	Output Resistance	f = 1 kHz			8			18			19		mΩ