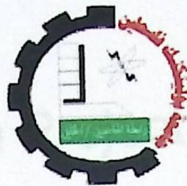


PALESTINE POLYTECHNIC UNIVERSITY



COLLEGE OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

GRADUATION PROJECT REPORT

INFRARED NET BASED TOUCH SCREEN

Researched by:

ANAS AL BAKRI MOHAMMAD AL QAISI
WALEED DAHMAN

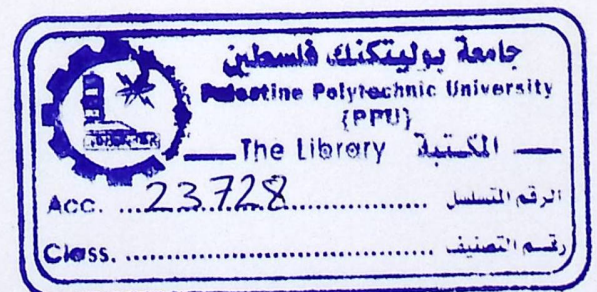
Supervisor:

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HEBRON - PALESTINE

May, 2007

I



PALESTINE POLYTECHNIC UNIVERSITY
Hebron-Palestine
COLLEGE OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

Graduation Project Evaluation
INFRARED NET BASED TOUCH SCREEN

Researched by:

ANAS AL BAKRI MOHAMMAD AL QAISI WALEED DAHMAN

According to the system of the College of Engineering and Technology, and to the recommendation of the Project Supervisor and with agreement of the testing group, this project is presented to Electrical and Computer Engineering Department as a part of requirements of B.Sc. degree in Electrical Engineering – Computer Systems Engineering.

Project Supervisor signature

.....

Testing Group signature

.....

Department Headmaster signature

.....

Dedication

To our mothers

To our fathers

To our brothers and sisters

To our teachers

To our friends

To every one who helped us

To whom we love

We dedicate our humble effort

Project team

Abstract

Touch screens are input devices that allow users to interact easily with PC through finger touches on the screen surface. Touch screen was used in many applications of real life, because of its flexibility, efficiency, ease of use and high response; It became one of the most widely used input devices today.

Our project is building a touch screen that is dependent on the infrared technology; the screen we created is an infrared aluminum frame that contains a group of senders and receivers, such that there will be a net of infrared beams over the screen surface that will be blocked when receiving a touch. We connected this frame with an interfacing circuit that is controlled by the PC through the parallel port. A software driver installed will be responsible for monitoring the frame by sending control signals to the interfacing circuit and scan the receivers in the frame to detect the touch on the screen.

The system worked correctly in most cases. The infrared frame was connected to an interfacing circuit and then to the PC, we received touches on the screen surface and correctly determine the touch position. As a final result, we have succeeded in achieving the actions of click, double click, scroll and right click actions.

Acknowledgment

We would like to thank every one who helped us to complete this project, and to appreciate all the encouragements of our families and friends.

We would like specially to thank:

- ❖ Eng. Amal Al Dweik Wazwaz, Project Supervisor, for her efforts.
- ❖ Mr. Ra'ed Abu Markhyya
- ❖ Eng. Marwan Al Hashlamoon
- ❖ Eng. Sami Al Salameen
- ❖ Rasmi Sied- Ahmad

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Chapter One

Introduction

1.1 Overview

1.2 General Idea of the System

1.3 Literature Review

1.4 Human Resources

1.5 Estimated Cost

1.6 Time Schedule

1.7 Risk Management

1.8 Report Contents

1.10 Summary

Chapter One

Introduction

1.1 Overview

In the last few years we were in a huge technology evolution in both software and hardware that focuses on improvements of the speed, efficiency, flexibility and time after all. The new developed applications came out with a problem that lies in the inflexibility of most used input devices (mouse and keyboard) to support such applications for unskilled users.

Hardware developers solved such problem by creating a very interactive technology which is a screen that requires the users to only touch on it with their fingers or using the so called "Stylus" which looks like a pen to use the screen and click on whatever they want.

Various technologies used to build touch screens which resulted in different kinds and also levels of flexibility, efficiency and accuracy. A special kind of touch screens was designed as only a frame that can be placed on only usual screen and being connected to the computer with a usual plug, also being supported by compatible software to interact with the screen's hardware.

1.2 General Idea of the System

Several kinds of frame touch screens were created, the main idea of our project is to design a special kind of touch screen that is based on the infrared technology with the supporting software.

There will be a net of face-to-face infrared senders/receivers which are mounted on the frame that lies on the original screen. When the user touches the frame surface, an event will be raised from the hardware by locating the touch location with x and y coordinates, then the PC software will provide a click in the equivalent position on the application. Other services will be provided by the software like right clicking, controlling timing and speed, choosing the preferred configuration for the software, and the user interface to fit with the user's needs.

1.2.1 Project Importance

The field of touch screen technology is a new area of research for us as students. It combines many of the fundamentals we studied for the last five years in both hardware and software. In addition it is an interesting topic to search for and learn about with many details that we can take advantages.

We choose the idea of creating a touch screen because we noticed the importance of the infrared technology in many products in life today such as remote temperature sensing, short-ranged wireless communication, spectroscopy, and weather forecasting; also it allows us to concentrate on the interaction between the software and also the hardware components.

In addition, touch screens are one of the most recent input devices used today with many applications that take advantages of its effectiveness and flexibility.

1.3 Literature Review

In this section we list some of the researches on touch screen technology and what results they came up with.

1- Albinsson, Par-Anders & Zhai, Shumin. (2003). High Precision Touch Screen Interaction. *Computer Human Interaction 2003*, 5. [14]

- Results:

- Explore a series of touch screen methods to obtain higher precision.
- Take-off as a click helps quite a bit, compared to clicking on touch.
- People preferred a simple technique - a zoom menu, though one may lose context of surrounding information while zoomed in.

2- Benko, Hrvoje, Wilson, Andrew D., & Baudisch, Patrick. (2006). Precise Selection Techniques for Multi-Touch Screens. *Computer Human Interaction 2006*. [14]

- Results:

- Compares 5 possible zoom-like techniques for touchscreen usage - ways to be more accurate on smaller buttons.
- Ultimately, a speed/zoom menu, a slider-control, and a two-finger zoom proved better than a simple offset, which allows the cursor to be separated from fingers.
- Also contribute SimPress, a clicking technique done by rocking the finger (and temporarily increasing touching surface).
- Two-finger zoom worked best and was most preferred.

3- Leahy, Michael & Hix, Deborah. (1990). Effect of Touch Screen Target Location on User Accuracy. *Proceedings of the Human Factors Society 34th Annual Meeting - 1990*. [14]

-Results:

- Studied accuracy of touchscreen responses given the location of a target onscreen and horizontal angle of viewing.
- Found users generally touch below targets.
- Findings from seating parallax aren't made entirely clear.

1.4 Human Development Resource

The team of the project consists of a three electrical and computer engineering students.

Project Team:

Anas Al Bakri

Mohammad Al Qaisi

Waleed Dahman

Supervisor:

Eng. Amal Al-Dweik

1.5 Estimated Cost

The following table specifies the estimated total costs for the different components in the project.

Number	Object	Cost(Total)\$
1	IR Sender	20
2	IR Receiver	24
3	Decoder	5
4	Analog to Digital Converter	40
5	Inverter	4

6	Clock Generator	2
7	Frame	35
8	WindowsXp(Rent)	25
9	Visual Studio 2005	25
10	Connections and Board	50
11	Buffer	5
12	Tools	30
11	Printing	50
Total		315

Table 1.1: Estimated cost of project components.

1.6 Time Schedule

In the following tables we view the stages in designing and building the components of the project and the timing for each stage.

ID	Task Name	Start	Finish	Duration	Sep 2006	Oct 2006				Nov 2006				Dec 2006			
					9/24	10/1	10/8	10/15	10/22	10/29	11/5	11/12	11/19	11/26	12/3	12/10	
1	Idea Decision	09/20/2006	09/26/2006	1w	[Gantt bar from 9/20 to 9/26]												
2	Full Description	09/27/2006	10/10/2006	2w	[Gantt bar from 9/27 to 10/10]												
3	Study	10/11/2006	11/28/2006	7w	[Gantt bar from 10/11 to 11/28]												
4	Primary Design	11/08/2006	11/28/2006	3w	[Gantt bar from 11/08 to 11/28]												
5	Primary Implementation	11/21/2006	12/11/2006	3w	[Gantt bar from 11/21 to 12/11]												
6	Revision	12/07/2006	12/20/2006	2w	[Gantt bar from 12/07 to 12/20]												
7	Documentation	10/19/2006	12/20/2006	9w	[Gantt bar from 10/19 to 12/20]												

Table 1.2: Project scheduling stages and time table for the first semester 2006/2007.

6	Clock Generator	2
7	Frame	35
8	WindowsXp(Rent)	25
9	Visual Studio 2005	25
10	Connections and Board	50
11	Buffer	5
12	Tools	30
11	Printing	50
Total		315

Table 1.1: Estimated cost of project components.

1.6 Time Schedule

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1	Idea Decision	09/20/2006	09/26/2006	1w	▽△												
2	Full Description	09/27/2006	10/10/2006	2w	▽△												
3	Study	10/11/2006	11/28/2006	7w	▽△												
4	Primary Design	11/08/2006	11/28/2006	3w	▽△												
5	Primary Implementation	11/21/2006	12/11/2006	3w	▽△												
6	Revision	12/07/2006	12/20/2006	2w	▽△												
7	Documentation	10/19/2006	12/20/2006	9w	▽△												

Table 1.2: Project scheduling stages and time table for the first semester 2006/2007.

ID	Task Name	Start	Finish	Duration	Feb 2006			Mar 2006			Apr 2006							
					2/5	2/12	2/19	2/26	3/5	3/12	3/19	3/26	4/2	4/9	4/16	4/23	4/30	
1	Hardware Circuit	02/01/2006	04/18/2006	11w	[Gantt bar with triangle at end]													
2	Interfacing Circuit	2/8/2006	03/14/2006	5w	[Gantt bar with triangle at end]													
3	Software Implementation	2/22/2006	04/18/2006	8w	[Gantt bar with triangle at end]													
4	Testing	3/14/2006	5/9/2006	8.2w	[Gantt bar with triangle at end]													
5	Documentation	02/01/2006	5/9/2006	14w	[Gantt bar with triangle at end]													

Table 1.3: Suggested Project scheduling stages and time table for the second semester 2007.

1.7 Risk Management

There are some possible risks that may occur in our project in both hardware and software.

1 - Technology Risks

Such risks may occur because of the software or hardware used in the system.

- Hardware risks:

- Infrared transmitter/receiver Malfunctions.
- Interface connection Malfunctions.
- Unavailability of some hardware component that is required.

- Software risks:

- Incompatibility.
- Problems that might occur with using the software development environment.

2 - People Risks

- Member of the team gets ill.
- Member of the team becomes unavailable for any reason.

3 - Organizational Risks

- Facing financial problems.

- Facing project resources problems.

4 - Tools Risks

- Lose of any supported software or hardware used to develop the system.

5 - Requirements Risks

Risks that might occur if new changes are required in the system requirements that need major changes in the system design, like facing unexpected problems in hardware or software that requires a significant change in the project's requirements.

6 - Estimation Risks

Risks that may derive from the wrong estimation in the system design, implementation, resources and management.

1.6.1 Risk Avoidance

- Taking care when using hardware components and using them according to their specifications.
- Using only compatible software development environment to implement the software.
- Taking care of the team's member's health during the project development.
- Good estimation and usage of the projects budget and resources.
- Good estimation of system requirements.

1.6.2 Risk Management:

- Software development environment risks will be handled by the backup of software.
- Including an extra amount of the hardware components we already have, so when any problem occurs we can find an alternative for the component we lost.

- People risks are handled by using work load balancing on students especially when a member can't perform some of his tasks, then it will be done by other member.
- Tools risks: software and hardware components tools are protected by preparing backups for such components.

1.8 Project's Scope

After completing the main requirements of our project, it can be used in a range of widely used applications:

- Trade show displays.
- Tanning touch screen for unskilled users.
- Restaurants touch screens.
- Touch screen for users with special needs.
- Point of sale touch screens.
- Computerized gaming.
- Vending machines

1.9 Report Contents

Chapter one focuses on the general idea, importance and scope of our project, in addition to the literature review and report's contents, and project planning. The second chapter covers the theoretical background that states the theory of the system, its general explanation for the project's software/hardware components, and also the system requirements.

Chapter three specifies the theoretical design concepts of the infrared net-based touch screen as a system and describes the project's objectives in addition to the system's working method with descriptive block diagrams and the system modeling. Chapter four discusses system design options, detailed description of the different project parts and interfacing circuits.

Chapter five specifies the implementation of our system in hardware and software, then chapter six previews the main stages of testing the project components, at last in chapter seven we state our conclusions, expectations and advisement for the future work on related projects.

1.10 Summary

Chapter one of the Infrared Net Based Touch Screen provides an abstract idea of the whole project in sections starting from the overview which is an introduction to the chapter; the second section is the general idea of the system that creates a brief understanding of the system we build, the third is the revision of the previous work done on related projects through the literature review section.

Section four is an evaluation of the project costs, followed by the indication of the time required to accomplish each task in the project which is the subject of section five, a listing of the possible risks in the project and how they are going to be handled are described in the risk management section.

Section seven is a listing of the applications that may take advantage of our system, followed by a specification of the whole report contents in section eight.

Chapter Two

Theoretical Background

2.1 Overview

2.2 System Requirements

2.3 Theoretical Background

2.4 Hardware Components

2.5 Software Components

2.6 Summary

2.2 System Requirements

This section is a listing of the main requirements that must be met in our project in order to get the main services that will be provided.

2.2.1 User Requirements

This section views the system requirements for the touch screen's users.

1- Functional Requirements

1- The frame will be assumed in front of the usual screen for the user to touch on.

Chapter Two

Theoretical Background

2.1 Overview

This chapter describes the theory of the touch screen technology in general, by describing the general idea of each technology. In addition, it will view the requirements of our system, and also it lists the main components that will be used in both software and hardware.

2.2 System Requirements

This section is a listing of the main requirements that must be met in our project in order to set the main services that will be provided.

2.2.1 User Requirements

This section views the system requirements for the touch screen's users.

1- Functional Requirements

1- The frame will be mounted in front of the usual screen for the user to touch on.

- 2- The software driver will provide the user with a graphical user interface that allows him/her to change the screen settings and set his/her own configurations for hardware and software options.
- 3- The user will touch anywhere on the screen surface and an equivalent click will be provided on the application by software.
- 4- The touch screen will ignore multiple touches and accept only one touch.
- 5- The touch screen will provide the user with all mouse services including right clicking and scrolling.
- 6- The touch screen software will be implemented to run under WindowsXp operating system.
- 7- Recommended resolution is 600x800.

2- Non- Functional Requirements

Non-functional requirements are divided into two categories:

2.1 Product Requirements

For the touch screen to satisfy the product requirements, it should have the following:

- Flexibility

The touch screen will provide the user with a higher flexibility of usage than that provided using traditional input devices like mouse, especially for users with disabilities, such it can be used by users with different skills that ranges from the unskilled to the advanced and professional users.

- Speed

The use of touch screen will increase the speed of user's interaction with different applications, such that the direct touching on the screen is faster than other input devices in satisfying user's needs.

- Ease of use

The touch screen will be easy to use; the user just clicks the location he/she wants on the screen.

-Accuracy

The touch screen must be accurate and take the action on the screen where the user wanted it to happen.

- Efficiency

The touch screen solves the problems of other input devices, such that it will save time and effort especially when using application that requires too much user's interaction.

- Software capabilities

The software driver gives the user the ability to set his preferred options according to the interaction with the screen and also choose the best configuration.

- Mobility

Our screen is a lightweight input device and can be moved easily from one PC to another.

2.2 External Requirements

The spread of touch screens will not replace the usage of other traditional input devices and so results in a lose to the companies producing such devices, because each kind of input devices have a set of applications that it best serve, so there will be a balance in spreading the use of different input devices on the various kinds of user applications.

2.2.2 System Requirements

These are the set of requirements that specify the system details and specification from the developer's point of view.

1- Functional Requirements

- 1- The touch screen frame will contain a net of face-to-face infrared transmitters and receivers that will receive the user touch as input by producing an infrared beam net over the screen's surface.
- 2- The infrared net will be monitored repeatedly by an interfacing circuit consisting of analog to digital converters and analog multiplexers controlled by the PC which will detect the touch on the screen when the beam on a random position is blocked.
- 3- The interfacing circuit controlled by the PC will scan the receivers one by one and provide the information necessary for the software to determine the location of the touch,
- 4- The software driver will take an action that is similar to using the mouse as output, depending on the position of the cursor on the screen when the touch occurred.
- 6- All the interfacing communications will be provided using the parallel port.
- 7- The suggested resolution for the desktop of the screen is (600x800 pixels).
- 8- The suggested infrared sensor resolution is (15x21 LEDs).

2- Non-functional Requirements

- 1- Fast response / speed (1 millisecond)

The screen must respond to the user's action within a limited specific amount of time.

- 2- Strong infrared detection

The infrared signal received must not overlay with other kinds of lighting around the screen, and this should not confuse the infrared receivers.

- 3- Reliability

The touch screen must be trusted to respond to the user's touch in the same position where the user touched the screen.

4- Efficiency

The touch screen will be accurate, respond able, fail tolerated, maintainable.

5- Performance

The screen will provide the user with a fast reaction regarding the whole system speed for both the screen's hardware and the PC software.

2.3 Theoretical Background

2.3.1 General Description

A frame touch screen is a frame that is placed in front of usual display screen. It is activated by touching with finger on a specific location which is specified by X and Y coordinates, also the frame has an independent logical X-Y position that is calibrated to be equivalent to the coordinates on the screen. When a click occurs by touching on the screen surface it will be located by an X-Y coordinate. Then a proper action will be taken in a way that is similar to the action that is caused by a mouse click.

Touch screen characteristics:

- 1- Video display equivalent resolution.
- 2- It would be activated by
 - Conducting or non-conducting stylus.
 - A gloved or non-gloved finger.
- 3- It would be modular and capable of being added to a display and computer in the same manner that other input devices are added.
- 4- It would be impervious to dust, grease, moisture chemical or oil vapors or pressure hose down that may be present in a hostile environment. [8]

2.3.2 Major Touch Screen Technologies

The main technologies that are used in touch screens are:

- 1- Analog Resistive
- 2- Capacitive
- 3- Scanning Infrared (IR)
- 4- Surface Acoustic Wave (SAW) [8]

Next we will provide a brief description of each one of these technologies.

2.3.2.1 Analog Resistive

The resistive system consists of a normal glass panel that is covered with a conductive and a resistive metallic layer. These two layers are held apart by spacers, and a scratch-resistant layer is placed on top of the whole setup. An electrical current runs through the two layers while the monitor is operational. When a user touches the screen, the two layers make contact in that exact spot. The change in the electrical field is noted and the coordinates of the point of contact are calculated by the computer. Once the coordinates are known, a special driver translates the touch into something that the operating system can understand. Figure 2.1 illustrates the idea of analog resistive touch screens. [8]

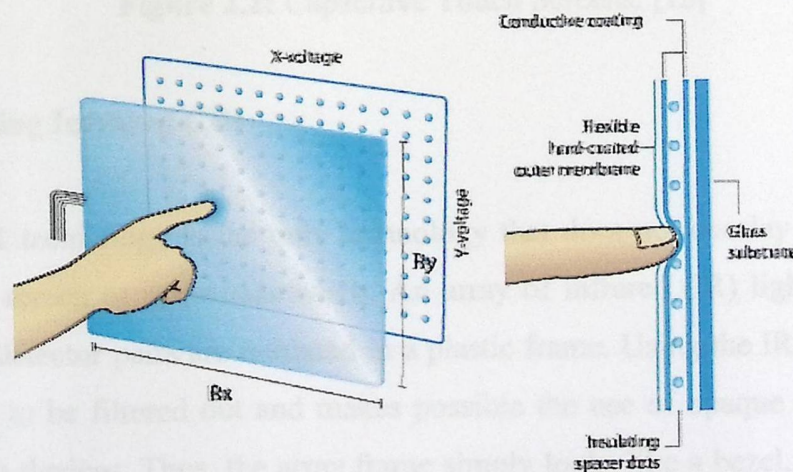


Figure 2.1: Analog Resistive Touch Screens. [15]

2.3.2.2 Capacitive

A glass panel is coated with a conductive coating material that is fused into the glass. The coating is connected to four electrodes at the edges of the screen. Each electrode is connected to an oscillator circuit. When operator touches the screen, the body capacitance of the operator causes a change in the impedance of the screen. The impedance change causes the oscillator frequencies to vary, and the frequency differentials are converted into X-Y coordinates by an A-D converter. Figure 2.2 illustrates the capacitive touch screen. [8]

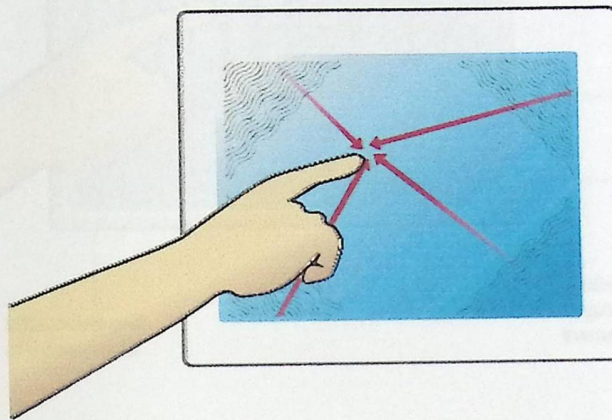


Figure 2.2: Capacitive Touch Screens. [15]

2.3.2.3 Scanning Infrared (IR)

The IR technology is the only technology that does not overlay the display with an additional screen or screen sandwich. An array of infrared (IR) light emitting diode (LED)/photo detector pairs are mounted in a plastic frame. Using the IR spectrum allows ambient light to be filtered out and makes possible the use of opaque plastic frames to hide the photo devices. Thus, the array frame simply looks like a bezel. In operation, the LED/photo detector array is continuously and sequentially scanned horizontally and then vertically when an operator touches the display breaking one or more of the light beams, the X-Y position of the touch stylus is transmitted to the host computer. The maximum resolution using an interpolation technique is approximately double the number of

LED/photo detector pairs in the array. Using interpolation, when an odd number of beams is broken along either axis, the X or Y coordinate of the center beam is transmitted, but when an even number of beams is broken, the coordinates of the interpolated beam are calculated and transmitted to the host computer. Figure 2.3 illustrates the idea of infrared touch screen. [8]

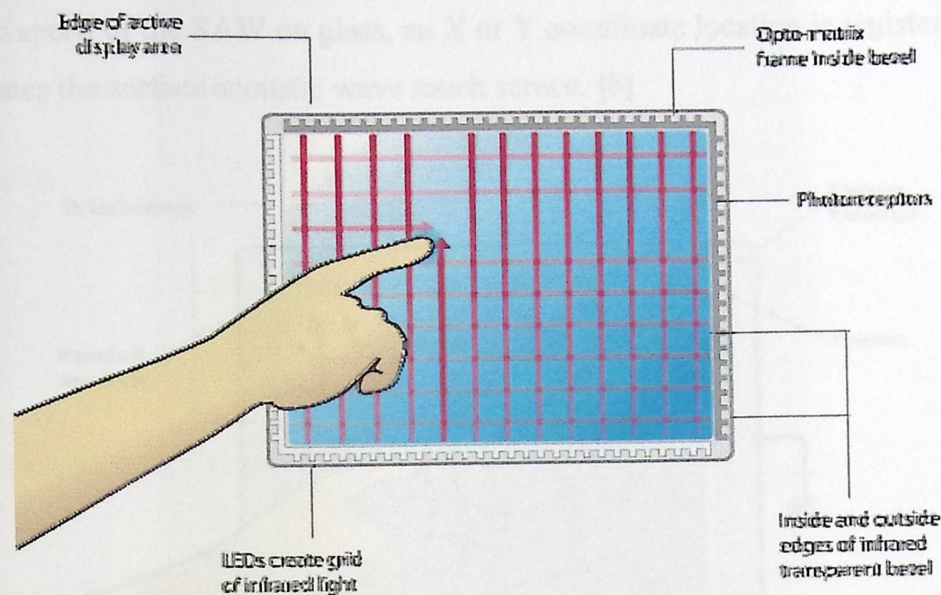


Figure 2.3: Infrared Touch Screens. [15]

2.3.2.4 Surface Acoustic Wave (SAW)

The surface acoustic wave technology is the latest of the touch input technologies and uses inaudible acoustic waves traveling over the surface of a glass panel at precise speeds in straight lines. X and Y transmitting transducers are located along the horizontal and vertical edges of a glass plate. Corresponding X and Y receiving transducers are located at the opposite edges of the glass plate. A reflective array made of powdered glass is printed along the edges of the glass plate. The array consists of .2 mil thick by 1/2 inch wide diagonal, parallel lines. In operation, the transducer generates a surface acoustic wave which travels along the axis of the reflector array. At each reflector element, a small amount of the energy in the wave is deflected orthogonally to the direction of the

wave, travels over the surface of the glass and is again deflected orthogonally toward the receiving transducer by a mirror image reflector. Since the energy in the wave is reduced as it travels the length of the reflective array, the reflector elements are placed increasingly closer together to compensate for the decreasing energy level. When an operator touches the screen, a portion of the energy is absorbed by the touch stylus. This reduced energy level is detected and, by comparing the speed of the received signal with the known speed of the SAW on glass, an X or Y coordinate location is registered. Figure 2.4 illustrates the surface acoustic wave touch screen. [8]

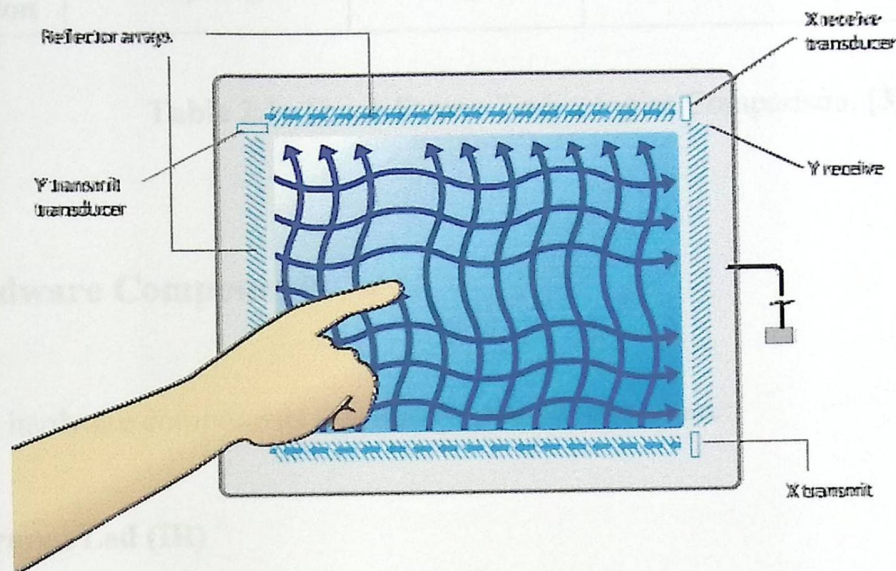


Figure 2.4: Surface Acoustic Wave Touch Screens. [15]

Table 2.1 is a comparison between the different touch screen technologies.

Technology	Capacitive Touch Panel	Resistive Touch Panel	Infrared Touch Panel	SAW Touch Panel
Clarity	85% light transition excellent clarity	75% clear ,good Clarity	90% light transition, Excellent Clarity	90% light transition, excellent Clarity.
Durability	Excellent, contains hardened glass surface which conductive metal oxide.	Good, contains hard coated plastic overlay but can be damaged.	Excellent, contains no overlays, optical sensors around the frame.	Excellent contains no overlays, all glass panels.

Reliability	Very High	High	Very High	Very High
Accuracy, calibration, stability	Very accurate, very stable	Very accurate, very stable	Very accurate, very stable	Extremely consistent, very stable
Activation, sensitivity	Finger contact for touch activation, easily detects contact.	Pressure sensitive. Activated by any object, good for gloved application.	Interruption of the light beam matrix: life to no pressure required.	Soft objects, non glare, require significant contact.
Touch Resolution	Very High	high		

Table 2.1: Touch Screen Technologies Comparison. [3]

2.4 Hardware Components

The main hardware components that our system consists of are:

2.4.1 Infrared Led (IR)

Infrared is an invisible electromagnetic radiation waves that is longer than the visible light and shorter than the radio waves, the name infrared means below red, and red here means the portion of visible light.

Infrared technology has many applications in life today including target acquisition and tracking by in military applications, remote temperature sensing, and short-ranged wireless communication. In our project we can take advantage of this technology to detect the motion above the service of screen. [9]

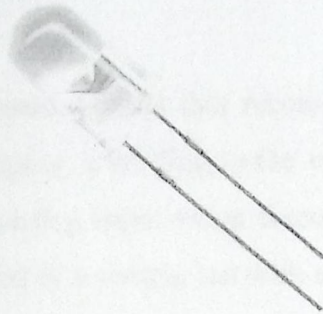


Figure 2.5: Infrared LED

2.4.2 Analog to Digital Converter

Analog to digital converters (ADC's) are integrated circuits that convert the analog input into a digital equivalent, there are many types of ADC's, each one has different features and properties like conversion speed, accuracy and number of inputs.

In our project, the ADC's will be used to read the analog input coming out from each receiver on the frame and convert it into a digital equivalent that will be sent to the PC software to be analyzed.

The kind of ADC that we are going to use is ADC808 Compatible A/D Converter with 8-Channel Analog Multiplexer, these devices have a good advantage of including an inner multiplexer that we need for the interfacing circuit, this kind of multiplexer will be discussed in the next section.

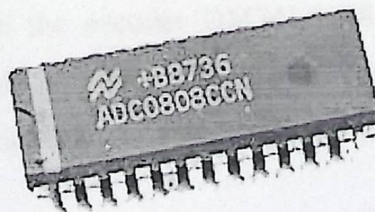


Figure 2.6: Analog to Digital Converter

2.4.3 Analog Multiplexer

These are logical integrated circuits that receive multiple inputs, and contain a group of selection lines and outputs, according to the value on the selection lines, these circuits will pass the selected analog input value through the output and prevent other inputs from passing, so it's a kind of a switch, but with extended capabilities.

The analog multiplexer is the same as the digital multiplexer in that they pass a selected input to the output, they differ only in the kind of input they pass, analog or digital, in our project we need to pass an analog input because the value of the voltage on each receiver is critical and must be read exactly as it is, without conversion or approximation into a digital value.

There is an advantage that is the analog multiplexer used in our project is already included in the ADC's used, so this will decrease the level of hardware complexity in the interfacing circuit.

2.4.4 Decoder

The decoder is a logical IC that is used to enable one of a group of output lines in response to a specific selection on its input lines, such that there is a set of combinations to choose from, and we provide the appropriate input value to enable the output line we need.

In our project we use the decoder DM74LS138 as an enable IC; by using a decoded group of selection lines we can enable one of the analog to digital converters in the interfacing circuit, so the decoder is a kind of chip selector in such case.

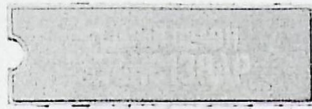


Figure 2.7: Decoder

2.4.5 Inverter

These are logical integrated circuits that are used to invert the logical state of the input line and provide the inverted signal as output.

In our project we use the CD74CHT04 inverter because other IC's has an inverted output that can't be used directly in interfacing with other components, so we use an inverter the invert the signal as we need.

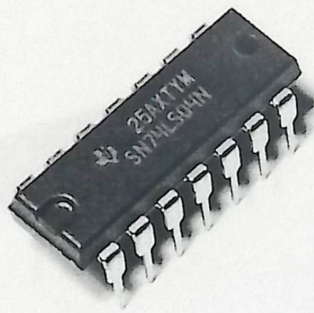


Figure 2.8: Inverter

2.4.6 Clock Generator

This IC is used to generate a clock with a specified frequency, some integrated circuits needs a clock input to work properly, one of these IC's is the analog to digital converter.

In our project we need the 555 clock generator IC to provide a clock signal as input to the analog to digital converters, to enable their conversion process.

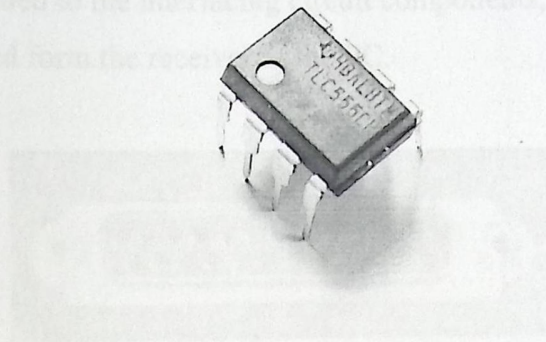


Figure 2.9: Clock Generator

2.4.7 Tri-State Buffer

The buffer is used as an output device that can pass the input signal to its output pins or prevent it from passing (tri-state case), in our project we need the buffers to isolate the each ADC's output from the output of the others, because they are sharing the output lines, and without using buffers this may cause an interference in the signals.

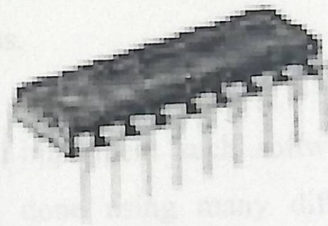


Figure 2.10: Tri-state buffer

2.4.8 Parallel Port

A parallel port is a type of socket found on personal computers for interfacing with various peripherals. It is also known as a printer port or Centronics port.

In our project we use the parallel port as communication mechanism between the PC and the interfacing circuit, such that some of the parallel port lines are used to provide the control signals supplied to the interfacing circuit components, and other lines are used to enter the data received form the receiver to the PC.

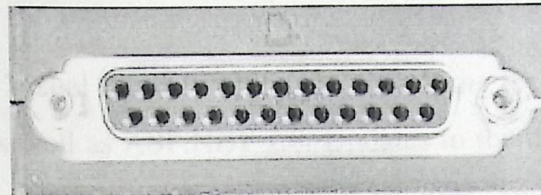


Figure 2.11: Parallel Port

2.5 Software Components

2.5.1 Introduction

The touch screen software will provide the hardware/software interaction mechanism; also it will provide a graphical user interface with many options that the user can set with his preferred options.

In our project we will implement such software to control our screen, this implementation phase can be done using many different application development environments and tools which makes us face a wide range of options that we may take and also with many differences between them in the flexibility, efficiency, time, speed, cost and the resource management with a lot such affecting factors that requires us to make a good decision.

Our software and hardware choices were made to be:

- **Software Environment:** Visual Studio 2005.
- **Hardware Interfacing:** Serial port.

2.5.2 Why Visual Studio 2005?

Next we will state the new features that have been added to VS 2005, and why we choose it as a development environment.

A key aspect of Visual Studio 2005 is the underlying technology, which includes .NET Framework 2.0 as well as ASP.NET 2.0. Updates to the .NET Framework include performance enhancements, many new language features, and stronger Web services support. [5]

2.5.2.1 New features

Here we list a group of new features for which we choose VS 2005 that helps us in programming and building the software of the screen with many capabilities that provides programming flexibility for us and also results with good software.

- 1- Tighter integration with other products allows developers to utilize their skills across a range of products
- 2- Edit and Continue allows developers to edit code in place and continue with execution.
- 3- Click once installation provides a much smoother install process. It allows applications to be installed and updated as opposed to redeploying the entire application.
- 4- Smart Tasks allow easy access to information and common tasks within the IDE.
- 5- Line Revision marks allow to see the changes that have been made during a coding session. Colored lines appear down the left side of the code pane to denote changes and additions.
- 6- The IDE now allows its settings to be exported and imported. This is a welcome addition because it is troublesome to move to a new computer after getting Visual Studio .NET configured as we like it. With a new installation, we can easily import our previous settings and we are good to go.

7- Microsoft IntelliSense code snippets enable developers to easily create and distribute their own customized code libraries. It allows us to develop generic or template code that may easily be reused.

8- There's drag and drop support for working with data sources. [6]

In addition to those features, VS 2005 provides many features for controlling hardware and providing an easy data acquisition, like the large set of API's, libraries, functions and also available tools to allow for full control of hardware by providing many interfacing services.

2.6 Summary

The second chapter increases the understanding the project by introducing a theoretical background about the touch screen technology by a group of sections starting with a chapter overview as the first, then the listing of the system and user requirements which comes in the second section.

The third section titled the theoretical background and as the name indicates is a brief description of the main technologies used in related projects, which is the technologies of the touch screens, follow that the hardware components section that lists the main components of the project's hardware with a brief description.

At last the description of the software development environment, its capabilities, features and usage are specified in the software component section.

Chapter Three

Chapter Three

Architectural Design

Architectural Design

3.1 Overview

3.2 System Objectives

3.3 System Block Diagram

3.4 How Does the System Work?

3.5 System Modeling

3.6 Summary

3.2 System Objectives

The main objectives in our project are:

- 1- Build an infrared based touch screen that receives a finger touch on the screen's surface and do the appropriate action.
- 2- Build an infrared based net that is mounted on a frame on a device that is connected to the interfacing circuit.
- 3- Building the main interfacing circuit including the analog to digital converters, multiplexers, decoder, clock generator and inverter.
- 4- Connecting the interfacing circuit with the PC using the parallel port.
- 5- Implementing the software that communicates with the hardware and provides the user's services.

Chapter Three

Architectural Design

3.1 Overview

This chapter focuses on the main design concepts in the infrared net based touch screen, lists the detailed system objectives, and describes the main components of the system using block diagrams to show how these components are connected with each other. Also in this chapter we will discuss the main architecture of the system, how it works, and how it is modeled.

3.2 System Objectives

The main objectives in our project are:

- 1- Build an infrared based touch screen that receives a finger touch on the screen's surface and do the appropriate action.
- 2- Build an infrared based net that is mounted on a frame on a circuit that is connected to the interfacing circuit.
- 3- Building the main interfacing circuit including the analog to digital converters, multiplexers, decoder, clock generator and inverter.
- 4- Connecting the interfacing circuit with the PC using the parallel port.
- 5- Implementing the software that communicates with the hardware and provides the user's services.

3.3 System Block Diagram

The following block diagram indicates the general idea of the system:

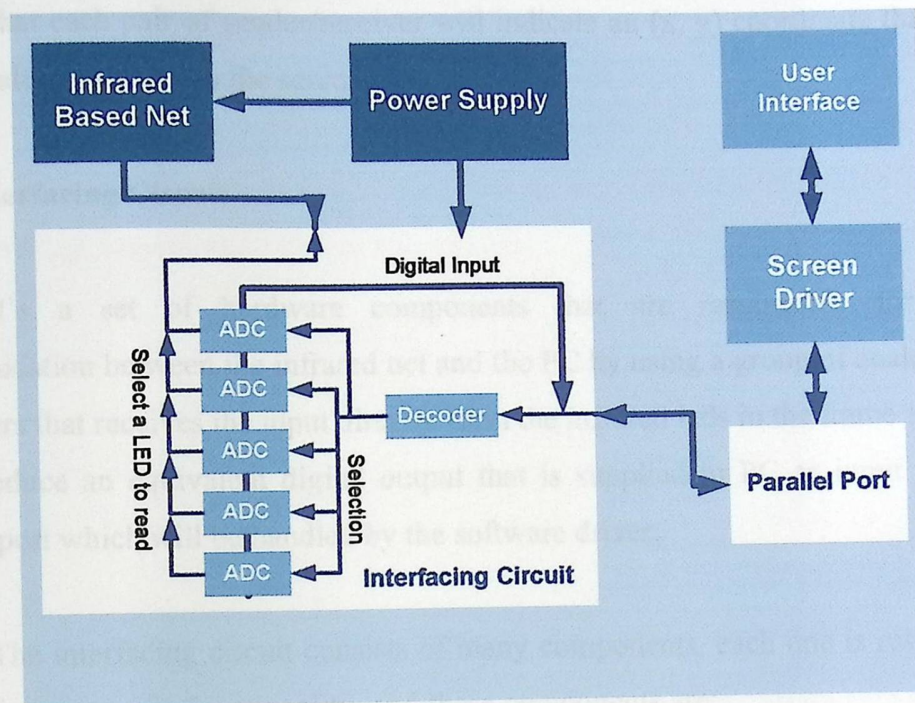


Figure 3.1: Overall System Block Diagram

3.3.1 Power Supply

This unit is used to provide the power supply required for enabling the net of infrared transmitters/receivers and the interfacing circuit components, the power supply used for the infrared net is a high voltage power supply because of the high power consumption caused by the infrared senders.

3.3.2 Infrared Based Net

This component is a frame that includes a group of infrared transmitters that sends an invisible infrared light over the surface of the screen such that it will be received by a facing infrared receiver that works as a switch. This switch will detect the broken light

line from the sender in the opposite direction and cause a change in the logic level read by the ADC's.

This group of transmitters and receivers will be placed in two dimensions, x and y, such that each pair of sender/receiver will indicate an (x, y) coordinate that will have an equivalent location on the screen.

3.3.3 Interfacing Circuit

It's a set of hardware components that are responsible for providing communication between the infrared net and the PC by using a group of analog to digital converters that receives the input directly from the infrared leds in the frame and converts it to produce an equivalent digital output that is supplied to PC as input through the parallel port which will be handled by the software driver.

The interfacing circuit consists of many components, each one is responsible for performing a specific functionality, and these components are:

- Analog to Digital Converters:

Each ADC will read the voltage on a group of eight infrared receivers and be responsible for converting it to digital output.

- Internal Multiplexer:

The internal multiplexer in each ADC is responsible for switching between the groups of receivers that the ADC can read the voltage on.

- Decoder:

The decoder is responsible for switching between the five ADC IC's, such that each time a circuit will be enabled, this ADC then will switch between eight receivers to read their voltage and pass this voltage to the PC, then the decoder will switch to the next ADC and so on.

- Clock Generator:

This IC will be responsible for providing the ADC's with the clock signal they need to perform the analog to digital conversion.

- Buffer:

This IC will be responsible isolating the ADC's output, to prevent the interference.

3.3.5 Parallel Ports

The parallel port is used as a communication mechanism between the PC and the interfacing circuit, such that it will pass the control signals to the circuit, and output the data from it.

3.3.7 Screen Driver

This is the PC's part of the interfacing mechanism in the system, such that it will monitor the computer ports all the time, sending control signals to the interfacing circuit components, each time enabling one ADC, and for this ADC, it will switch between eight receivers reading the voltage, and so on until all the receivers are read, The software will analyze the voltage values and determine the action that will be taken.

The action taken by the screen driver in software will be implemented by a set of tools that provides a direct control of the operating system.

3.3.8 User Interface

This is the part of the program that user can interact with, such that it will provide the user with ability to control the whole services provided by the software driver including the interaction with the system's hardware, also it allows for choosing the preferred user's configurations, settings and user options.

3.4 How Does the System Work?

Our touch screen will provide the user with the ability to touch on a frame's surface that is mounted on the original screen, such that the frame will include inside of it a group of face-to-face infrared senders and receivers, each side of the frame will contain senders and receivers, each sender is next to a receiver and vice versa, in addition each sender will be facing to a receiver in the opposite direction, and also each receiver will be facing a sender in the opposite direction.

The senders will receive a power supply all the time to keep sending the infrared signals, what we are concerned about are the receivers actually, because they work as switches that will generate a specific logic level when receiving the infrared signal and this level will be changed when it is blocked by a touch in the same direction.

The receivers will change the amount of voltage between their sides when they receive a touch, so this voltage will be passed to an analog to digital converter that will be responsible for converting it to a digital output to be sent to the PC.

The number of receivers is large, and we can't take an input line from each receiver and connect it to the PC directly, so we need a switching mechanism that will let

us read the receivers one after another, fortunately each ADC has an inner multiplexer that can switch between eight different receiver's analog input, this way we need five ADC's to cover the whole frame receivers.

To switch between the five ADC's we use a decoder that is controlled by the PC through the parallel port, each time enabling only one ADC to read eight receivers, by this way the software driver will provide the control signal to the interfacing circuit.

On the other hand reading the output of the ADC's, storing the amount of voltage of each receiver, this voltage is an indicator of the state of the infrared beam in front of each receiver.

The software driver will analyze the voltages and determine if there is a touch on the screen surface, and also it will determine its position.

The receiver index will be passed to a position calculation function that will determine the exact X-Y position of the user touch, then the driver will take an action on the desktop through the operating system, that action could be a click, a right click or a scroll.

3.5 System Modeling

In this section we will view some models that describe the functionality of our system components in both hardware and software.

3.5.1 Data Flow Model

Figure 3.2 shows the data flow model of our system.

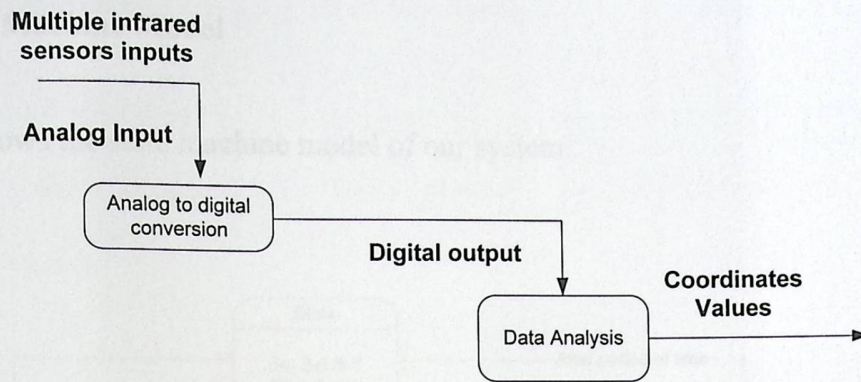


Figure 3.2: Data Flow Model

2.5.2 Use Case Model

Figure 3.3 shows the use case model of our system.

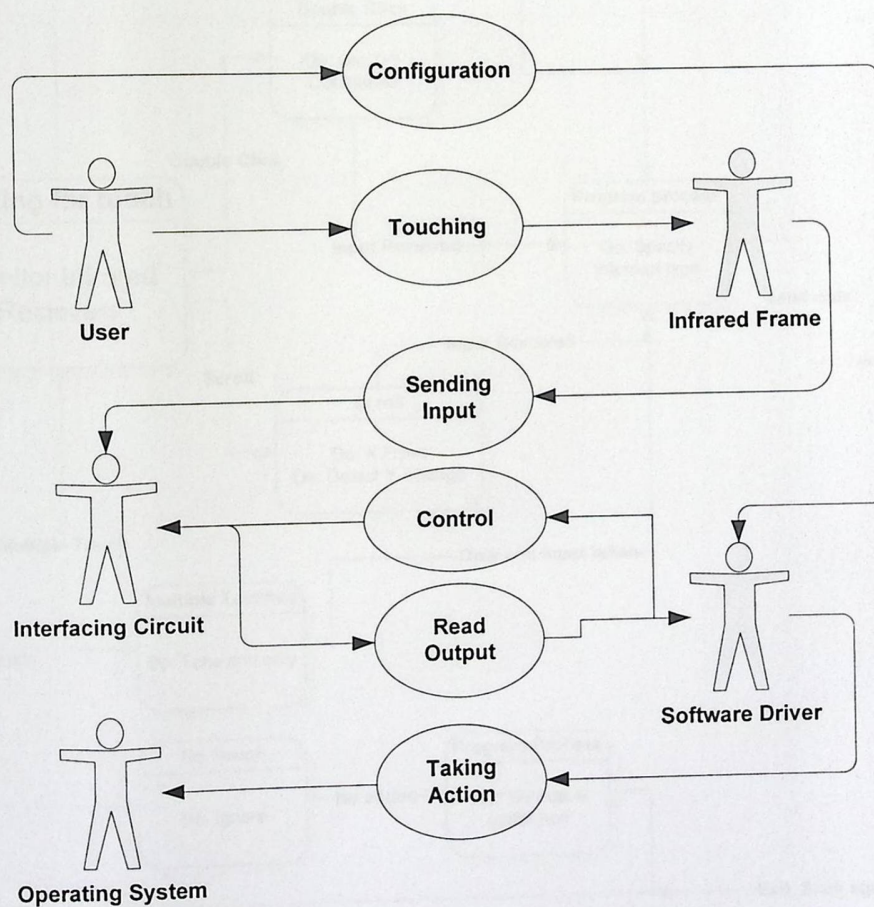


Figure 3.3: Use Case Model

3.5.3 State Machine Model

Figure 3.4 shows the state machine model of our system.

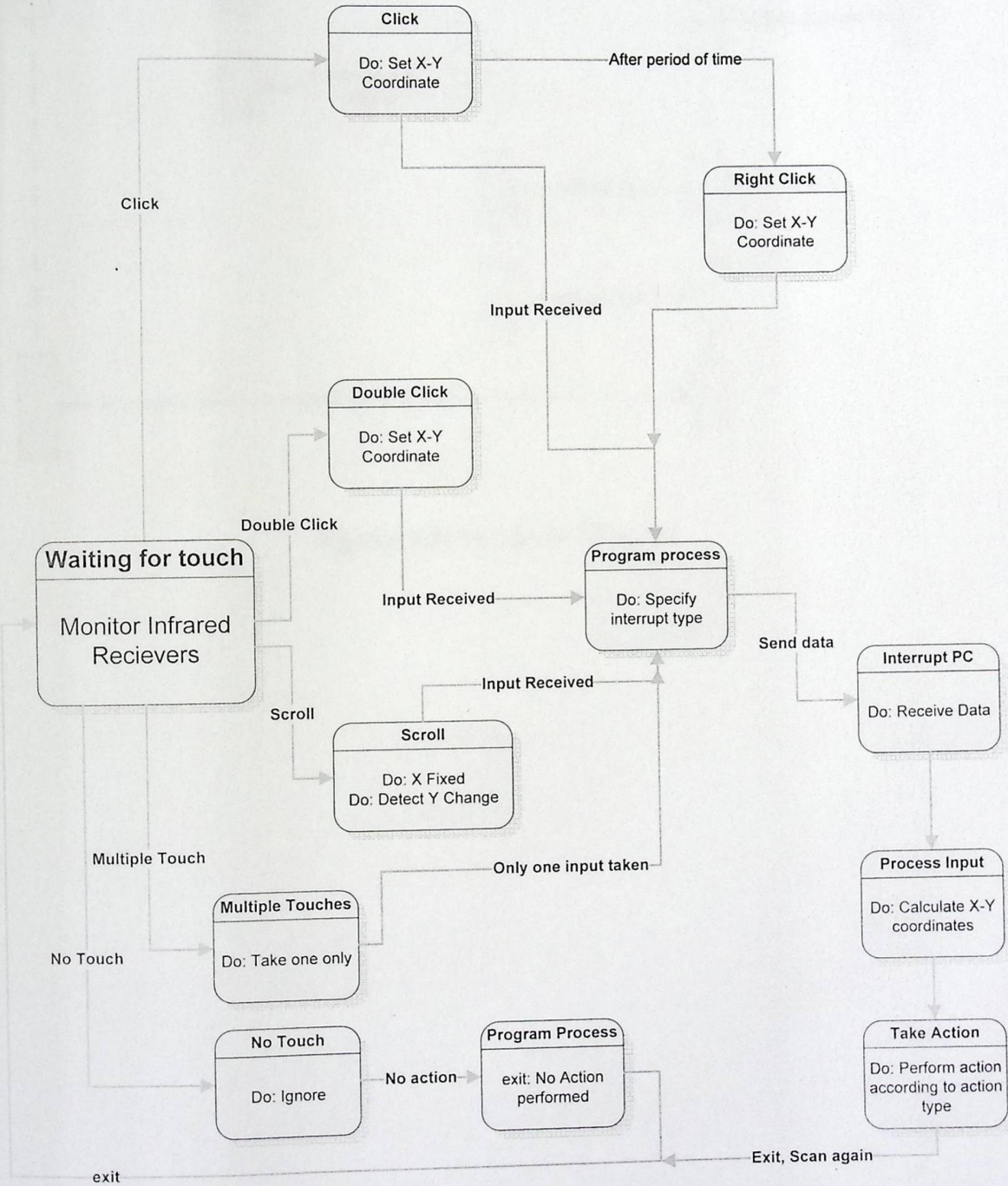


Figure 3.4: State Machine Model

3.5.4 Sequence Diagram

Figure 3.5 shows the sequence diagram of our system.

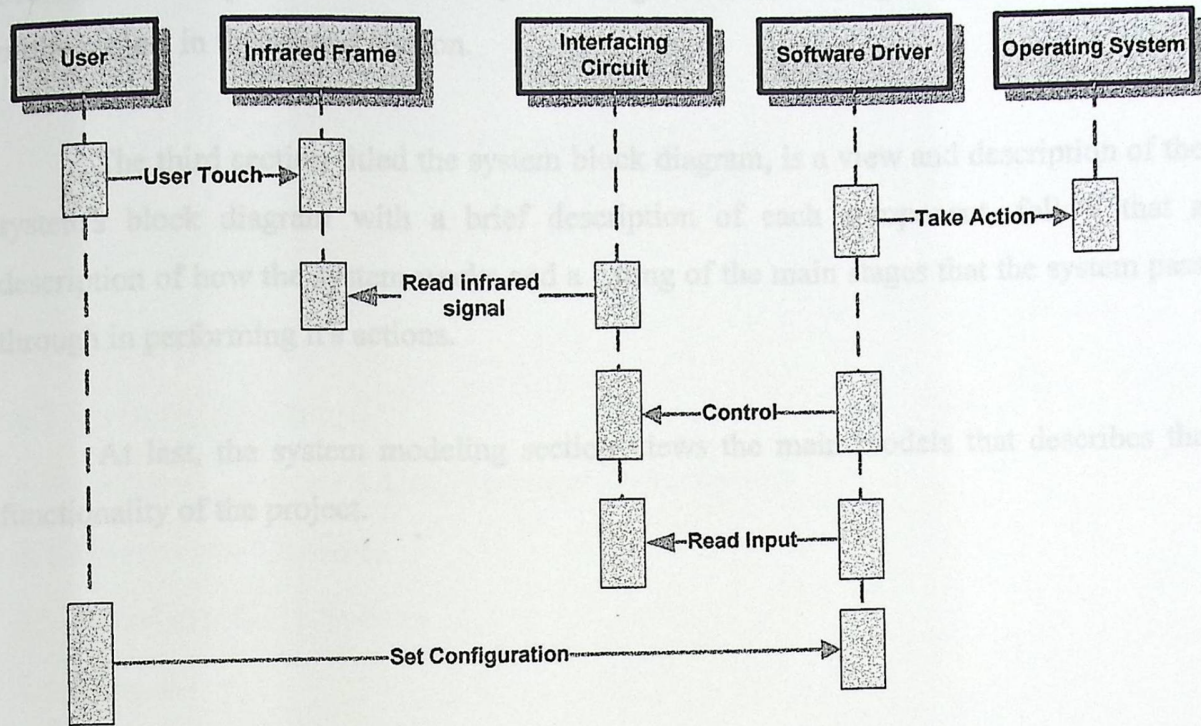


Figure 3.5: Sequence Diagram

3.6 Summary

Chapter three focuses on the architectural design of the project, starting with an overview the chapter and its sections, following that with a listing of the main objectives of the project in the second section.

The third section titled the system block diagram, is a view and description of the system's block diagram with a brief description of each component, follow that a description of how the system works and a listing of the main stages that the system pass through in performing it's actions.

At last, the system modeling section views the main models that describes the functionality of the project.

4.1 Overview

This chapter discusses the main structural design of the whole project in details, showing the main system design. In the third sections lists each component used in the system in both software and hardware with its details.

Chapter Four

Structural Design

Section four views the options that was available to use in the project, the effectiveness of each option and its ability to make the project work appropriately, then section five includes some scenes of the user interfaces for the software driver.

4.1 Overview

4.2 Structural Design

4.3 Detailed System's Components Description

4.4 Hardware Options

4.5 Software GUI Scenes

4.6 Summary

4.1 Overview

This chapter discusses the main structural design of the whole project in details, showing the main system design in the second section, the third sections lists each component used in the system in both software and hardware with its details.

Section four views the options that was available to use in the project, the effectiveness of each option and its ability to make the project work appropriately, then section five includes some scenes of the user interfaces for the software driver.

4.2 Structural Design

In this section we will view the diagrams and schematics that describe the design details of our project as a whole and the details for each component in the system. The following figure generally views the main components in our system and how they are connected to each other.

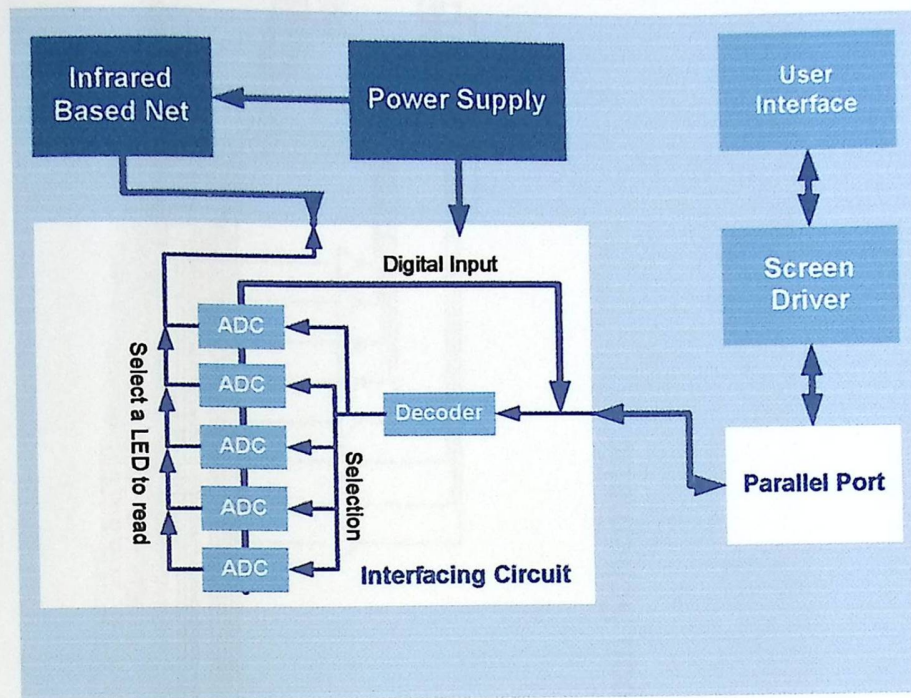


Figure 4.1: Overall System Block Diagram

The detailed communication between all the system components that we specified in figure 4.1 will be described through the complete system schematic in figure 4.2.

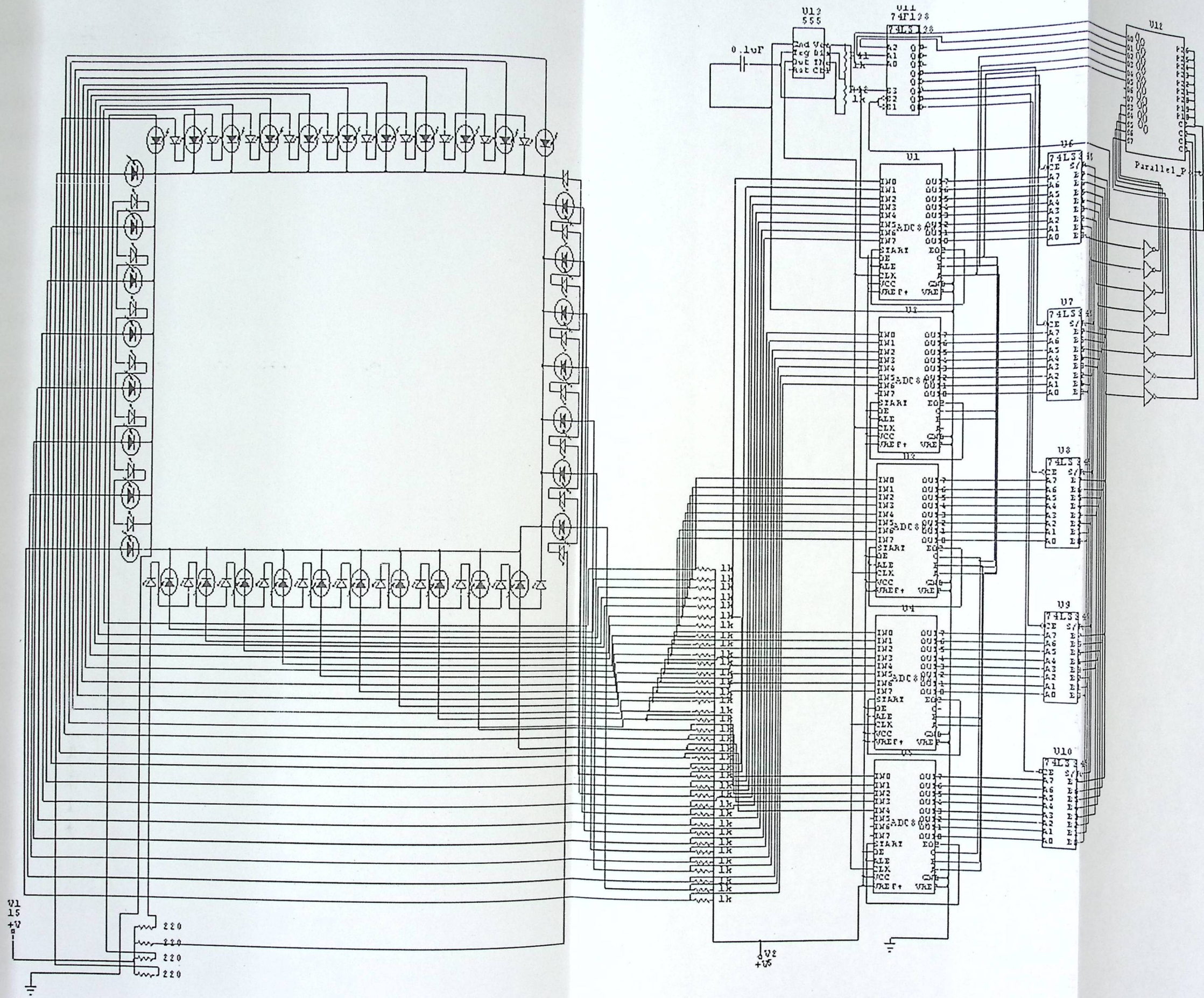


Figure 4.2: Infrared Touch Screen Schematic

4.3 Detailed System's Components Description

In this section we will list the main components of our touch screen describing their details and specifications.

4.2.1 Infrared Sensors

4.2.1.1 Why infrared sensors

We choose infrared sensors for the following reasons:

- 1- Low cost.
- 2- Infrared signals are not visible to user.
- 3- High power output and clarity.
- 4- High reliability, accuracy and stability.
- 5- Long life for long use.
- 6- Low drift.

The infrared LEDs that we will use in our project are:

1-Infrared Emitter (Transmitter) and its number is (QED233).

- Description

The QED233 is a 940 nm LED encapsulated in a clear untinted, plastic package

- Features

The QED233 has the following design features:

- Package type: T-1 3/4 (5mm lens diameter).
- Matched Photodiodes Numbers: QSD122/123/124.
- Medium Emission Angle, 40°.
- High Output Power.
- Package material and color: Clear, unstinted, plastic.

- Operating temperature (-40-100 C°).
- Continuous Forward Current (100 mA).
- Reverse Voltage (5 V)
- Power Lose (200 mW)

Figure 4.3 shows the dimensions for the infrared led package, and figure 4.4 shows its schematic.

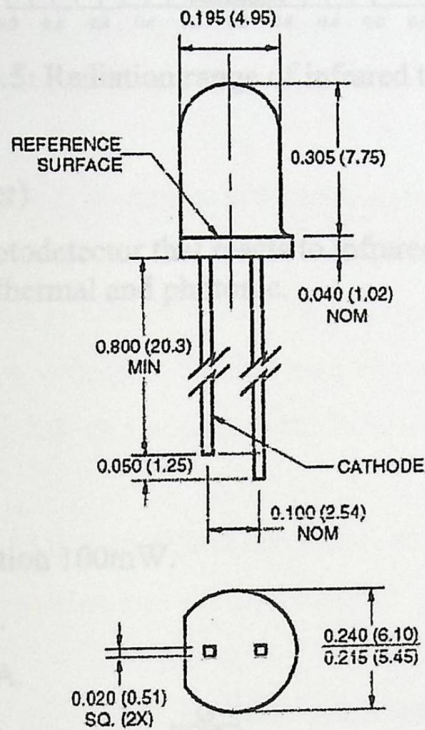


Figure 4.3: Infrared LED Package Dimensions

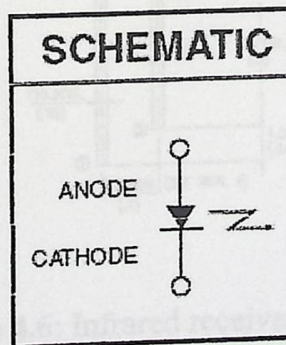


Figure 4.4: Infrared Transmitter Schematic.

Figure 4.5 shows the radiation angle of the infrared led.

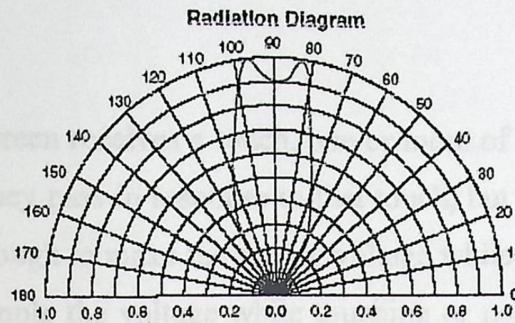


Figure 4.5: Radiation range of infrared transmitter.

2- Infrared Detector (receiver)

An infrared detector is a photodetector that reacts to infrared (IR) radiation. The two main types of detectors are thermal and photonic.

Features:

- 1- High sensitivity.
- 2- Low cost.
- 3- Maximum power dissipation 100mW.
- 4- Maximum voltage 1s0 V.
- 5- Maximum current 100mA.

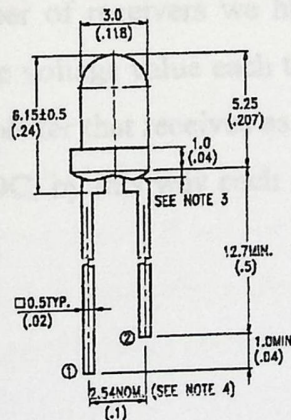


Figure 4.6: Infrared receiver diagram

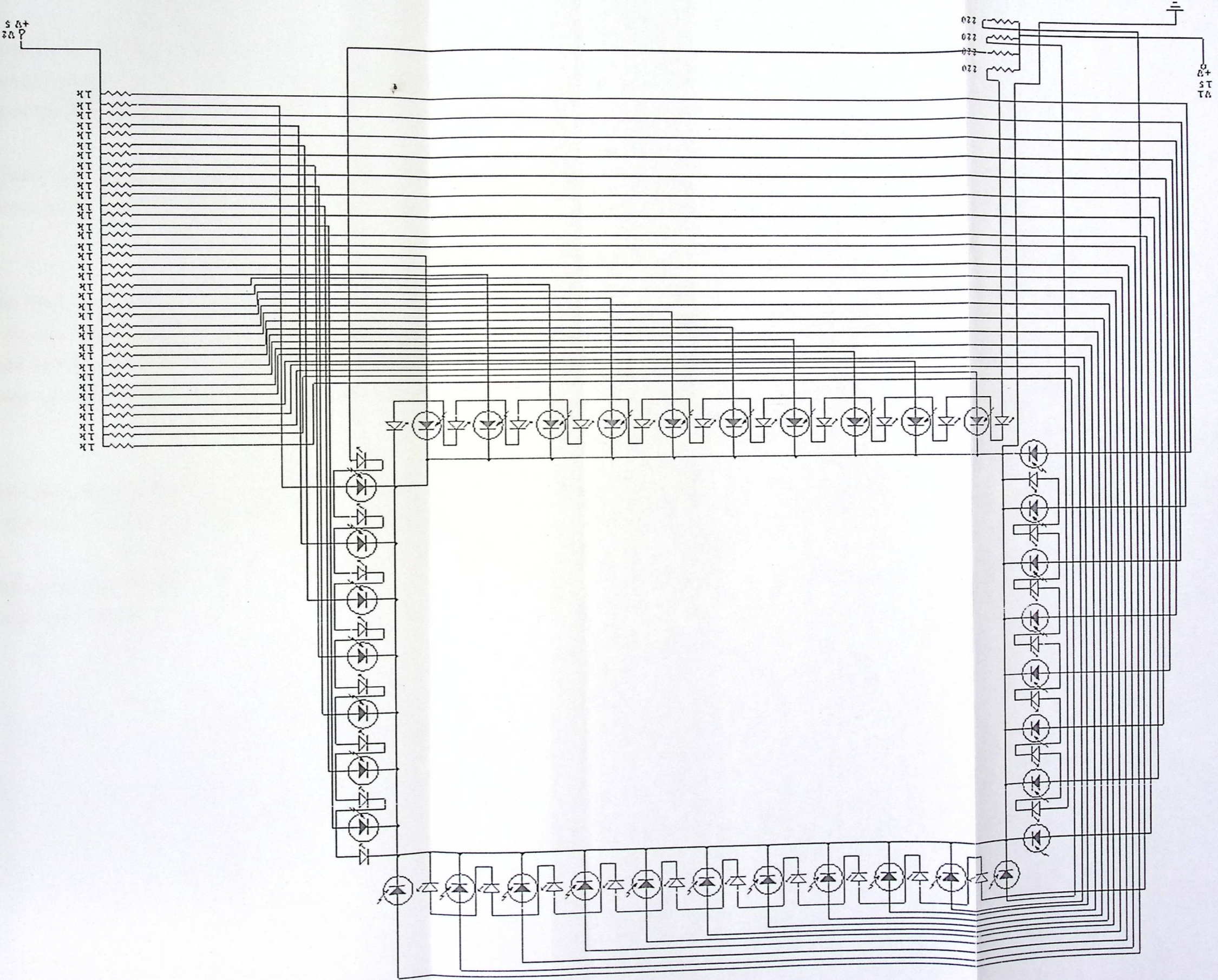


Figure 5.1: Infrared Net Circuit Diagram

Figure 5.1 views the infrared net circuit diagram, it consists mainly of infrared senders, each eight senders are connected in series and they are connected in parallel with the rest of the senders, after each group of senders there is a high power resistor that is used because it can handle the high current in the circuit.

The High current (120 mA) caused a very high temperature in the traditional resistors, which increase the possibility of resistors damage, we solve this problem by replacing them with a high power resistors (220 Ω , 5 Watt) that can handle the temperature

The receivers in the circuit are connected in parallel with each other, each one connected to 1K resistor, for each resistor there is an output line that passes the voltage on that resistor to the ADC to be converted and sent to PC.

For the infrared net frame work properly it needs a 15V power supply for the senders, and a 120 mA current, for the receivers, they are supplied form a 5V power supply.

In case of touching, the change in the amount of voltage read from the receivers is approximately from 0.7V to 1V, the change in voltage is not large enough because of the interference in receivers caused by the sent infrared beams, the receiver's voltage will be read by the ADC, and converted to a digital value, the change in voltage will be analyzed by the PC software.

There are lines that are coming out of the infrared net frame, those lines are:

- **Data Lines:** Line that are coming from the side of the receiver, to pass the voltage value to the ADC.
- **VCC:** provide the power supply to the circuit.
- **GND:** provide a ground to the circuit.

- Interfacing Circuit

This is the circuit that is responsible for reading the receiver's voltage, convert it from analog input to a digital output through the ADC's, switching between receivers by using the internal multiplexer and the decoder.

The interfacing is connected to the infrared net frame using an IDE data cable, reading the receivers analog voltages, and it is connected to the PC through the parallel port, to receive the control signals and also send the result of conversion to the PC software driver to be analyzed.

The interfacing circuit consists of the following components:

- Analog to Digital Converters:
- Internal Multiplexer
- Decoder
- Inverter
- Timer

Figure 5.2 views the circuit diagram of the interfacing circuit, it consists of a group of analog to digital converters, these converters are responsible for reading the voltage on the receivers, converting it from analog to digital, each converter output lines are connected to a buffer that enables or disables the ADC's output, each buffer enable line is connected to one of the decoder output lines, such that the decoder selects the ADC to be enabled by enabling it's buffer.

Each ADC contains an internal multiplexer, it is responsible for switching between multiple analog inputs received at the ADC inputs, and the 555 timer is responsible of providing the clock signal to the ADC's to enable a proper analog to digital conversion.

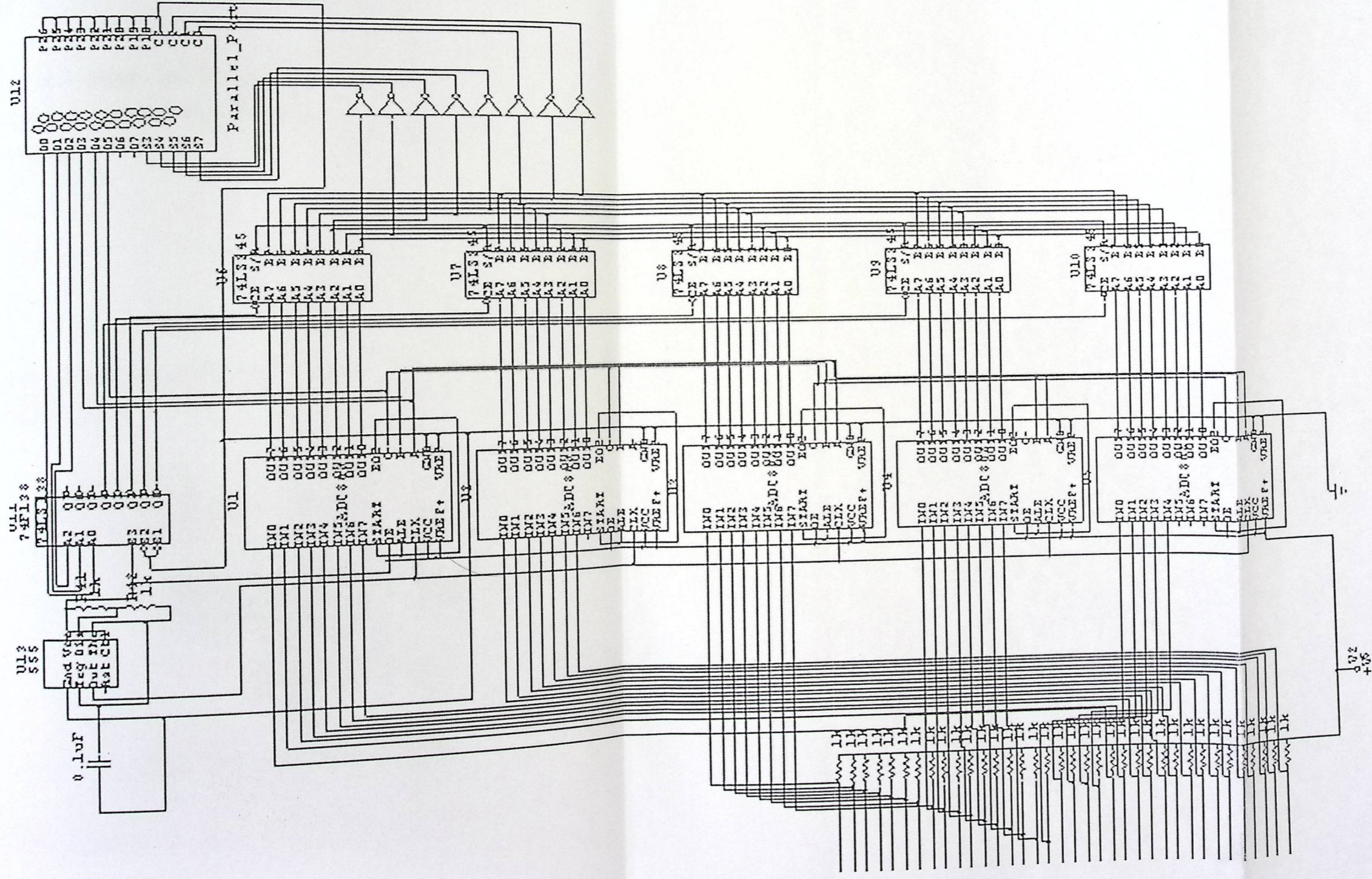


Figure 5.2: Interfacing Circuit

The line of the ADC's are connected to the parallel port, receiving control signals on the parallel port data lines because they are used to output data from the PC, and the ADC's send the digital output to the buffer and then to an inverter because the parallel port lines are inverted, the inverters output lines are connected to the parallel port control and status line because they can be used to input data to the PC.

- Parallel Port

Parallel port is a simple and inexpensive tool for building computer controlled devices and projects, it contains 25 pins and can be in many modes, and those modes are:

- Compatibility Mode
- Nibble Mode
- Byte Mode
- EPP
- ECP

The parallel port in our project is working in the ECP mode; figure 5.3 show the layout of the parallel port,

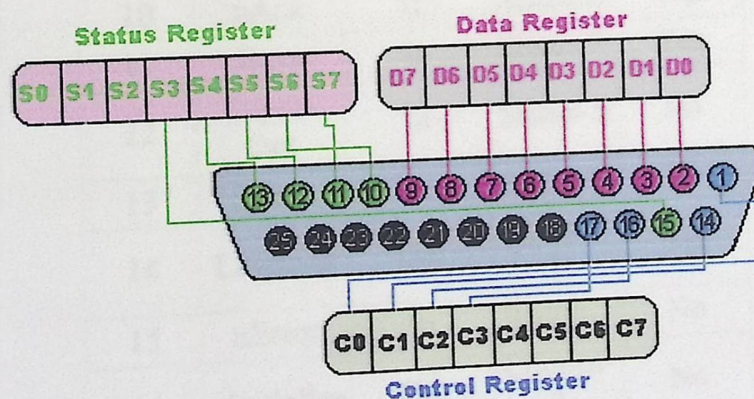


Figure 5.3: Parallel Port Layout

The lines in DB25 connector are divided in to three groups, they are

- Data lines

- Control lines
- Status lines

In our project we use the data line to send the control signals from the PC to the interfacing circuit, because they can be used as output lines, we use the control and status line as input lines to the PC because it can be used to input data, such that it receives the digital value of conversion.

The following shows the pins, their numbers and functionality.

Pin No (DB25)	Signal name	Direction	Register - bit	Inverted
1	nStrobe	Out	Control-0	Yes
2	Data0	In/Out	Data-0	No
3	Data1	In/Out	Data-1	No
4	Data2	In/Out	Data-2	No
5	Data3	In/Out	Data-3	No
6	Data4	In/Out	Data-4	No
7	Data5	In/Out	Data-5	No
8	Data6	In/Out	Data-6	No
9	Data7	In/Out	Data-7	No
10	nAck	In	Status-6	No
11	Busy	In	Status-7	Yes
12	Paper-Out	In	Status-5	No
13	Select	In	Status-4	No
14	Linefeed	Out	Control-1	Yes
15	nError	In	Status-3	No
16	nInitialize	Out	Control-2	No
17	nSelect-Printer	Out	Control-3	Yes
18-25	Ground	-	-	-

Table 5.1: Parallel Port Pins Layout

- Parallel Port Registers

In the parallel port data, control and status lines are connected to a corresponding register in the computer, by controlling these registers we can read or write to the parallel port, these registers are data, control and status registers.

The registers have addresses that can be accessed to control them, these are the addresses.

- Data: 0x378

- Control: 0x379

- Status: 0x37A

- Pins Usage:

1- Pin2 to Pin8 (D0 to D1):

- **D0, D1, and D2:** Selection lines on the decoder in the interfacing circuit.

The possible combinations are:

000: ADC0

001: ADC1

010: ADC2

011: ADC3

100: ADC4

- **D3, D4, D5:** Selection lines on the ADC internal multiplexer, it has an eight combinations to choose from.

- **D6:** connected to the start signal, to start the conversion process.

2- S3 to S7:

Used to input the first five bits of the converted data from the ADC.

3- C0 to C3:

The pins c0, c1, c2 are used to input the last three bits of the converted data to the PC.

5.3 Software Implementation

This section describes in general the software driver in the project, why it is needed, what it does and how it works by viewing a set of models that describes the actions of the software's different components, in addition to a pseudo code sections that provide a brief description of each part in the software and the tasks it performs.

5.2.1 General Description

As mentioned in the previous chapters, the hardware components in the project needs a control signals to be provided as inputs so as to work appropriately, those signals are supposed to be generated by the PC.

This is the main objective of the software driver, to monitor the infrared net through controlling the interfacing circuit, and take an action when it needs, this requires the software driver to communicate with the interfacing circuit in order to send control signals and receive the data to be analyzed.

According to data analysis, timing and software options the software will take actions directly in the operating system.

5.2.2 Software and Hardware Communication

To allow the communication between the hardware and the software, a data transmission mechanism must be used; in the project we choose the parallel port be that mechanism.

In the next chapter a full description of the parallel port will be provided, now as an introduction, the parallel port will be used to send the control signals to the interfacing circuit to provide the selection inputs to the integrated circuits used.

On the other hand, the parallel port will be used to send the data from the interfacing circuit to the PC, store it and analyze it after all, this analysis will determine the position on the screen and decide what action to be taken in the operating system.

5.2.3 Software Specifications

The software driver has two main objectives, the first is the monitoring of the infrared frame by sending control signals to the interfacing circuit, and receiving data to be analyzed, the second objective is to provide services to the user and allow changing the software settings and options.

The software contains a group of features and settings, some of them are related to the way that the software deals with the hardware, like touch timing, speed and response, on the other hand it contains settings for the program itself, to specify its behavior in general.

To allow an easy interaction with the software driver user interfaces, the software menus, buttons and controls were chosen to be appropriate for touching, using large sizes of buttons and other controls needed.

5.2.5 Software Models

In this section we show the models that specify the actions of the software and how it handles each event.

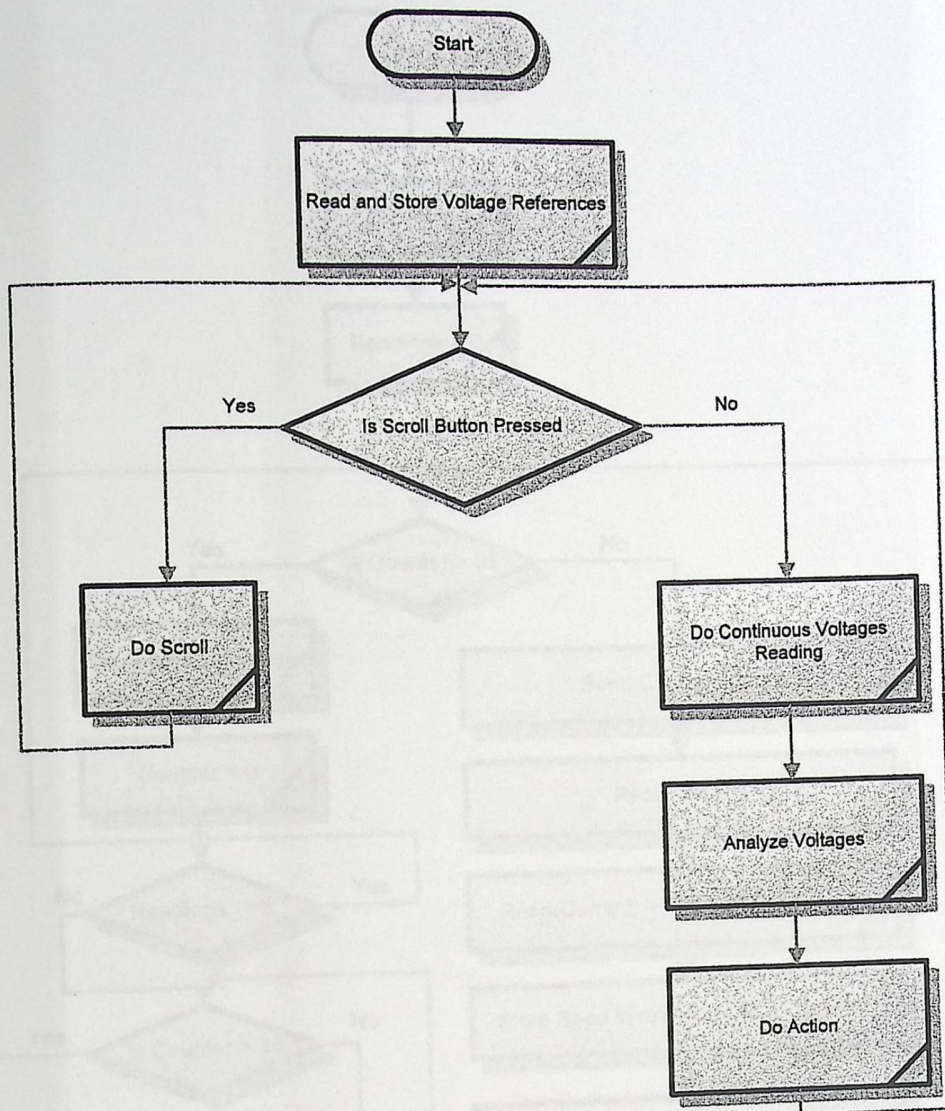


Figure 5.4: General Software Functionality

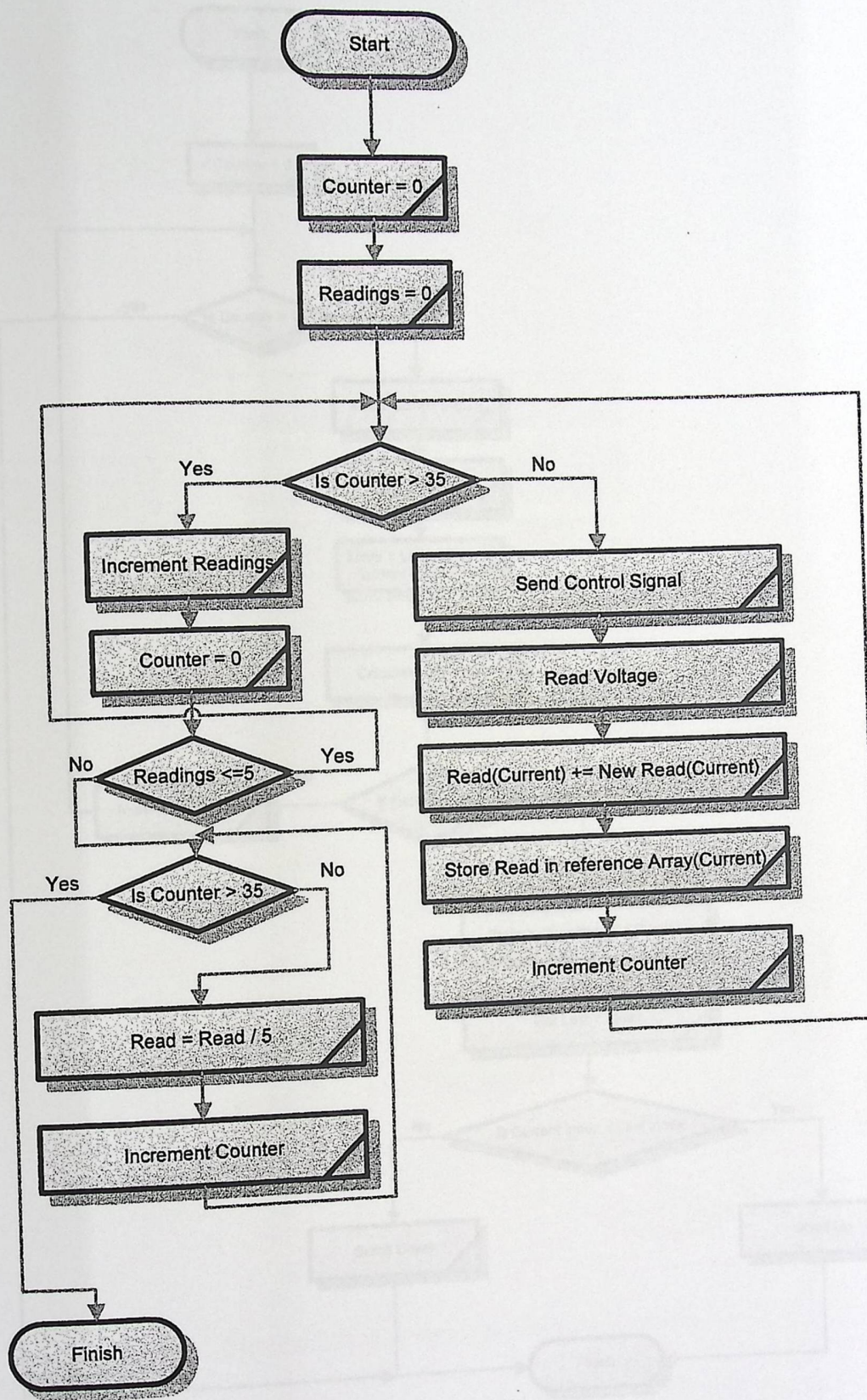


Figure 5.5: Reading the voltages references and storing the average values

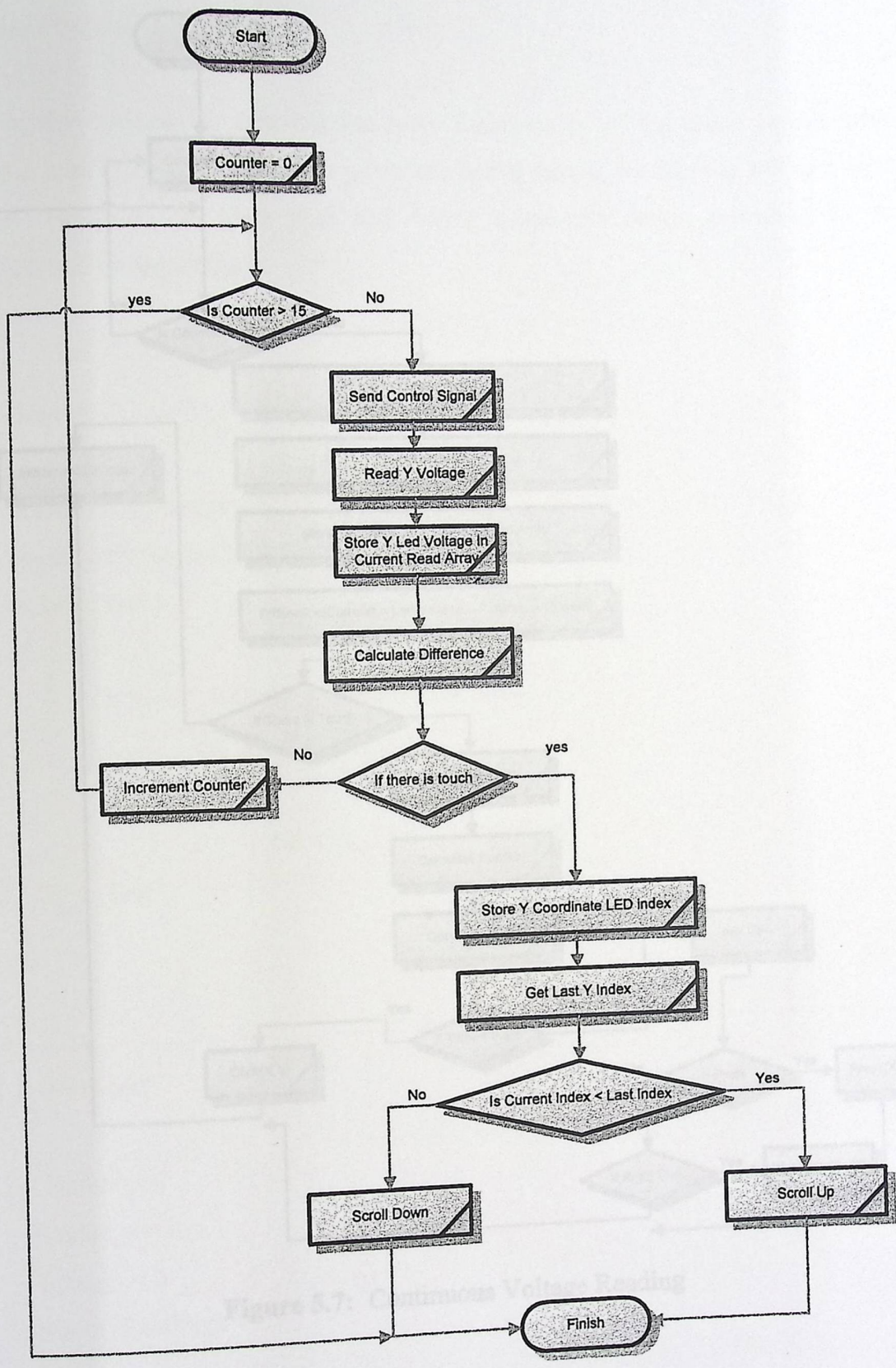


Figure 5.6: Scroll Action

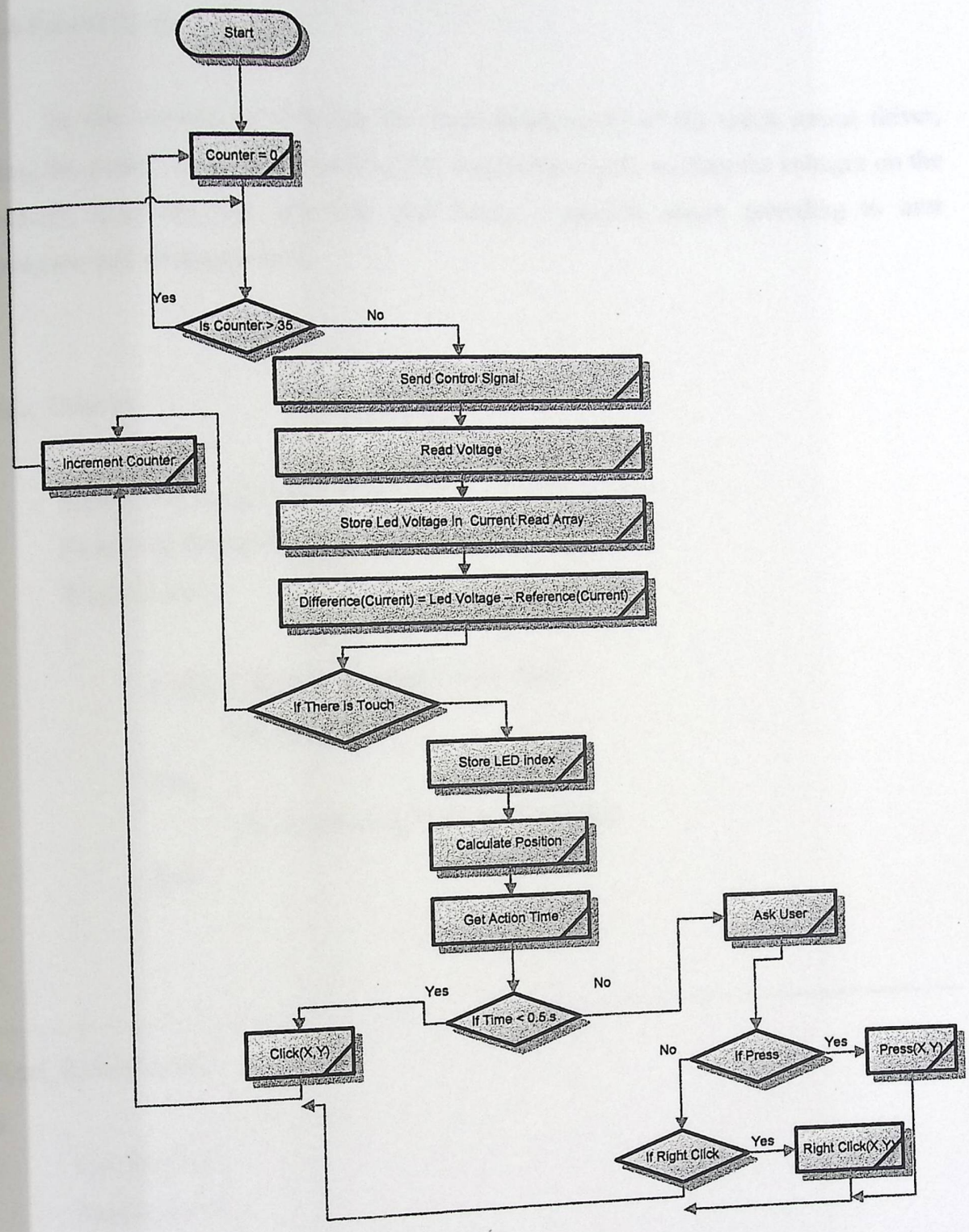


Figure 5.7: Continuous Voltage Reading

5.2.6 Pseudo Code

In this section we describe the main functionality of the touch screen driver, listing the pseudo code for controlling the interfacing circuit, reading the voltages on the receivers, analyzing the data read and taking a specific action according to user interaction and timing options.

```
Main_Timer()
```

```
{  
    References_Array = 0  
    Read_References(35) = 0  
    While (True)  
    {  
        If Scroll_Button_Pressed = True Then  
            Do_Scroll()  
        Else  
            Do_Continuous_Voltage_Reading()  
        End  
    }  
}
```

```
Read_References()
```

```
{  
    Counter = 0  
    Readings = 0  
    Voltage = 0  
    While (Readings <= 5)  
    {  
        While (Counter < 35)  
        {
```

```

        Send_Control_Signal(Counter)
        Voltage = Read_Voltage(Counter)
        References_Array(Counter) += Voltage
        Counter +=1
    }
    Counter = 0
    Readings += 1
}
While (Counter <=35)
{
    References_Array(Counter) = References_Array(Counter) /5
    Counter +=1
}
}

```

Do_Scroll()

```

{
    Counter = 0
    Voltage = 0
    V1 = 0
    V2 = 0
    While(Counter <15)
    {
        Send_Control_Signal(Counter)
        Voltage = Read_Voltage(Counter)
        Store_Y_LED_Voltage(Counter) = Voltage
        If (Voltage - Reference_Array(Counter) > 0.5 )
        {
            V1 = Read_Voltage(Counter - 1) - Reference_Array(Counter -1)
            V2 = Read_Voltage(Counter +1)- Reference_Array(Counter + 1)
        }
    }
}

```

```

    }
    If (V1 > V2)
    {
        Scroll_Up()
        return (Counter) > 0.5)
    Else
        Scroll_Down()
        return 0
    }
}
Counter += 1
}
}

```

Do_Continuous_Voltage_Reading()

```

{
    Counter = 0
    Voltage = 0
    Differences(35) = 0
    While (Counter < 35)
    {
        Send_Control_Signal(Counter)
        Voltage = Read_Voltage(Counter)
        Store_LED_Voltage(Counter) = Voltage
        Differences(Counter) = Voltage - Reference_Array(Counter)
        If (Counter < 15)
        {
            If (Differences(Counter) > 0.5)
            {
                Store_Y_LED_Index(Counter)
                Counter = 14
            }
        }
    }
}

```

```
}
}
If (15<Counter<35)
{
    If (Differences(Counter) > 0.5 )
    {
        Store_X_LED_Index(Counter)
        Counter = 0
    }
}
Counter +=1
}
Calculate_Position(X_LED_Index,Y_LED_Index)
Get_Action_Time()
Do_Action()
}
```

```
Send_Control_Signal(Currnet)
{
    Out_On_Parallel_Port(Contro_Word(Currnet),OutputAddress)
}
Do_Action(Click)
```

```
Read_Voltage(Current)
{
    Voltage_Value = 0
    Voltage_Value = Analyse_Input(In_From_Parallel_Port(Input_Address))
    Return Voltage_Value
}
```

Analyse_Input(Binary_Input)

```
{  
    Byte_Data = 0  
    Value = 0  
    Byte_Data = Invert_Active_Low_Lines(Binary_Input)  
    Value = Calculate_Volage(Byte_Data)  
    Return Value  
}
```

Calculate_Position(X_Index, Y_Index)

```
{  
    X_Poistion = X_Index * Screen.Resolution.Width / 21  
    Y_Poistion = Y_Index * Screen.Resolution.heigh / 15  
}
```

Get_Action_Time()

```
{  
    If (Time < Click_Time_In_Seconds)  
    {  
        Do_Action(Click)  
    }  
    Else  
        AskUser()  
}
```

AskUser()

```
{  
    Show_Option_Menu()  
    If (Option = Press)  
    {  
        Do_Action(Press)  
    }  
}
```

```
}  
Else if (Option = Right_Click)  
{  
    Do_Action(Right_Click)  
}  
}
```

Do_Action(Option)

```
{  
    If (Option = Click)  
    {  
        DoClick()  
    }  
    Elseif (Option = RightClick)  
    {  
        DoRightClick()  
    }  
    Elseif (Option = Press)  
    {  
        DoPress()  
    }  
}
```

5.4 Summary

This chapter specifies the implementation in details for both the hardware and software; in hardware it lists the main components and circuits diagrams, functional specifications and features. In software it lists a pseudo code of the algorithms used in the software and its functionality.

Testing

6.1 Overview

6.2 Hardware Testing

6.3 Software Testing

6.4 Summary

Chapter Six

Testing

6.1 Overview

6.2 Hardware Testing

6.3 Software Testing

6.4 Summary

6.1 Overview

This chapter focuses on the testing phase in the project, it consists of two sections, the first discusses the hardware testing operations, for each component alone, and also when it is connected to other components.

The second section discusses the software testing stages, the interfaces used and the results of each testing process.

6.2 Hardware Testing

This section views the main steps of testing the project's components, solving the problems that occur and finding alternative solutions, we specify how we attempted to build each component in the project, if it succeeded or not, and in case of failure, how we solved the problem or what kind of alternative solution we took.

In the following we list all the components we used specifying both the unit and block testing.

6.1 Infrared Sender:

- Unit Testing

When connecting the infrared sender, directly without using a resistor, the result is that the led will be burned because of the high current, when using a high resistance the radiation will be very low in a manner that the signal will not be detected by the receiver.

When connecting the infrared sender with a low resistance, the radiation will be in its maximum ratio.

- Block Testing

When each sender in series with a resistor, and connecting the senders in parallel with each other, this connection requires a very high current amount, which causes a large increase in the resistors temperature.

The serial connection of each sender with other senders and finally connecting each ten sender with a resistor is appropriate because the temperature on the resistors is normal and the current is low.

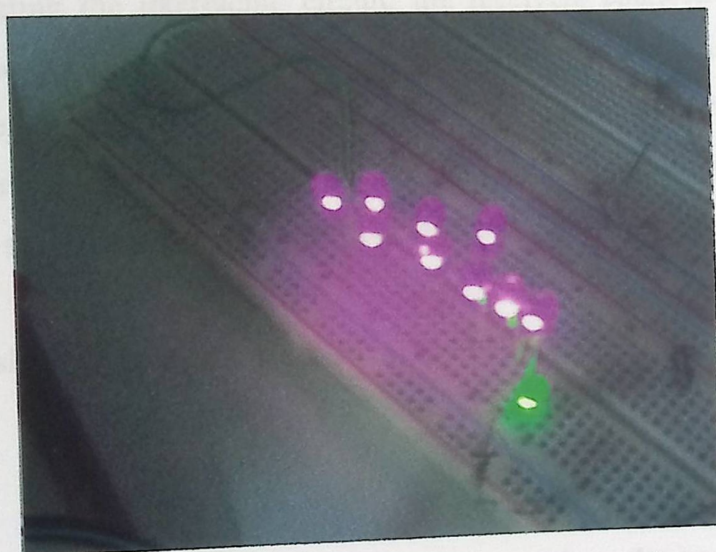


Figure 6.1: Infrared Senders Serial Connection

6.2 Infrared Receiver

- Unit Testing

Connecting the receiver without a resistor causes a low sensitivity, in a try to increase it we used an amplification circuit that contains an NPN transistor, but this option increases the circuit complexity without causing a significant efficiency.

In addition the transistor option that was use for switching between one and zero was functioning only for short distances, connecting the receiver with a resistor to the ground line and the other receiver's side being connected to the power supply was functioning correctly.

- Block Testing

Each receiver negative side was connected in series with a resistor connected to a common ground line to all other receivers in parallel, and the other side of the receiver being connected to a power supply, this option was functioning without being connected to the interfacing circuit.

When connecting the interfacing circuit, the receivers connection didn't work because the input lines of the ADC was receiving the voltage on the resistor rather than the receiver's voltage, to solve the problem the receiver's signal was taken from the node between the receiver and the resistor with the resistors being connected to the power supply and the other side of the receiver being connected to the ground.

6.3 High Power Resistors

- Unit Testing

Because of the high current consumption on the senders, the traditional resistors was burning because of the high temperature, to solve this problem we used a high power resistor to that can handle the high temperature.



Figure 6.2: High Power Resistors

6.4 Power Supply

- Unit Testing

We needed a 15V power supply that provides an enough current to the senders, also we needed a 5V power supply, and we took it from the USB port of the PC.

6.5 Oscillator

- Unit Testing

In the first try of using the oscillator, we took the output signal without using specific oscillator circuit, the result was an erroneous conversion by the ADC, the reason was that the ADCs needs a specific clock frequency that ranges from 640 to 680 KHZ, that is controlled by the values of two resistors and a capacitor being used in the oscillator circuit.

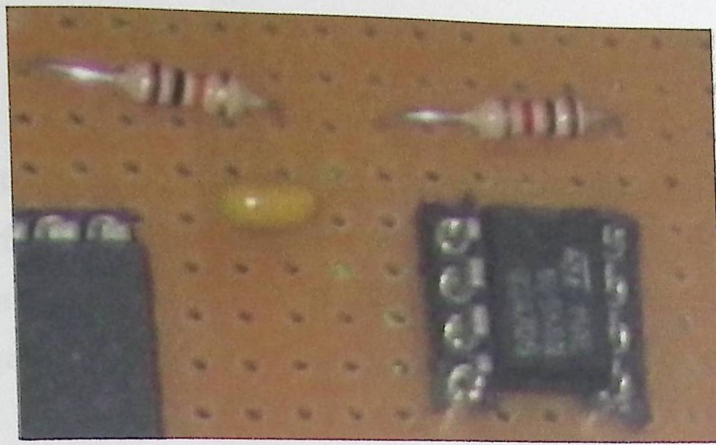


Figure 6.3: Oscillator

6.6 Analog to Digital Converter

- Unit Testing

In using the ADC ICs, there were many problems that came out into the scene, next we list each line of the ADC that caused a problem, and how we solved it.

- Clock:

At the first usage of the line, we supplied the ADC with a random clock frequency that caused a failed conversion process, after that we provided the appropriate clock frequency from the oscillator by build a correct oscillation circuit with a specific resistor's and capacitor's amount.

- Start:

The start pin was receiving the signal from the PC, this caused a problem because the period of the active low signal was very short, and being undetected by the ADC, to solve the problem we connected the start signal with the end of conversion output signal.

This connection is called a free running conversion, such that after each conversion, the ADC will automatically start conversion again.

- ALE:

At first, the ALE pin was connected to the power supply, this caused a wrong input selection, from the timing diagram of the ADC, and we concluded that the ALE signal must be provided as a pulse on the conversion starting process, so we connected it with the start signal.

- Output Enable:

The problem with the output enable, that it didn't prevent the signal on the output lines of the ADC from being passed because it didn't being changed to a tri-state, this was a problem because the output lines of the ADC's are shared, and this causes interference if the signals are buffered.

To solve the problem we used a buffer to prevent the signal from being interfered with other signals, and the output enable line was always connected to the power supply, such that the output is always enabled.

- Block Testing

When connecting the five ADC ICs with each other, the problem we faced was in the output signals interference, this problem was solved by using tri-state transceiver.

6.7 Decoder

- Unit Testing

Once a decoder IC was connected in wrong way which caused the decoder to be crashed, and we didn't discover that early, which caused a delay in the progress.

6.8 Parallel Port

In using the parallel port, there were many problems, first of all we didn't connect the ground lines of the parallel port to the ground line of the circuit, and this caused an erroneous data reading on the parallel port.

The second problem was using the wrong lines of the parallel port to receive the input from the ADCs; this was because the wrong view of the numbers on the parallel port.

The third problem was in that the parallel port control and status line are all active low, and some of them are inverted, we used to provide them with an active high and this caused no data receiving at the parallel port.

6.3 Software Testing

This section views the main steps of testing the software, determine its behavior and how to interact with the interfacing circuit through a temporary software interfaces that helps in understanding the actions of both the software and hardware.

Next we list each stage of using the software, the purpose of it and the problems that we faced.

- Reading the parallel port lines

At this level of testing the software, we created a temporary software interface to test the interfacing circuit and study its behavior according to each input coming from the PC.

The following figure shows a section of the testing software, it contains controls that reads continuously the parallel port line and shows the output as binary and as

decimal values, also it allows us to send data to the control and data lines because they can be used to output data on the parallel port. The data in the text boxes needs adjustment because some of the pins are inverted.

The screenshot shows a window titled "Form1" with three rows of input fields. Each row has a label, a text box for a decimal value, a text box for a binary value, a "Send" button, and an empty text box for the result.

Label	Decimal Value	Binary Value	Action	Result
Data	8	00001000	Send	
Status	120	01111000		
Control	12	00001100	Send	

Figure 6.4: Reading the data on the parallel port line

- Sending control signal to the interfacing circuit

At this level of testing the software, we used components and controls to send interfacing signals to the interfacing circuit, each time selecting a specific IC of the ADCs in the circuit and for each IC, we can choose which receiver to read its voltage, this can be done by sending a specific selection word on the parallel port output lines.

Pressing a specific button will change the value of the control word send, which will change the selected receiver on the circuit.

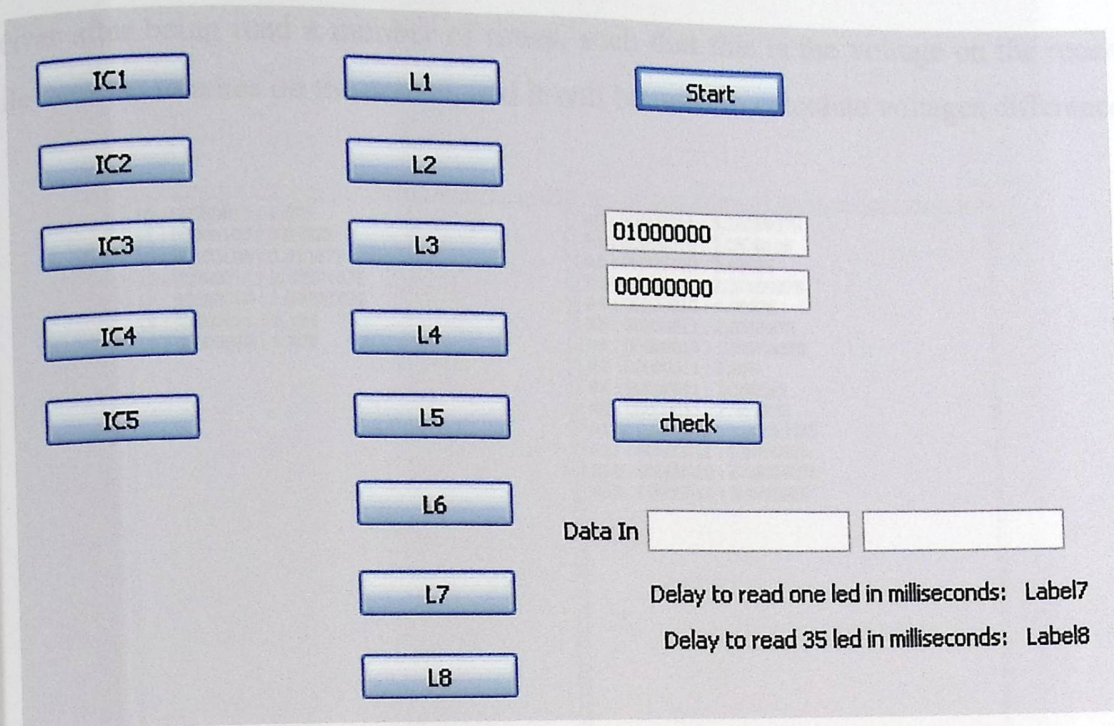


Figure 6.5: Sending Control Signals on the Parallel Port

In the last figure, there are five buttons to select each ADC, and eight buttons to select a specific receiver in the ADC to be read, after selection, the receiver voltage will be shown in the text boxes as binary and decimal values.

On the other hand the time required for sending the control signal and until receiving the voltage value is calculated and placed in the text box as a value in milliseconds.

- Reading the receivers voltages using the parallel port

At this stage of software testing we were reading the analog voltage of each receiver and store it to be used in calculation, this calculation will determine the index of the led that detected a touch, and calculate the position of the touch on the screen.

The following figure shows the storing of the receivers voltages as they are read successively one after another, it also shows the average value of the voltage on each

receiver after being read a number of times, such that this is the voltage on the receiver while there no touches on the screen, and it will be used to calculate voltages differences.

L0 : 00000010 : 1.875	R0 : 00000011 : 3.18359375
L1 : 00000100 : 3.59375	R1 : 00000010 : 2.2578125
L2 : 00000100 : 3.671875	R2 : 00000100 : 3.65625
L3 : 00000011 : 2.63671875	R3 : 00000010 : 2.37109375
L4 : 00000010 : 1.69921875	R4 : 00000010 : 1.90625
L5 : 00000011 : 3.125	R5 : 00000011 : 2.8359375
L6 : 00000010 : 1.875	R6 : 00000010 : 1.91796875
	R7 : 00000011 : 2.875
	R8 : 00000011 : 3.390625
	R9 : 00000011 : 2.859375
	R10 : 00000011 : 2.80859375
	R11 : 00000011 : 2.5390625
	R12 : 00000010 : 2.18359375
	R13 : 00000011 : 3.4765625

Figure 6.7: Reading Receivers Voltages

The following figure shows an image of the software while running; it shows that the screen is receiving touch, using a label that is visible only when a touch occurs; it also shows the voltages of the receivers on each reading.

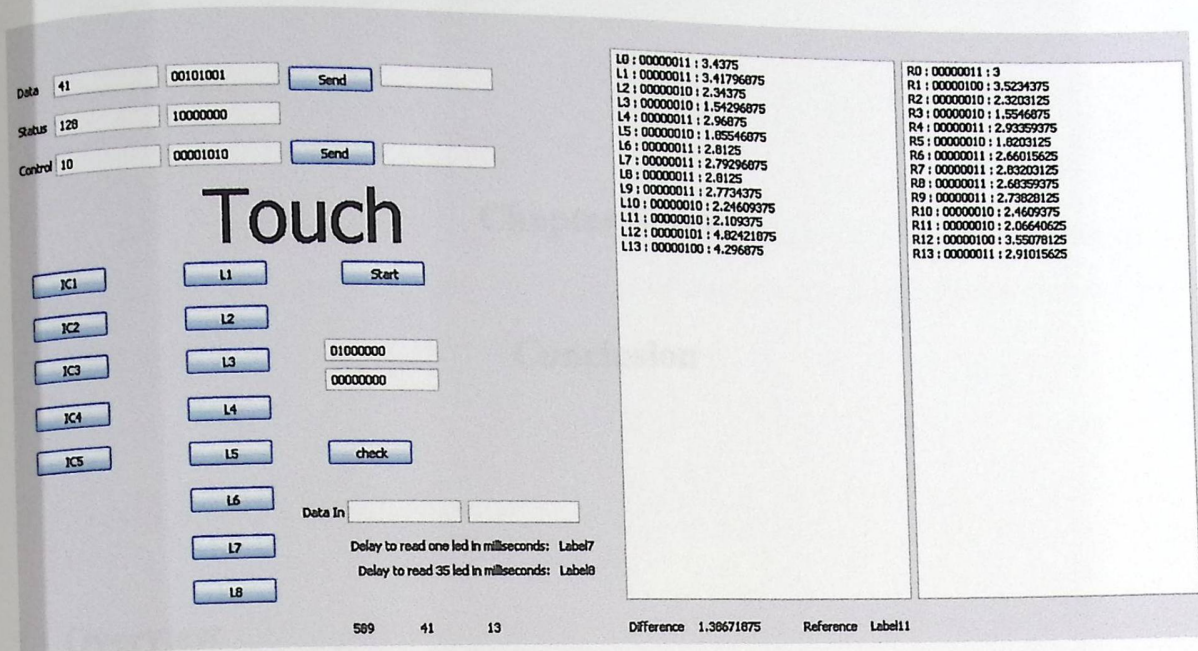


Figure 6.8: Touch State

6.4 Summary

This chapter focuses on the testing stage of the project, the first section is about hardware testing, it shows each unit that is tested, what problems we faced and how we solved it, the result of unit and block testing for each component in the hardware.

Section two is about the software testing, showing the interfaces that were used, what results we had after testing each component and the problems that we faced.

Chapter Seven

Conclusion

7.1 Overview

7.2 Results and Conclusion

7.3 Challenges

7.4 Future Work

7.5 Summary

7.1 Overview

This chapter reviews the results of the project as a whole, including the conclusion that we came out with, the results of our project, the problems that we faced and our suggestion for future work on related project.

7.2 Results and Conclusion

In the infrared net based touch screen project, we built an infrared net that consists of a group of sender and receivers facing each other, mounted on an aluminum frame, also we connected the frame into an interfacing circuit that is connected to the PC.

The software on the PC will be responsible for scanning the infrared frame through sending control signals to the interfacing circuit, the results we came out with satisfies the main requirement we stated in the previous chapters, and the following are the results we achieved:

- 1- We built an infrared based touch screen that is interactive and sensitive to a finger touch.
- 2- We built the main interfacing circuit including the analog to digital converters, internal multiplexers, decoder, tri-state transceiver, clock generator and inverters.
- 3- We connected the interfacing circuit with the PC using the parallel port.
- 4- We implemented the software that communicates with the hardware and provides the user's services.
- 5- Threads can be used to reduce the response time because it allows the pipelining
- 6- Win32 APIs provide functions that give the programmer a full control of the operating system's hardware and software components.
- 7- The light of the computer screen doesn't affect the infrared beam over its surface.

7.3 Challenges

The following are the main challenges and problems that we faced while the project building process:

- 1- The infrared beam interference causes a wrong detection of the touch on the screen, such that multiple receivers can be affected by a touch that is not really in their direction.
- 2- Despite that the aluminum is a good choice to build the frame, but it causes beams reflections that results in wrong detection.
- 3- The infrared senders consume a high level of power and require high power resistors to work in an efficient manner.
- 4- There is a significant delay in scanning the infrared net because of the time needed in transferring the control signal from the PC to the interfacing circuit and receiving the data from the interfacing circuit.
- 5- The large size of the senders and receivers causes a limitation on the number of the sensors that can be used as whole.

7.4 Future Work

- 1- A microcontroller can be used to provide the PC to infrared net interfacing, such that the microcontroller can interrupt the PC only when a touch occurs.
- 2- Increasing the number of the infrared receivers/senders, this increases the resolution.
- 3- Increasing the length of the frame canals to increase the filtration and reduce the interference.
- 4- Reducing the size of the frame holes to allow the increasing of the receivers/senders number.
- 5- Using a photo transistor instead of photo diodes because they have a higher sensitivity.
- 6- Using the USB port for data send and receive to increase the speed and response.

7.5 Summary

This chapter focused on the results of our project progress, the conclusion we came out and our suggestions for future work on related projects.

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URL: <http://www.computerhope.com/help/serial.htm>

APPENDIX

Appendix A: Data Sheets

APPENDIX A

DATA SHEETS

APPENDIX

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Appendix A:

Semiconductor

November 1985

ADC0808/ADC0809 8-Bit μ P Compatible A/D Converters with 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 A/D converter comprises a complete 8-bit device with an 8-bit analog-to-digital converter, 8-channel multiplexer and 8-bit parallel digital-to-analog converter. The 8-bit A/D converter uses successive approximation as the conversion technique. The conversion technique uses a successive approximation register, a 2.5V reference voltage with analog switch and a 2.5V reference voltage. The 8-bit digital-to-analog converter uses a 2.5V reference voltage.

The design of the ADC0808, ADC0809 has been optimized by incorporating the latest device technology of modern μ P compatible technology. The ADC0808, ADC0809 offers high speed for applications, internal temperature dependence, excellent accuracy, internal temperature dependence, and low power consumption. These features make the device ideally suited to applications from process and machine control to industrial and scientific applications. For technical information with complete circuit diagrams and the ADC0808 data sheet, see AD-247 or visit www.infocenter.infocenter.com.

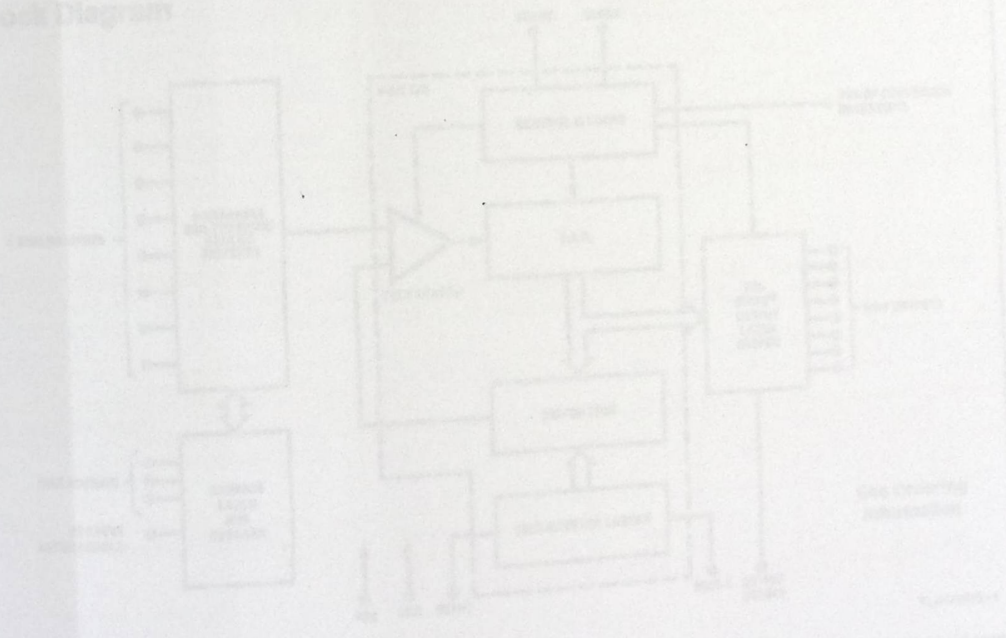
Features

- Easy interface to all microprocessors
- Complete independence of V_{DD} or analog input referred without reference
- No zero or full-scale output required
- 8-bit parallel interface with address logic
- 0V to 2V input range with input of 2V source
- 8-bit digital-to-analog converter
- 8-bit digital-to-analog converter
- 8-bit digital-to-analog converter
- 8-bit digital-to-analog converter

Key Specifications

- Resolution: 8 bits
- Total Converter Error: $\pm 1/2$ LSB
- Range: 0V to 2V
- Low Power
- Conversion Time

Block Diagram



ADC0808/ADC0809 8-Bit μ P Compatible A/D Converters with 8-Channel Multiplexer

ADC0808/ADC0809 8-Bit μ P Compatible A/D Converters with 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8 single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE[®] outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.)

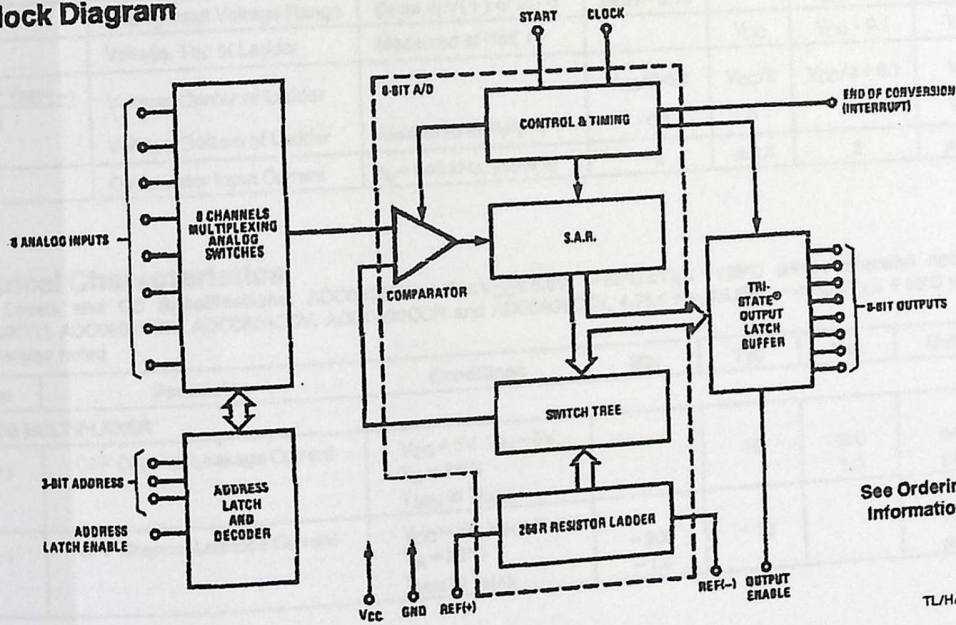
Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- No zero or full-scale adjust required
- 8-channel multiplexer with address logic
- 0V to 5V input range with single 5V power supply
- Outputs meet TTL voltage level specifications
- Standard hermetic or molded 28-pin DIP package
- 28-pin molded chip carrier package
- ADC0808 equivalent to MM74C949
- ADC0809 equivalent to MM74C949-1

Key Specifications

Resolution	8 Bits
Total Unadjusted Error	$\pm 1/2$ LSB and ± 1 LSB
Single Supply	5 V _{DC}
Low Power	15 mW
Conversion Time	100 μ s

Block Diagram



See Ordering Information

TL/H/5672-1

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin	-0.3V to ($V_{CC} + 0.3V$)
Except Control Inputs	
Voltage at Control Inputs	-0.3V to +15V
(START, OE, CLOCK, ALE, ADD A, ADD B, ADD C)	
Storage Temperature Range	-65°C to +150°C
Package Dissipation at $T_A = 25^\circ\text{C}$	875 mW
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Molded Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 8)	400V

Operating Conditions (Notes 1 & 2)

Temperature Range (Note 1)	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC0808CJ	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$
ADC0808CCJ, ADC0808CCN,	
ADC0808CCN	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$
ADC0808CCV, ADC0809CCV	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}

Electrical Characteristics

Converter Specifications: $V_{CC} = 5$, $V_{DC} = V_{REF+}$, $V_{REF(-)} = \text{GND}$, $T_{MIN} \leq T_A \leq T_{MAX}$ and $f_{CLK} = 640$ kHz unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808					
	Total Unadjusted Error (Note 5)	25°C T_{MIN} to T_{MAX}			$\pm 1/2$ $\pm 3/4$	LSB LSB
	ADC0809					
	Total Unadjusted Error (Note 5)	0°C to 70°C T_{MIN} to T_{MAX}			± 1 $\pm 1 1/4$	LSB LSB
	Input Resistance	From Ref(+) to Ref(-)	1.0	2.5		k Ω
	Analog Input Voltage Range	(Note 4) V(+) or V(-)	GND-0.10		$V_{CC} + 0.10$	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref()		V_{CC}	$V_{CC} \pm 0.1$	V
$\frac{V_{REF(+)} + V_{REF(-)}}{2}$	Voltage, Center of Ladder		$V_{CC}/2 - 0.1$	$V_{CC}/2$	$V_{CC}/2 + 0.1$	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(-)	-0.1	0		V
I_{IN}	Comparator Input Current	$f_c = 640$ kHz, (Note 6)	-2	± 0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0808CJ 4.5V $\leq V_{CC} \leq 5.5$ V, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ unless otherwise noted
ADC0808CCJ, ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, 4.75 $\leq V_{CC} \leq 5.25$ V, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
$I_{OFF(+)}$	OFF Channel Leakage Current	$V_{CC} = 5$ V, $V_{IN} = 5$ V, $T_A = 25^\circ\text{C}$ T_{MIN} to T_{MAX}		10	200 1.0	nA μA
$I_{OFF(-)}$	OFF Channel Leakage Current	$V_{CC} = 5$ V, $V_{IN} = 0$, $T_A = 25^\circ\text{C}$ T_{MIN} to T_{MAX}	-200 -1.0	-10		nA μA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0808CJ, ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, $4.5V \leq V_{CC} \leq 5.5V$, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ unless otherwise noted less otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	$V_{IN} = 15V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	$V_{IN} = 0$	-1.0			μA
I_{CC}	Supply Current	$f_{CLK} = 640 \text{ kHz}$		0.3	3.0	mA
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = -360 \mu A$	$V_{CC}-0.4$			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 1.6 \text{ mA}$			0.45	V
$V_{OUT(EO)}$	Logical "0" Output Voltage EOC	$I_O = 1.2 \text{ mA}$			0.45	V
I_{OUT}	TRI-STATE Output Current	$V_O = 5V$ $V_O = 0$	-3		3	μA μA

Electrical Characteristics

Timing Specifications $V_{CC} = V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, $t_r = t_f = 20 \text{ ns}$ and $T_A = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	(Figure 5)		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	(Figure 5)		100	200	ns
t_s	Minimum Address Set-Up Time	(Figure 5)		25	50	ns
t_H	Minimum Address Hold Time	(Figure 5)		25	50	ns
t_D	Analog MUX Delay Time From ALE	$R_S = 0 \Omega$ (Figure 5)		1	2.5	μS
t_{H1}, t_{H0}	OE Control to Q Logic State	$C_L = 50 \text{ pF}$, $R_L = 10k$ (Figure 8)		125	250	ns
t_{H1}, t_{H0}	OE Control to Hi-Z	$C_L = 10 \text{ pF}$, $R_L = 10k$ (Figure 8)		125	250	ns
t_c	Conversion Time	$f_c = 640 \text{ kHz}$, (Figure 5) (Note 7)	90	100	116	μS
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	(Figure 5)	0		$8 + 2 \mu S$	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs		10	15	pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0V_{DC} to 5V_{DC} input voltage range will therefore require a minimum supply voltage of 4.800 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See Figure 3. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See Figure 13.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence (Figure 6). See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Note 8: Human body model, 100 pF discharged through a 1.5 k Ω resistor.

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Functional Description

Multiplexer. The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table I shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE I

SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

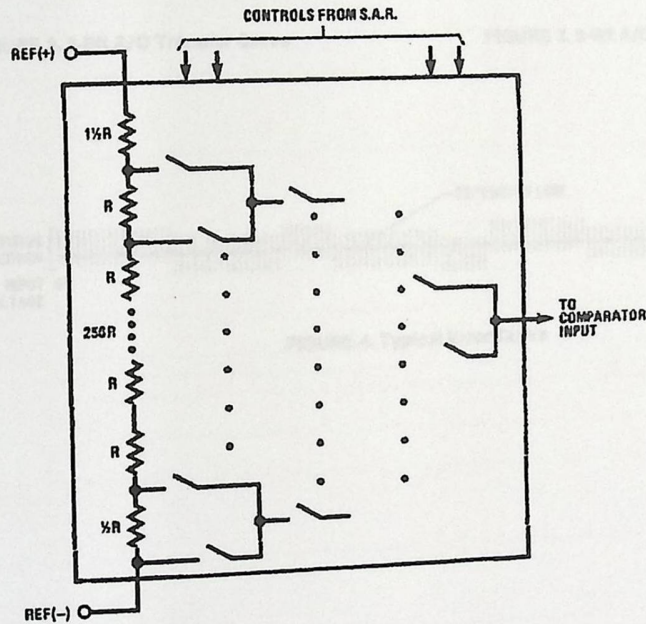
The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed

to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach (Figure 1) was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in Figure 1 are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached $+\frac{1}{2}$ LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. Figure 2 shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.



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FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion. The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the

comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

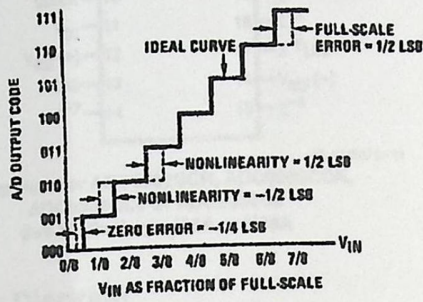


FIGURE 2. 3-Bit A/D Transfer Curve

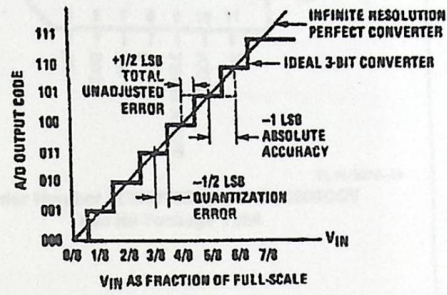


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

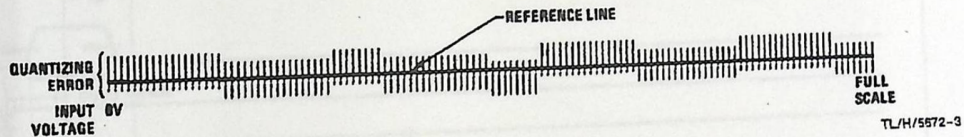


FIGURE 4. Typical Error Curve

Functional Description (Continued)

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion. The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the

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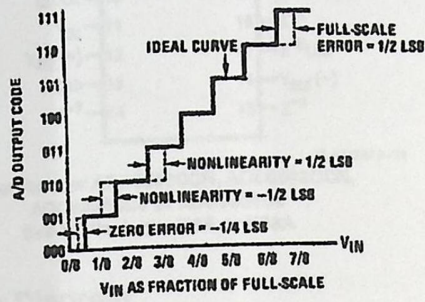


FIGURE 2. 3-Bit A/D Transfer Curve

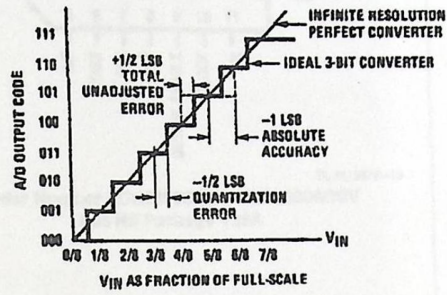


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

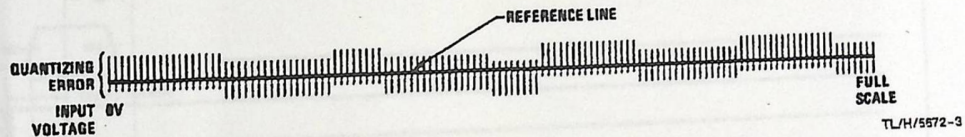
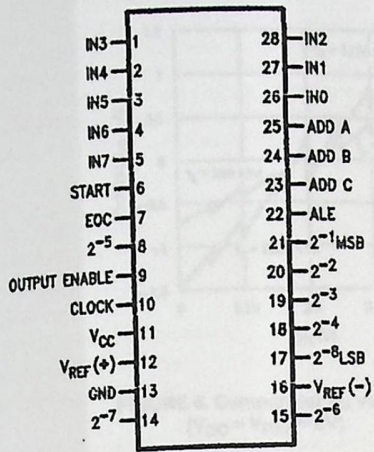


FIGURE 4. Typical Error Curve

Connection Diagrams

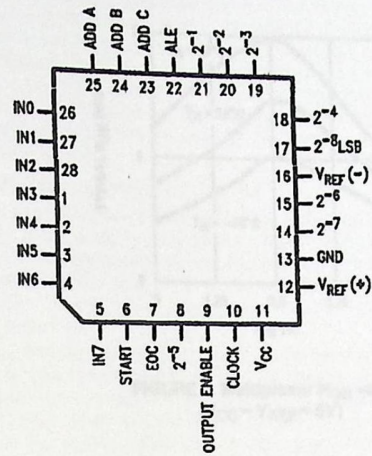
Dual-In-Line Package



TL/H/5672-11

Order Number ADC0808CCN, ADC0809CCN,
ADC0808CCJ or ADC0808CJ
See NS Package J28A or N28A

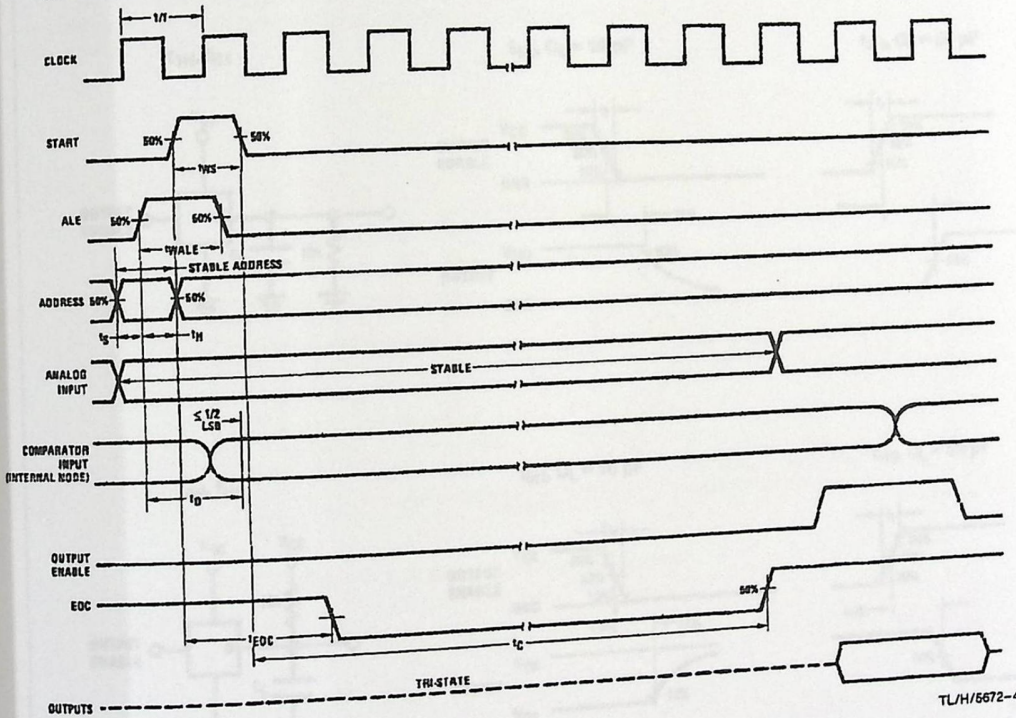
Molded Chip Carrier Package



TL/H/5672-12

Order Number ADC0808CCV or ADC0809CCV
See NS Package V28A

Timing Diagram



TL/H/5672-4

FIGURE 5

Typical Performance Characteristics

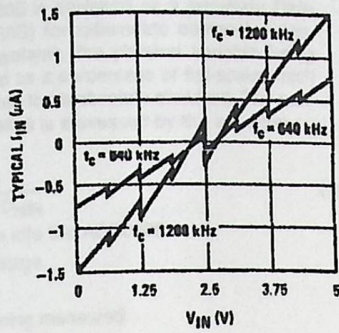


FIGURE 6. Comparator I_{IN} vs V_{IN}
($V_{CC} = V_{REF} = 5V$)

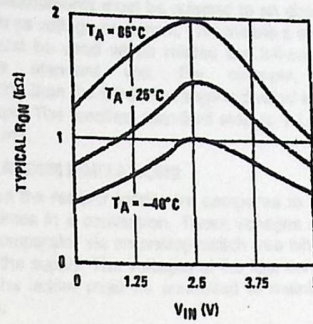
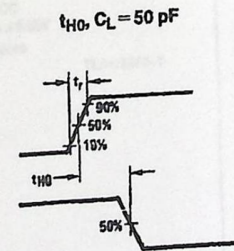
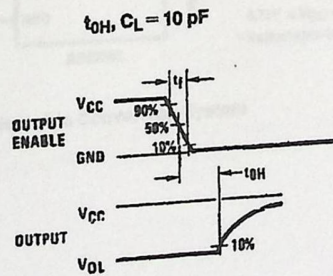
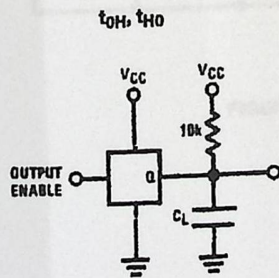
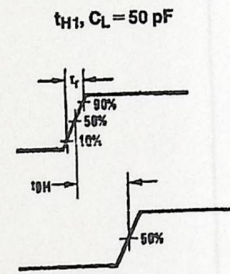
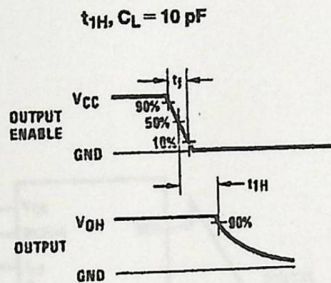
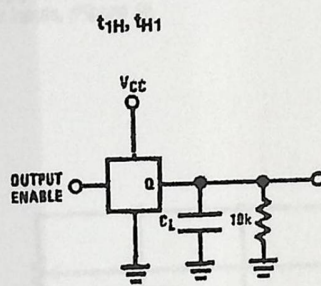


FIGURE 7. Multiplexer R_{ON} vs V_{IN}
($V_{CC} = V_{REF} = 5V$)

TL/H/5672-5

TRI-STATE Test Circuits and Timing Diagrams



TL/H/5672-6

FIGURE 8

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Applications Information

OPERATION

1.0 RATIOMETRIC CONVERSION

The ADC0808, ADC0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0808 is expressed by the equation

$$\frac{V_{IN}}{V_{FS} - V_Z} = \frac{D_x}{D_{MAX} - D_{MIN}} \quad (1)$$

V_{IN} = Input voltage into the ADC0808
 V_{FS} = Full-scale voltage
 V_Z = Zero voltage
 D_x = Data point being measured
 D_{MAX} = Maximum data limit
 D_{MIN} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0808, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, (Figure 9).

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} = 5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 RESISTOR LADDER LIMITATIONS

The voltages from the resistor ladder are compared to the selected into 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(-), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.

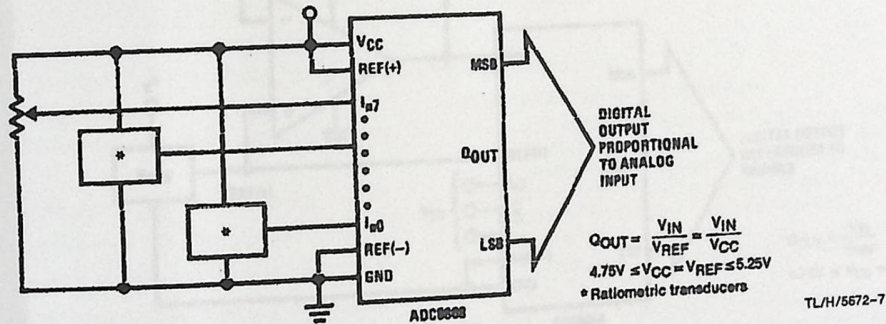


FIGURE 9. Ratiometric Conversion System

Applications Information (Continued)

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 μ F output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.

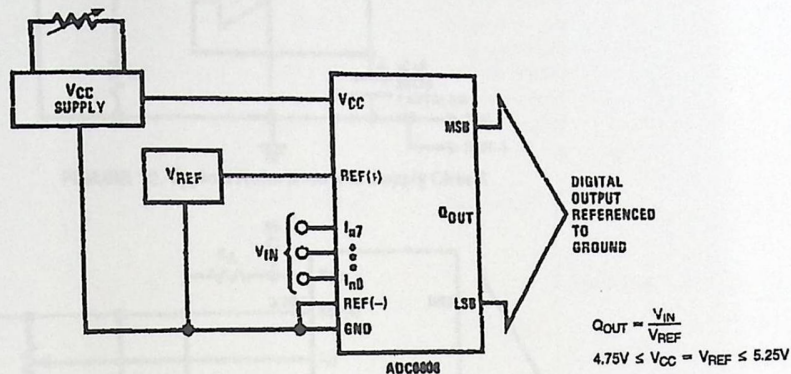


FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply

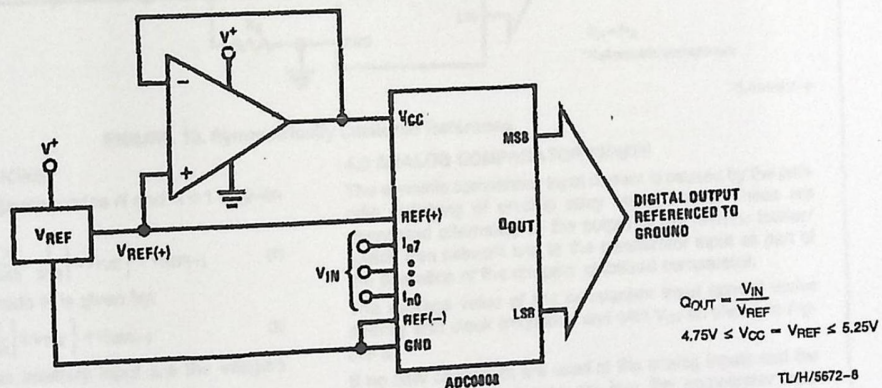


FIGURE 11: Ground Referenced Conversion System with Reference Generating V_{CC} Supply

Applications Information (Continued)

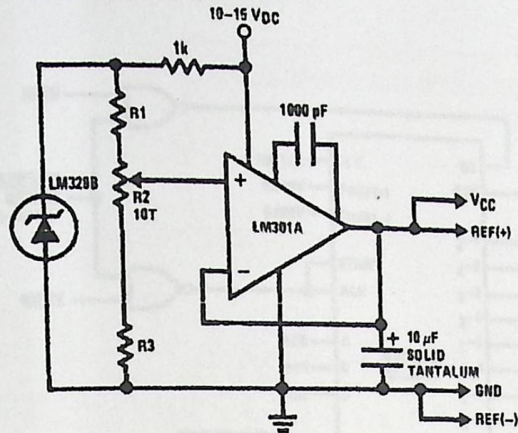


FIGURE 12. Typical Reference and Supply Circuit

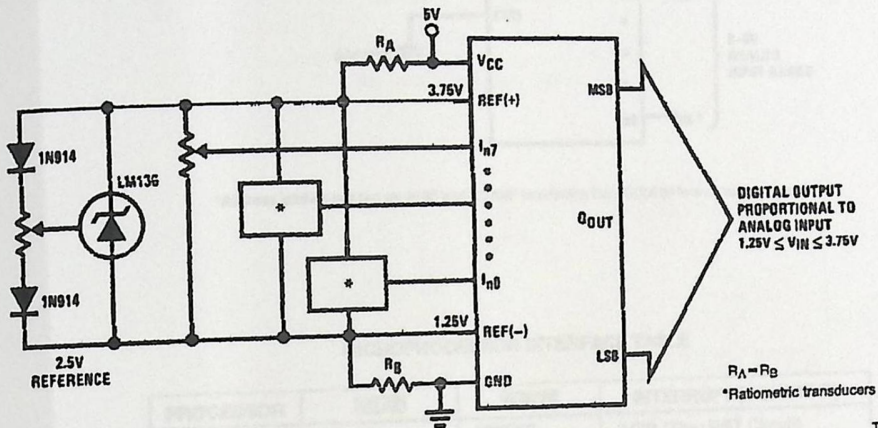


FIGURE 13. Symmetrically Centered Reference

3.0 CONVERTER EQUATIONS

The transition between adjacent codes N and $N + 1$ is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} + \frac{1}{512} \right] \pm V_{TUE} \right\} + V_{REF(-)} \quad (2)$$

The center of an output code N is given by:

$$V_{IN} \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} \right] \pm V_{TUE} \right\} + V_{REF(-)} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy} \quad (4)$$

where: V_{IN} = Voltage at comparator input

$V_{REF(+)}$ = Voltage at Ref(+)

$V_{REF(-)}$ = Voltage at Ref(-)

V_{TUE} = Total unadjusted error voltage (typically

$V_{REF(+)} \div 512$)

4.0 ANALOG COMPARATOR INPUTS

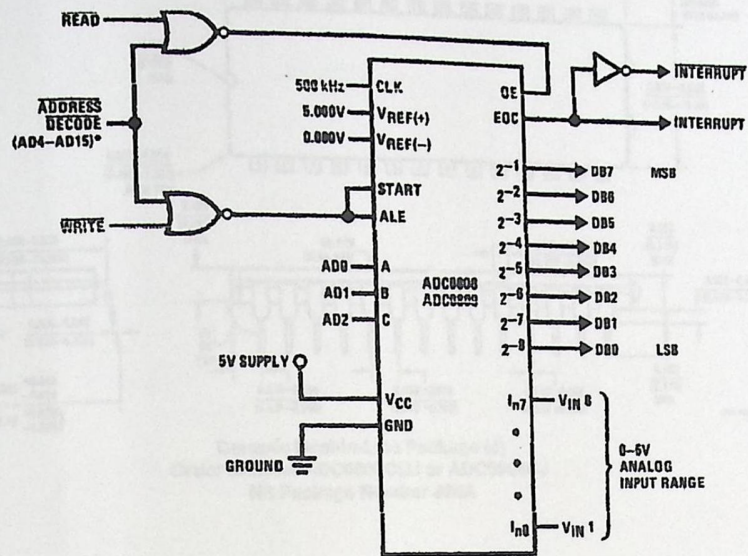
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in Figure 6.

If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.

Typical Application



TL/H/5672-10

*Address latches needed for 8085 and SC/MP interfacing the ADC0808 to a microprocessor

MICROPROCESSOR INTERFACE TABLE

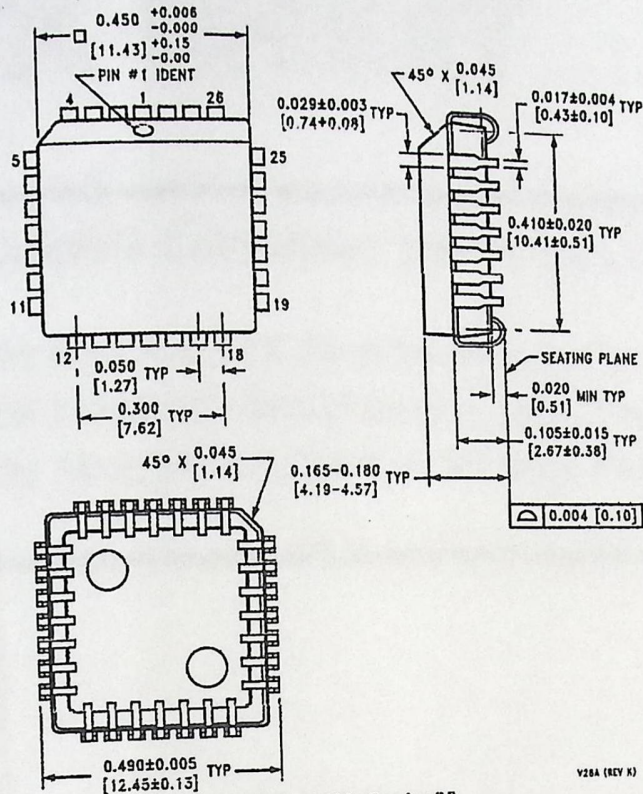
PROCESSOR	READ	WRITE	INTERRUPT (COMMENT)
8080	MEMR	MEMW	INTR (Thru RST Circuit)
8085	RD	WR	INTR (Thru RST Circuit)
Z-80	RD	WR	INT (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA ϕ 2 ϕ R/W	VMA ϕ ϕ R/W	TRQA or TRQB (Thru PIA)

Ordering Information

TEMPERATURE RANGE		-40°C to +85°C			-55°C to +125°C
Error	$\pm 1/2$ LSB Unadjusted	ADC0808CCN	ADC0808CCV	ADC0808CCJ	ADC0808CJ
	± 1 LSB Unadjusted	ADC0809CCN	ADC0809CCV		
Package Outline		N28A Molded DIP	V28A Molded Chip Carrier	J28A Ceramic DIP	J28A Ceramic DIP

<http://www.national.com>

Physical Dimensions inches (millimeters) (Continued)



Molded Chip Carrier (V)
Order Number ADC0808CCV or ADC0809CCV
NS Package Number V28A

V28A (REV X)

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DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT138

3-to-8 line decoder/demultiplexer; inverting

September 1993

Product specification
File under Integrated Circuits, IC06

Philips
Semiconductors



PHILIPS

3-to-8 line decoder/demultiplexer; inverting

74HC/HCT138

FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- Output capability: standard
- Icc category: MSI

GENERAL DESCRIPTION

The 74HC/HCT138 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT138 decoders accept three binary weighted address inputs (A_0, A_1, A_2) and when enabled, provide 8 mutually exclusive active LOW outputs (\bar{Y}_0 to \bar{Y}_7).

The "138" features three enable inputs: two active LOW (\bar{E}_1 and \bar{E}_2) and one active HIGH (E_3). Every output will be HIGH unless \bar{E}_1 and \bar{E}_2 are LOW and E_3 is HIGH.

This multiple enable function allows easy parallel expansion of the "138" to a 1-of-32 (5 lines to 32 lines) decoder with just four "138" ICs and one inverter.

The "138" can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The "138" is identical to the "238" but has inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL} / t_{PLH}	propagation delay	$C_L = 15\text{ pF}; V_{CC} = 5\text{ V}$			
	A_n to \bar{Y}_n		12	17	ns
t_{PHL} / t_{PLH}	E_3 to \bar{Y}_n		14	19	ns
	E_n to \bar{Y}_n				
C_i	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	67	67	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_1 = \text{GND to } V_{CC}$
For HCT the condition is $V_1 = \text{GND to } V_{CC} - 1.5\text{ V}$

ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

3-to-8 line decoder/demultiplexer; inverting

74HC/HCT138

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5	\bar{E}_1, \bar{E}_2	enable inputs (active LOW)
6	E_3	enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	\bar{Y}_0 to \bar{Y}_7	outputs (active LOW)
16	V_{CC}	positive supply voltage

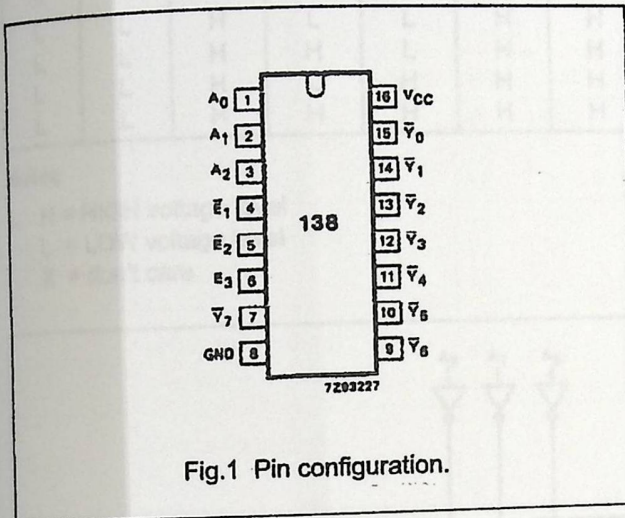


Fig.1 Pin configuration.

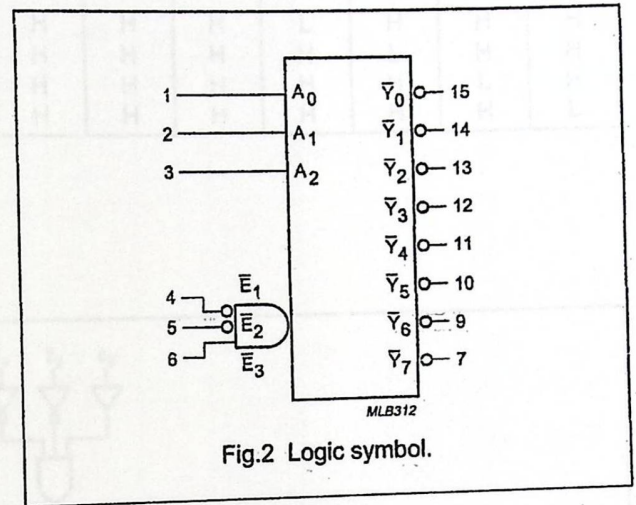


Fig.2 Logic symbol.

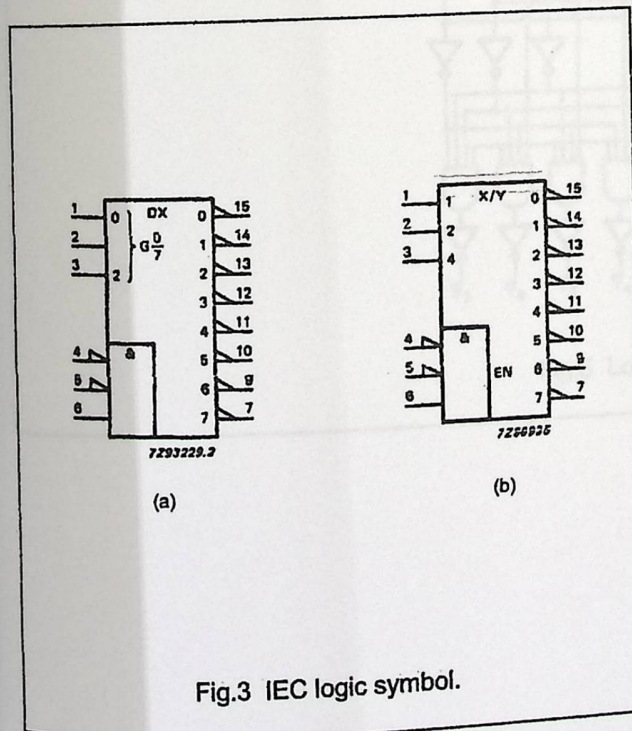


Fig.3 IEC logic symbol.

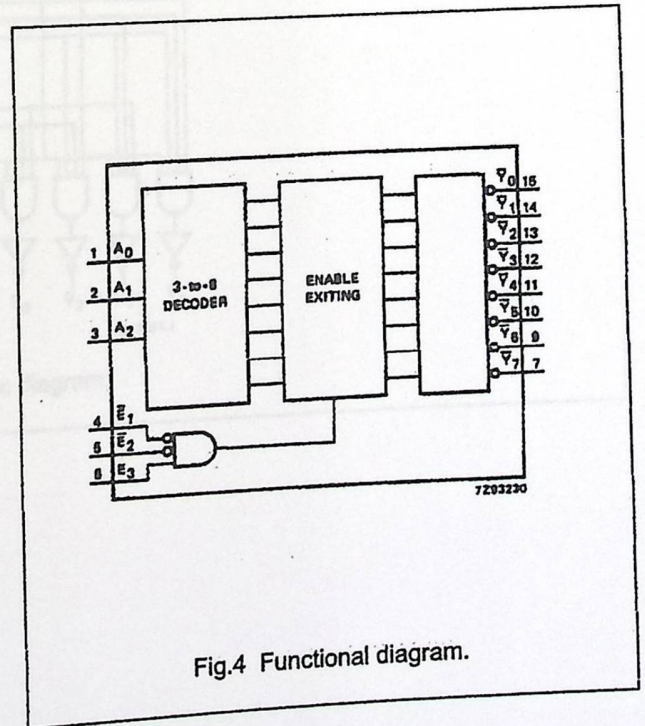


Fig.4 Functional diagram.

3-to-8 line decoder/demultiplexer; inverting

74HC/HCT138

FUNCTION TABLE

INPUTS						OUTPUTS							
\bar{E}_1	\bar{E}_2	E_3	A_0	A_1	A_2	\bar{Y}_0	\bar{Y}_1	\bar{Y}_2	\bar{Y}_3	\bar{Y}_4	\bar{Y}_5	\bar{Y}_6	\bar{Y}_7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	L	L	L	H	H	H	H	H	L	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L

Notes

- H = HIGH voltage level
L = LOW voltage level
X = don't care

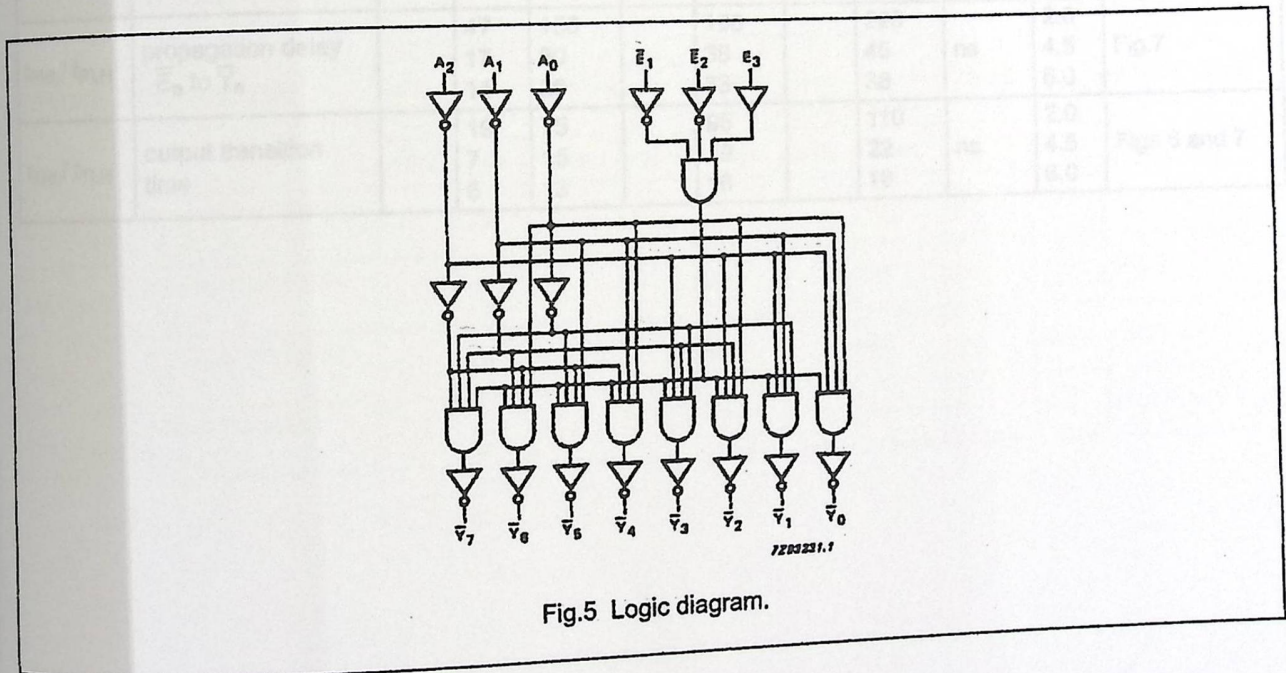


Fig.5 Logic diagram.

3-to-8 line decoder/demultiplexer; inverting

74HC/HCT138

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} /t _{PLH}	propagation delay A _n to \bar{Y}_n		41	150		190		225	ns	2.0 4.5 6.0	Fig.6
			15	30		38		45			
			12	26		33		38			
t _{PHL} /t _{PLH}	propagation delay E ₃ to \bar{Y}_n		47	150		190		225	ns	2.0 4.5 6.0	Fig.6
			17	30		38		45			
			14	26		33		38			
t _{PHL} /t _{PLH}	propagation delay \bar{E}_n to \bar{Y}_n		47	150		190		225	ns	2.0 4.5 6.0	Fig.7
			17	30		38		45			
			14	26		33		38			
t _{THL} /t _{TLH}	output transition time		19	75		95		110	ns	2.0 4.5 6.0	Figs 6 and 7
			7	15		19		22			
			6	13		16		19			

3-to-8 line decoder/demultiplexer; inverting

74HC/HCT138

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A _n	1.50
\bar{E}_n	1.25
E ₃	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HCT							V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} /t _{PLH}	propagation delay A _n to \bar{Y}_n		20	35		44		53	ns	4.5	Fig.6
t _{PHL} /t _{PLH}	propagation delay E ₃ to \bar{Y}_n		18	40		50		60	ns	4.5	Fig.6
t _{PHL} /t _{PLH}	propagation delay \bar{E}_n to \bar{Y}_n		19	40		50		60	ns	4.5	Fig.7
t _{THL} /t _{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7

3-to-8 line decoder/demultiplexer; inverting

74HC/HCT138

AC WAVEFORMS

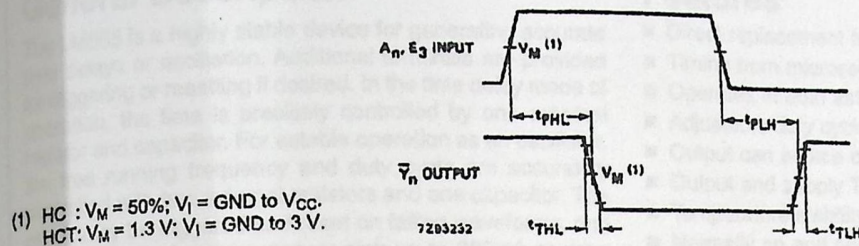


Fig.6 Waveforms showing the address input (A_n) and enable input (E_3) to output (\bar{Y}_n) propagation delays and the output transition times.

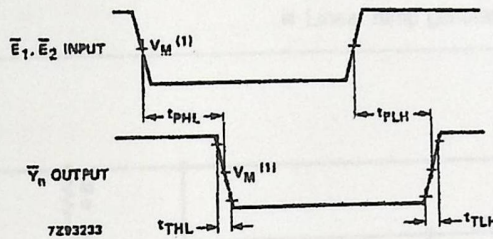


Fig.7 Waveforms showing the enable input (\bar{E}_n) to output (\bar{Y}_n) propagation delays and the output transition times.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".

LM555 Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

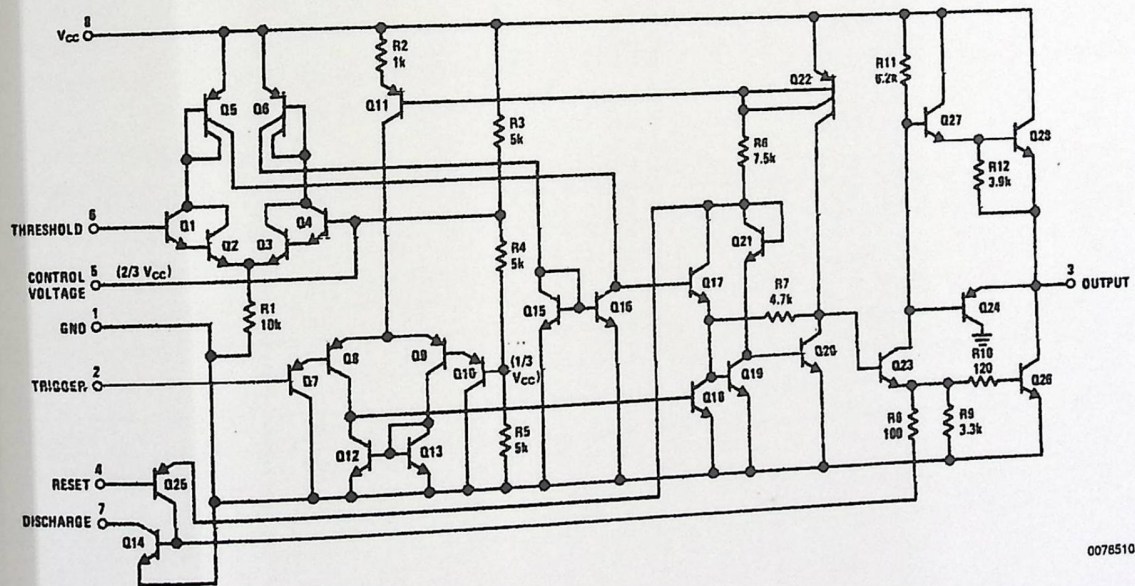
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output
- Available in 8-pin MSOP package

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

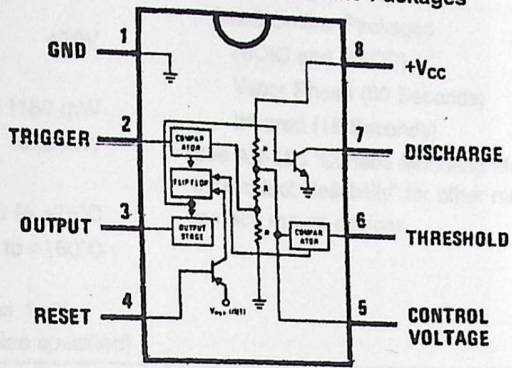
Schematic Diagram



00785101

Connection Diagram

Dual-In-Line, Small Outline and Molded Mini Small Outline Packages



Top View

00785103

Ordering Information

Package	Part Number	Package Marking	Media Transport	NSC Drawing
8-Pin SOIC	LM555CM	LM555CM	Rails	M08A
	LM555CMX	LM555CM	2.5k Units Tape and Reel	
8-Pin MSOP	LM555CMM	Z55	1k Units Tape and Reel	MUA08A
	LM555CMMX	Z55	3.5k Units Tape and Reel	
8-Pin MDIP	LM555CN	LM555CN	Rails	N08E

Absolute Maximum Ratings (Note 2)
 If Military/Aerospace specified devices are required,
 please contact the National Semiconductor Sales Office/
 Distributors for availability and specifications.

Supply Voltage	+18V
Power Dissipation (Note 3)	
LM555CM, LM555CN	1180 mW
LM555CMM	613 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 Seconds)	260°C
Small Outline Packages (SOIC and MSOP)	
Vapor Phase (60 Seconds)	215°C
Infrared (15 Seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Notes 1, 2)
 (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
Supply Voltage		4.5		16	V
Supply Current	V _{CC} = 5V, R _L = ∞ V _{CC} = 15V, R _L = ∞ (Low State) (Note 4)		3 10	6 15	mA
Timing Error, Monostable			1		%
Initial Accuracy			50		ppm/°C
Drift with Temperature	R _A = 1k to 100kΩ, C = 0.1μF, (Note 5)				%
Accuracy over Temperature			1.5		%/V
Drift with Supply			0.1		%/V
Timing Error, Astable			2.25		%
Initial Accuracy			150		ppm/°C
Drift with Temperature	R _A , R _B = 1k to 100kΩ, C = 0.1μF, (Note 5)				%
Accuracy over Temperature			3.0		%/V
Drift with Supply			0.30		%/V
Threshold Voltage			0.667		x V _{CC}
Trigger Voltage	V _{CC} = 15V V _{CC} = 5V		5 1.67		V V
Trigger Current			0.5	0.9	μA
Reset Voltage		0.4	0.5	1	V
Reset Current			0.1	0.4	mA
Threshold Current	(Note 6)		0.1	0.25	μA
Control Voltage Level	V _{CC} = 15V V _{CC} = 5V	9 2.6	10 3.33	11 4	V nA
Pin 7 Leakage Output High					mV
Pin 7 Sat (Note 7)			180		mV
Output Low	V _{CC} = 15V, I ₇ = 15mA		80	200	mV
Output Low	V _{CC} = 4.5V, I ₇ = 4.5mA				mV

Electrical Characteristics (Notes 1, 2) (Continued)

($T_A = 25^\circ\text{C}$, $V_{CC} = +5\text{V}$ to $+15\text{V}$, unless otherwise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
Output Voltage Drop (Low)	$V_{CC} = 15\text{V}$				
	$I_{\text{SINK}} = 10\text{mA}$		0.1	0.25	V
	$I_{\text{SINK}} = 50\text{mA}$		0.4	0.75	V
	$I_{\text{SINK}} = 100\text{mA}$		2	2.5	V
	$I_{\text{SINK}} = 200\text{mA}$		2.5		V
	$V_{CC} = 5\text{V}$				
Output Voltage Drop (High)	$I_{\text{SOURCE}} = 200\text{mA}$, $V_{CC} = 15\text{V}$		12.5		V
	$I_{\text{SOURCE}} = 100\text{mA}$, $V_{CC} = 15\text{V}$	12.75	13.3		V
	$V_{CC} = 5\text{V}$	2.75	3.3		V
Rise Time of Output			100		ns
Fall Time of Output			100		ns

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at elevated temperatures the device must be derated above 25°C based on a $+150^\circ\text{C}$ maximum junction temperature and a thermal resistance of 106°C/W (DIP), 170°C/W (S0-8), and 204°C/W (MSOP) junction to ambient.

Note 4: Supply current when output high typically 1 mA less at $V_{CC} = 5\text{V}$.

Note 5: Tested at $V_{CC} = 5\text{V}$ and $V_{CC} = 15\text{V}$.

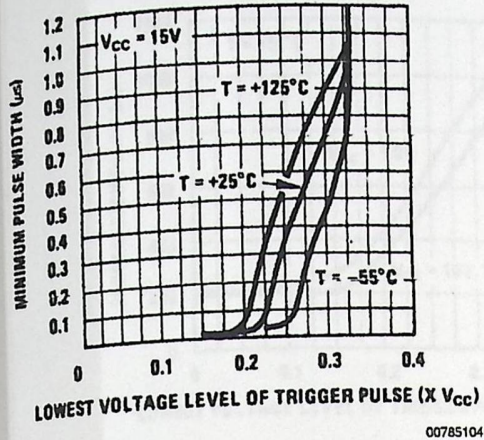
Note 6: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is $20\text{M}\Omega$.

Note 7: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Note 8: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

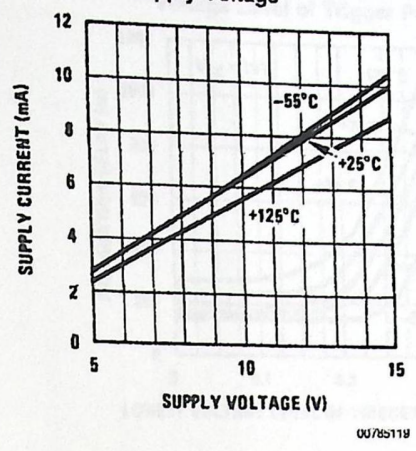
Typical Performance Characteristics

Minimum Pulse Width Required for Triggering



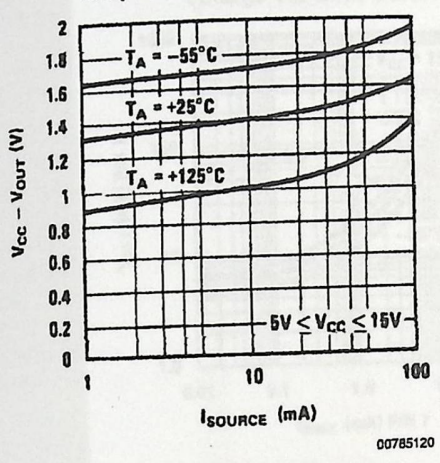
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Supply Current vs. Supply Voltage



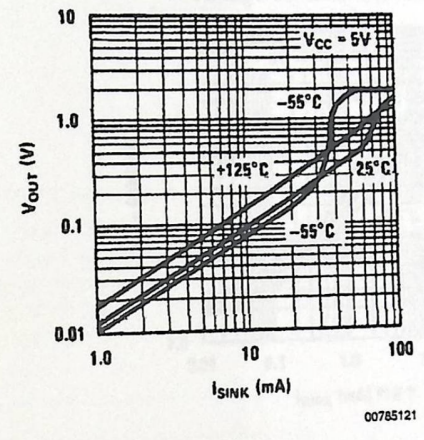
00785119

High Output Voltage vs. Output Source Current



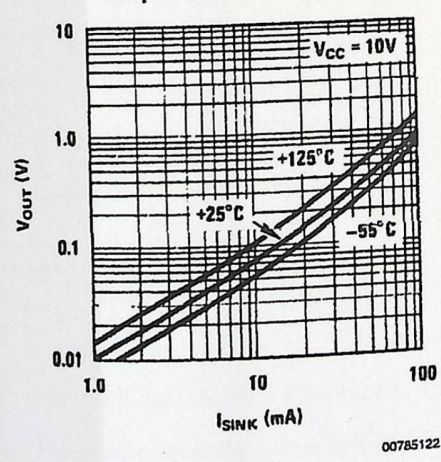
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Low Output Voltage vs. Output Sink Current



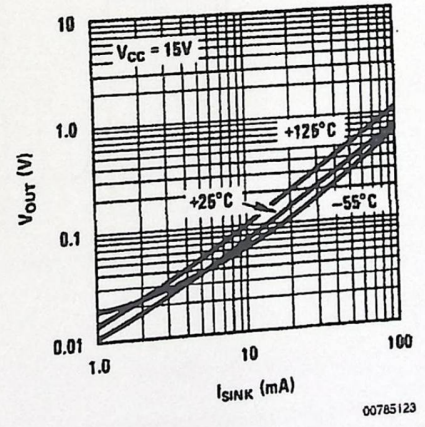
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Low Output Voltage vs. Output Sink Current



00785122

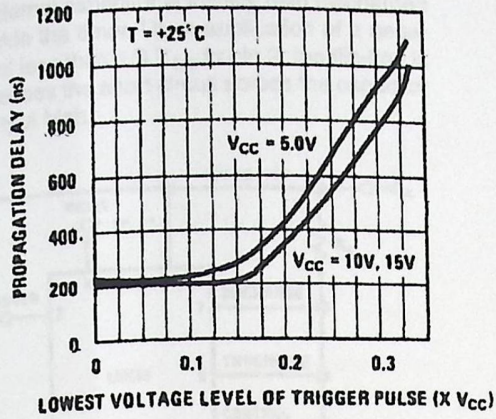
Low Output Voltage vs. Output Sink Current



00785123

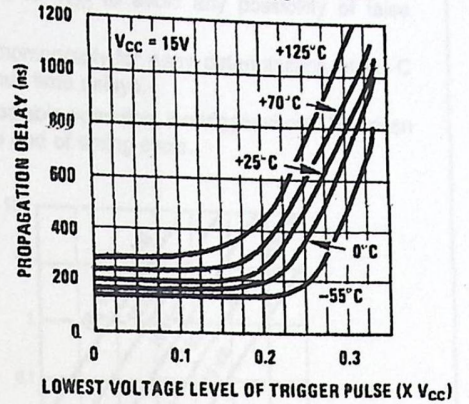
Typical Performance Characteristics (Continued)

Output Propagation Delay vs. Voltage Level of Trigger Pulse



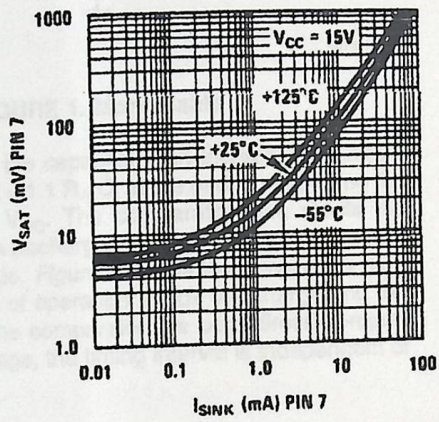
00785124

Output Propagation Delay vs. Voltage Level of Trigger Pulse



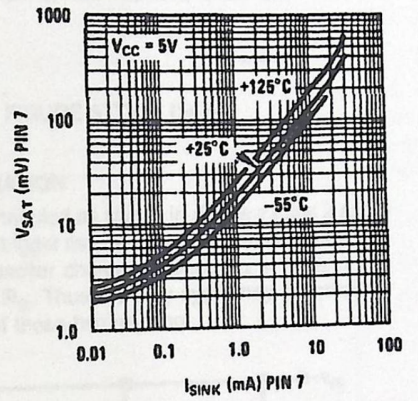
00785125

Discharge Transistor (Pin 7) Voltage vs. Sink Current



00785126

Discharge Transistor (Pin 7) Voltage vs. Sink Current

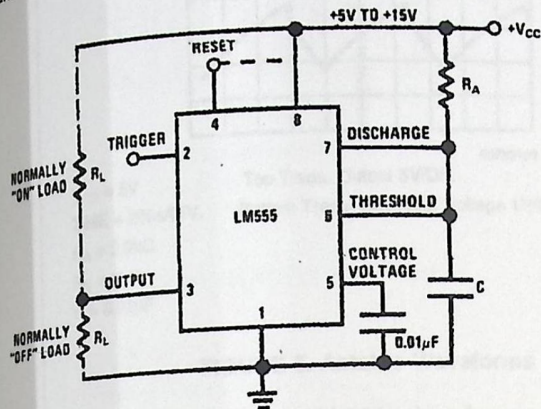


00785127

Applications Information

MONOSTABLE OPERATION

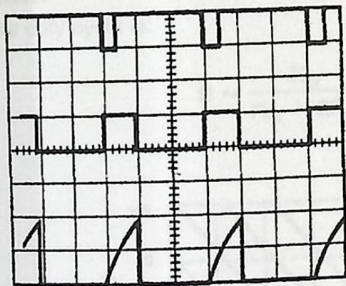
In this mode of operation, the timer functions as a one-shot (Figure 1). The external capacitor is initially held discharged (Figure 1). Upon application of a negative trigger pulse of less than $1/3 V_{CC}$ to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.



00785105

FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of $t = 1.1 R_A C$, at the end of which time the voltage equals $2/3 V_{CC}$. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. Figure 2 shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply.



00785106

$V_{CC} = 5V$
 TIME = 0.1 ms/DIV.
 $R_A = 9.1k\Omega$
 $C = 0.01\mu F$

Top Trace: Input 5V/Div.
 Middle Trace: Output 5V/Div.
 Bottom Trace: Capacitor Voltage 2V/Div.

FIGURE 2. Monostable Waveforms

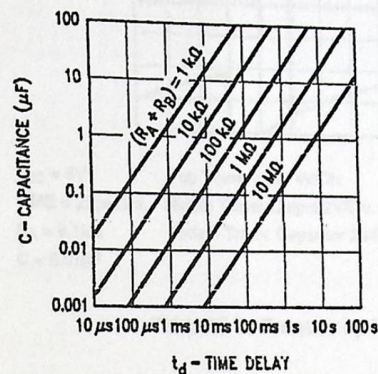
During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least $10\mu s$ before the end of the timing interval. However the circuit can be reset

during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

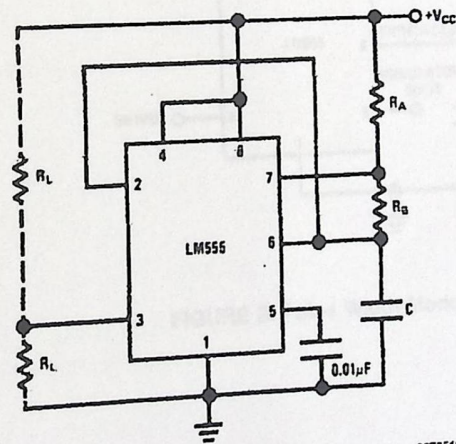


00785107

FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in Figure 4 (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B . Thus the duty cycle may be precisely set by the ratio of these two resistors.



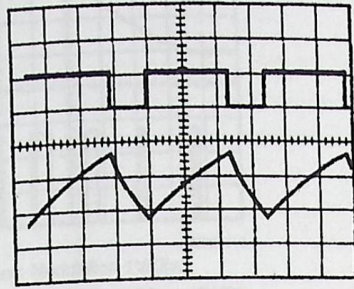
00785108

FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between $1/3 V_{CC}$ and $2/3 V_{CC}$. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Applications Information (Continued)

Figure 5 shows the waveforms generated in this mode of operation.



00785109

$V_{CC} = 5V$
 TIME = 20 μ s/DIV. Top Trace: Output 5V/Div.
 $R_A = 3.9k\Omega$ Bottom Trace: Capacitor Voltage 1V/Div.
 $R_B = 3k\Omega$
 $C = 0.01\mu F$

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693 (R_A + R_B) C$$

And the discharge time (output low) by:

$$t_2 = 0.693 (R_B) C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693 (R_A + 2R_B) C$$

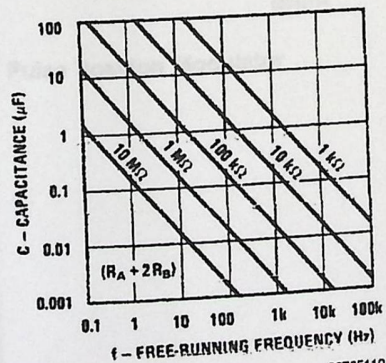
The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B) C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

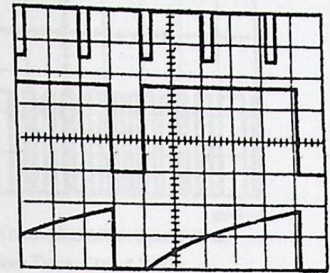


00785110

FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of Figure 1 can be used as a frequency divider by adjusting the length of the timing cycle. Figure 7 shows the waveforms generated in a divide by three circuit.



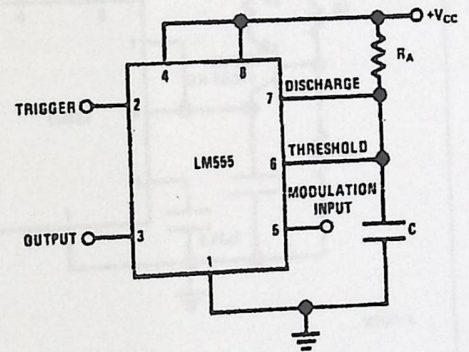
00785111

$V_{CC} = 5V$ Top Trace: Input 4V/Div.
 TIME = 20 μ s/DIV. Middle Trace: Output 2V/Div.
 $R_A = 9.1k\Omega$ Bottom Trace: Capacitor 2V/Div.
 $C = 0.01\mu F$

FIGURE 7. Frequency Divider

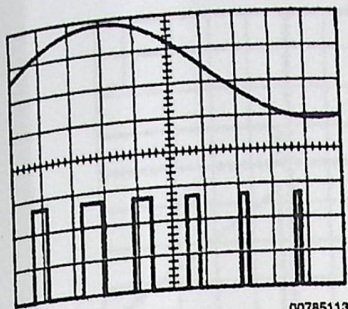
PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. Figure 8 shows the circuit, and in Figure 9 are some waveform examples.



00785112

FIGURE 8. Pulse Width Modulator

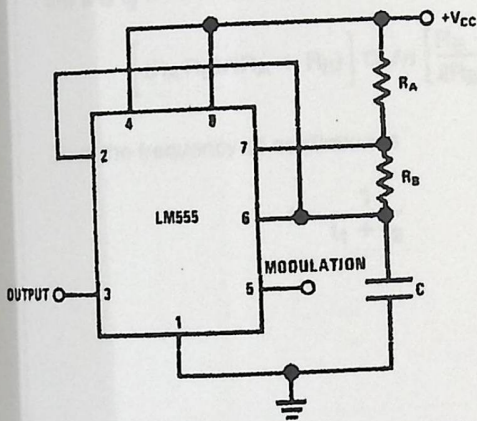


00785113
 Top Trace: Modulation 1V/Div.
 Bottom Trace: Output Voltage 2V/Div.
 $V_{CC} = 5V$
 $TIME = 0.2 \text{ ms/DIV.}$
 $R_A = 9.1k\Omega$
 $C = 0.01\mu F$

FIGURE 9. Pulse Width Modulator

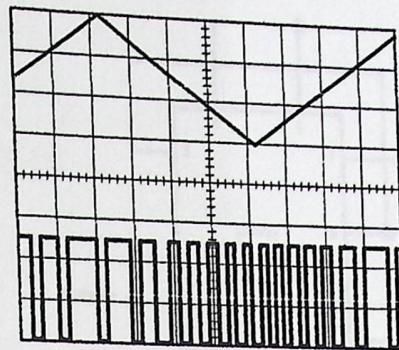
PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in Figure 10, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure 11 shows the waveforms generated for a triangle wave modulation signal.



00785114

FIGURE 10. Pulse Position Modulator

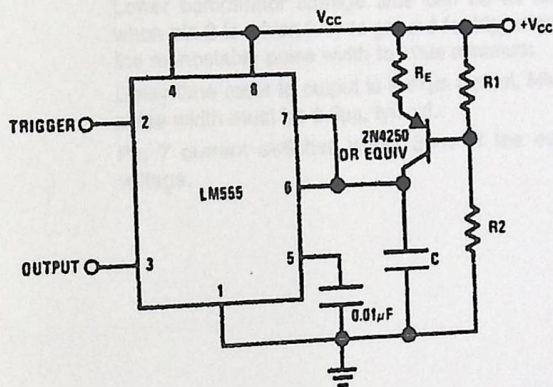


00785115
 Top Trace: Modulation Input 1V/Div.
 Bottom Trace: Output 2V/Div.
 $V_{CC} = 5V$
 $TIME = 0.1 \text{ ms/DIV.}$
 $R_A = 3.9k\Omega$
 $R_B = 3k\Omega$
 $C = 0.01\mu F$

FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A , in the monostable circuit is replaced by a constant current source, a linear ramp is generated. Figure 12 shows a circuit configuration that will perform this function.



00785116

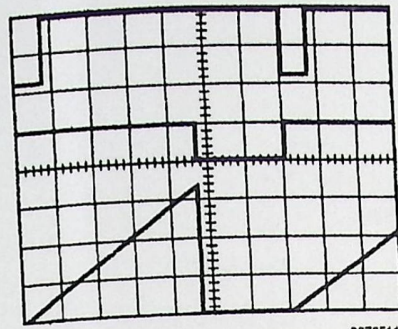
FIGURE 12.

Figure 13 shows waveforms generated by the linear ramp. The time interval is given by:

$$T = \frac{2/3 V_{CC} R_E (R_1 + R_2) C}{R_1 V_{CC} - V_{BE} (R_1 + R_2)}$$

$V_{BE} \approx 0.6V$

$V_{BE} \approx 0.6V$



00785117

$V_{CC} = 5V$
 TIME = 20 μs /DIV.
 $R_1 = 47k\Omega$
 $R_2 = 100k\Omega$
 $R_E = 2.7 k\Omega$
 $C = 0.01 \mu F$

FIGURE 13. Linear Ramp

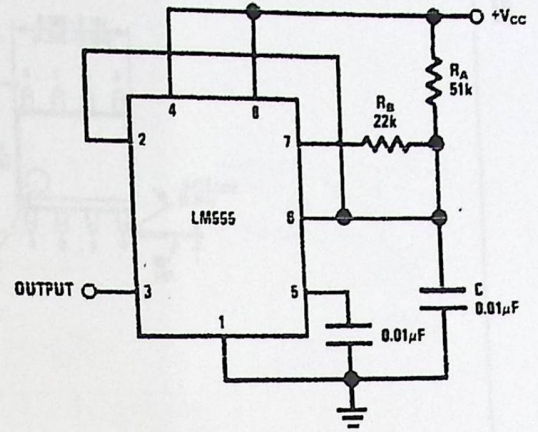
50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in Figure 14. The time period for the output high is the same as previous, $t_1 = 0.693 R_A C$. For the output low it is $t_2 =$

$$\left[\frac{(R_A R_B)}{(R_A + R_B)} \right] C \ln \left[\frac{R_B - 2R_A}{2R_B - R_A} \right]$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2}$$



00785118

FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than $1/2 R_A$ because the junction of R_A and R_B cannot bring pin 2 down to $1/3 V_{CC}$ and trigger the lower comparator.

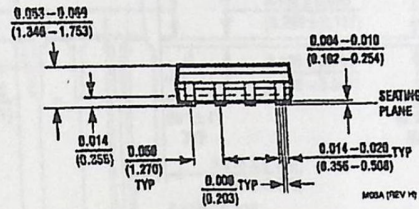
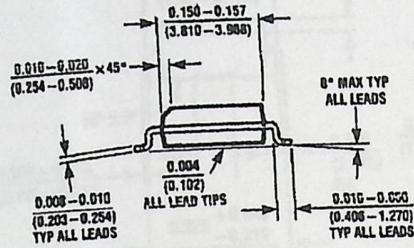
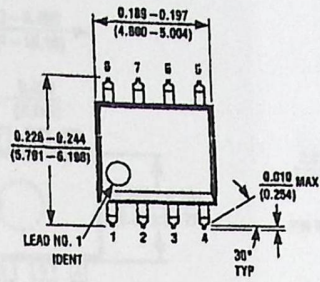
ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1 μF in parallel with 1 μF electrolytic.

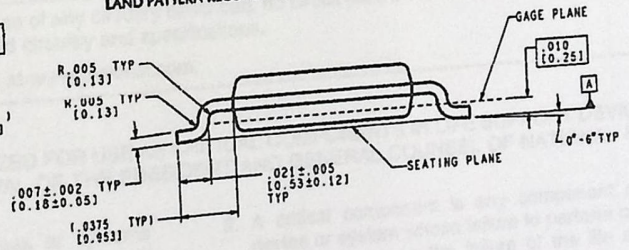
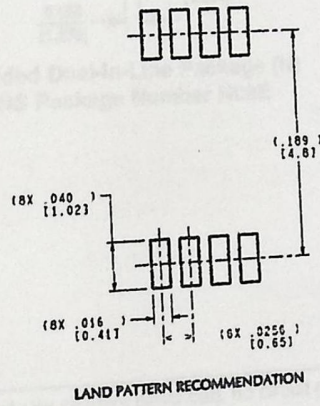
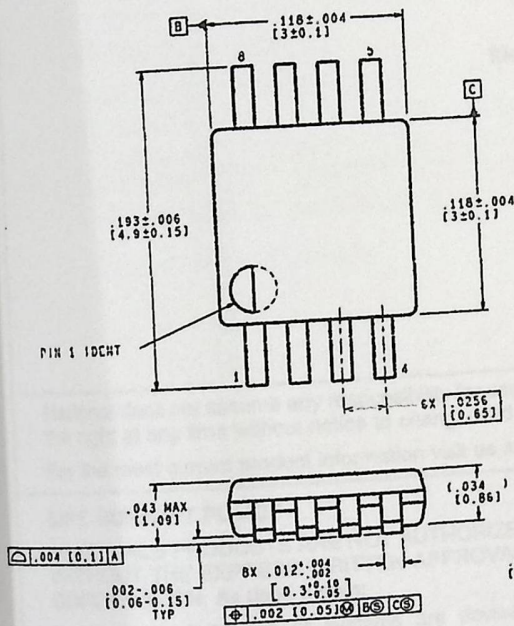
Lower comparator storage time can be as long as 10 μs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10 μs minimum.

Delay time reset to output is 0.47 μs typical. Minimum reset pulse width must be 0.3 μs , typical.

Pin 7 current switches within 30ns of the output (pin 3) voltage.



Small Outline Package (M)
NS Package Number M08A

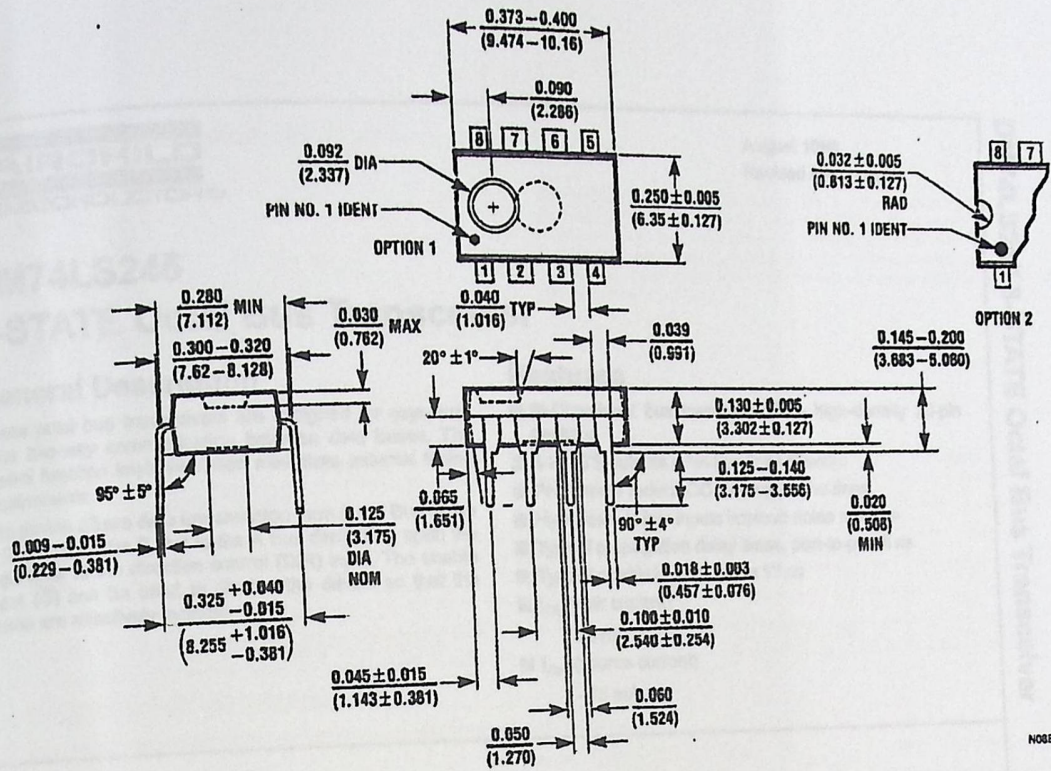


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MUA08A (Rev E)

8-Lead (0.118" Wide) Molded Mini Small Outline Package
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
NS Package Number N08E

NO8E (REV F)

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Tel: 81-3-5639-7560

DM74LS245 3-STATE Octal Bus Transceiver

General Description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A Bus to the B Bus or from the B Bus to the A Bus depending upon the logic level at the direction control (DIR) input. The enable input (\bar{G}) can be used to disable the device so that the buses are effectively isolated.

Features

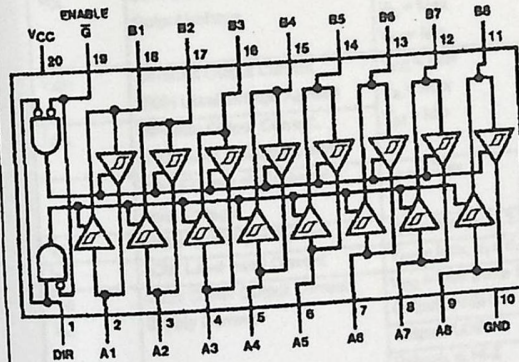
- Bi-Directional bus transceiver in a high-density 20-pin package
- 3-STATE outputs drive bus lines directly
- PNP Inputs reduce DC loading on bus lines
- Hysteresis at bus inputs improve noise margins
- Typical propagation delay times, port-to-port 8 ns
- Typical enable/disable times 17 ns
- I_{OL} (sink current)
24 mA
- I_{OH} (source current)
-15 mA

Ordering Code:

Order Number	Package Number	Package Description
DM74LS245WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74LS245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS245N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Enable \bar{G}	Direction Control DIR	Operation
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

H = HIGH Level
L = LOW Level
X = Irrelevant

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	
DIR or \bar{G}	7V
A or B	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			-15	mA
I_{OL}	LOW Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -18 \text{ mA}$			-1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{Min}$	0.2	0.4		V
V_{OH}	HIGH Level Output Voltage	$V_{CC} = \text{Min}, V_{IH} = \text{Min}$	2.7			V
		$V_{IL} = \text{Max}, I_{OH} = -1 \text{ mA}$				
		$V_{CC} = \text{Min}, V_{IL} = \text{Min}$	2.4	3.4		
		$V_{IL} = \text{Max}, I_{OH} = -3 \text{ mA}$				
V_{OL}	LOW Level Output Voltage	$V_{CC} = \text{Min}, V_{IH} = \text{Min}$	2			V
		$V_{IL} = 0.5V, I_{OH} = \text{Max}$			0.4	
V_{OL}	LOW Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = 12 \text{ mA}$			0.5	V
		$V_{IL} = \text{Max}, I_{OL} = \text{Max}$				
I_{OZH}	Off-State Output Current, HIGH Level Voltage Applied	$V_{CC} = \text{Max}, V_{IL} = \text{Max}, V_{IH} = \text{Min}$			20	μA
I_{OZL}	Off-State Output Current, LOW Level Voltage Applied	$V_{OH} = 2.7V, V_{OH} = 0.4V$			-200	μA
I_I	Input Current at Maximum Input Voltage	$V_{CC} = \text{Max}, V_I = 5.5V$			0.1	mA
		DIR or $\bar{G}, V_I = 7V$			0.1	
I_{IH}	HIGH Level Input Current	$V_{CC} = \text{Max}, V_I = 2.7V$			20	μA
I_{IL}	LOW Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4V$	-40		-0.2	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 3)			-225	mA
I_{CC}	Supply Current	Outputs HIGH			48	mA
		Outputs LOW			62	
		Outputs at HI-Z			64	

Note 2: All typicals are at $V_{CC} = 5V, T_A = 25^\circ\text{C}$.

Note 3: Not more than one output should be shorted at a time, not to exceed one second duration

Switching Characteristics

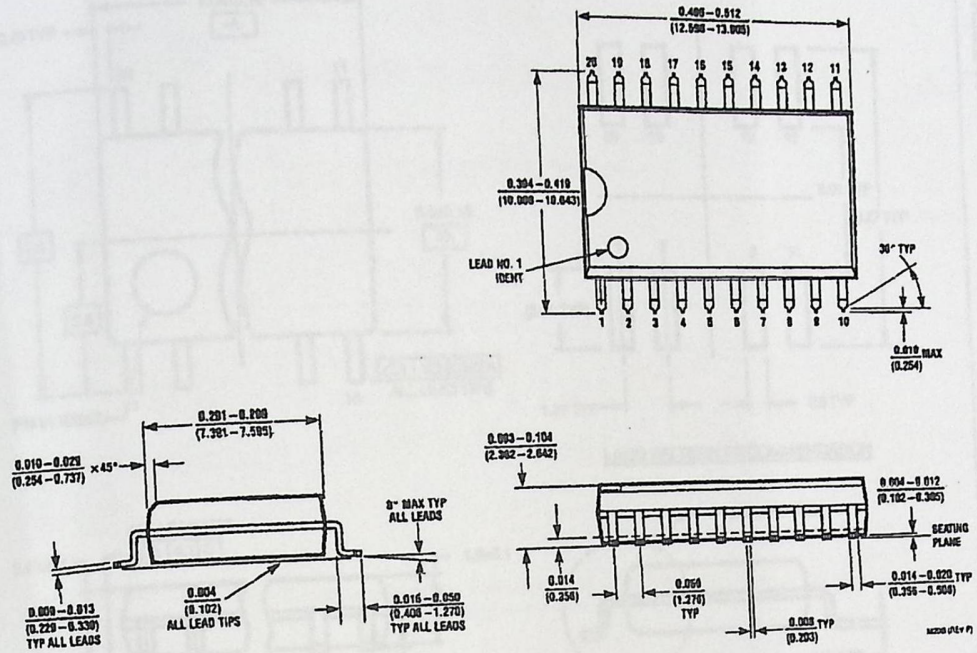
$V_{CC} = 5V, T_A = 25^\circ C$

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output	$C_L = 45 \text{ pF}$ $R_L = 667\Omega$		12	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output			12	ns
t_{PZL}	Output Enable Time to LOW Level			40	ns
t_{PZH}	Output Enable Time to HIGH Level			40	ns
t_{PLZ}	Output Disable Time from LOW Level	$C_L = 5 \text{ pF}$ $R_L = 667\Omega$		25	ns
t_{PHZ}	Output Disable Time from HIGH Level			25	ns
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output	$C_L = 150 \text{ pF}$ $R_L = 667\Omega$		16	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output			17	ns
t_{PZL}	Output Enable Time to LOW Level			45	ns
t_{PZH}	Output Enable Time to HIGH Level			45	ns

DM74ALS245

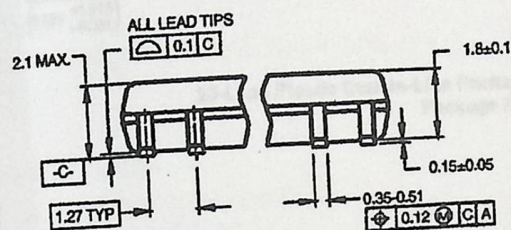
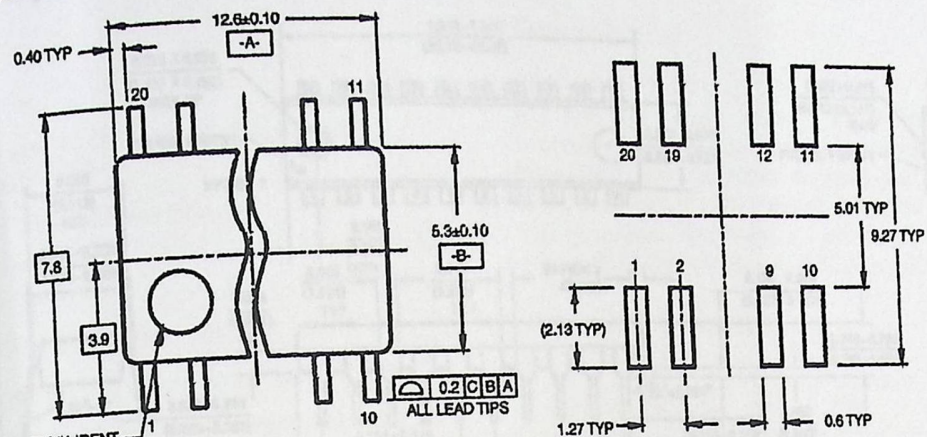
DM74LS245

Physical Dimensions Inches (millimeters) unless otherwise noted

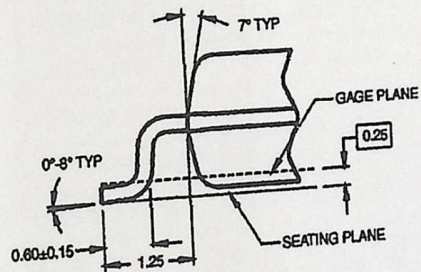
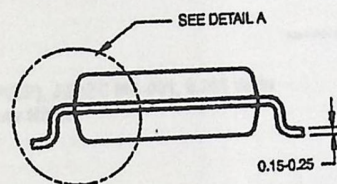


20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide Package Number M20B

Physical Dimensions Inches (millimeters) unless otherwise noted (Continued)



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DETAIL A

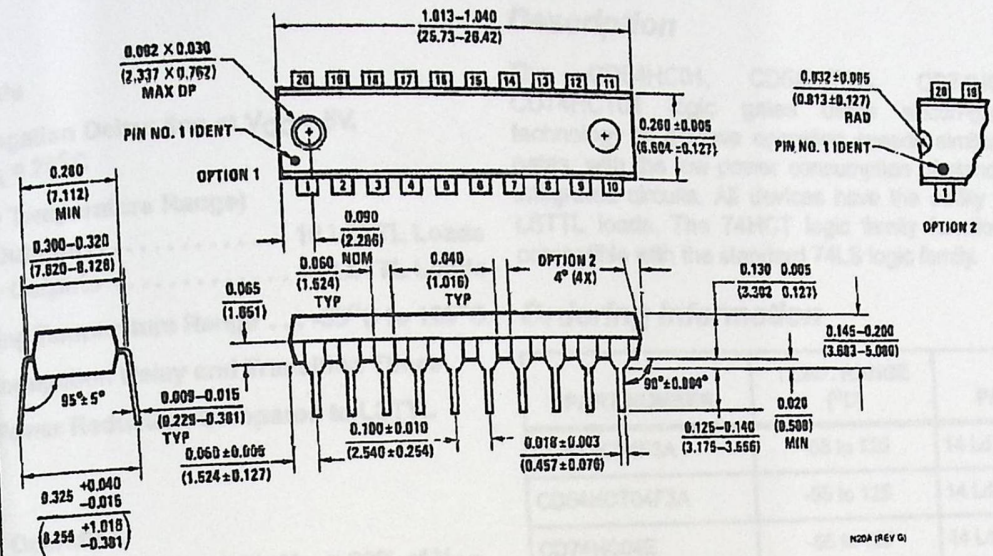
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 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRovB1

20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
 Package Number M20D

DM74LS245 3-STATE Octal Bus Transceiver

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N20A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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High-Speed CMOS Logic Hex Inverter

Features

- Buffered Inputs
- Typical Propagation Delay: 6ns at $V_{CC} = 5V$, $C_L = 15pF$, $T_A = 25^\circ C$
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . $-55^\circ C$ to $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2-V to 6-V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5-V to 5.5-V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_1 \leq 1\mu A$ at V_{OL} , V_{OH}

Description

The CD54HC04, CD54HCT04, CD74HC04 and CD74HCT04 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates, with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 74HCT logic family functionally is pin compatible with the standard 74LS logic family.

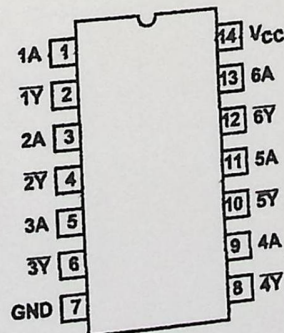
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC04F3A	-55 to 125	14 Ld CERDIP
CD54HCT04F3A	-55 to 125	14 Ld CERDIP
CD74HC04E	-55 to 125	14 Ld PDIP
CD74HC04M	-55 to 125	14 Ld SOIC
CD74HC04MT	-55 to 125	14 Ld SOIC
CD74HC04M96	-55 to 125	14 Ld SOIC
CD74HCT04E	-55 to 125	14 Ld PDIP
CD74HCT04M	-55 to 125	14 Ld SOIC
CD74HCT04MT	-55 to 125	14 Ld SOIC
CD74HCT04M96	-55 to 125	14 Ld SOIC
CD74HCT04PWR	-55 to 125	14 Ld TSSOP

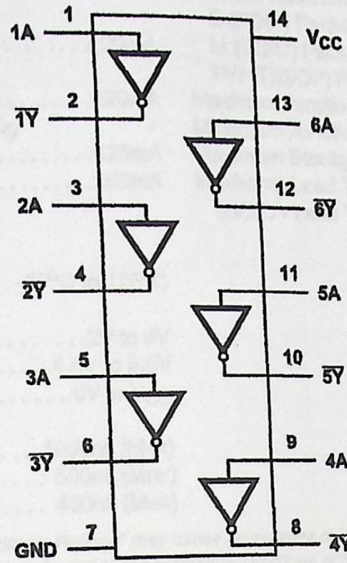
NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout

CD54HC04, CD54HCT04 (CERDIP)
CD74HC04 (PDIP, SOIC)
CD74HCT04 (PDIP, SOIC, TSSOP)
TOP VIEW



Functional Diagram



TRUTH TABLE

INPUTS	
nA	nY
L	H
H	L

H = High Voltage Level, L = Low Voltage Level

Logic Symbol



CD54HC04, CD74HC04, CD54HCT04, CD74HCT04

Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 7V
DC Input Diode Current, I_{IK} For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK} For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, I_O For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC} or I_{GND}	$\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^{\circ}C/W$)
E (PDIP) Package	80
M (SOIC) Package	86
PW (TSSOP) Package	113
Maximum Junction Temperature (Hermetic Package or Die)	175 $^{\circ}C$
Maximum Junction Temperature (Plastic Package)	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$ (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range (T_A)	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, V_{CC}	
HC Types	2V to 6V
HCT Types	4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O	0V to V_{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating, and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS			25 $^{\circ}C$			-40 $^{\circ}C$ TO +85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		V_I (V)	I_O (mA)	V_{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	-	-	-	1.9	-	1.9	-	1.9	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	V_{OH}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	3.7	V
			-4	4.5	3.98	-	-	3.84	-	5.2	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	V_{OL}	V_{IH} or V_{IL}	-	-	-	-	-	-	0.33	-	0.4	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	± 0.1	-	± 1	-	± 1	μA

CD54HC04, CD74HC04, CD54HCT04, CD74HCT04

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO +85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	6	-	-	2	-	20	-	40	μA
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} and GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	5.5	-	-	2	-	20	-	40	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 2)	V _{CC} - 2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

2. For dual-supply systems, theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
nB	1.2

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g. 360μA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES											
Propagation Delay, Input to Output (Figure 1)	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	85	-	105	-	130	ns
			4.5	-	-	17	-	21	-	26	ns
			6	-	-	14	-	18	-	22	ns
Propagation Delay, Data Input to Output Y	t _{PLH} , t _{PHL}	C _L = 15pF	5	-	6	-	-	-	-	ns	

Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Transition Times (Figure 1)	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	2	-	-	75	-	95	18	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_i	-	-	-	10	-	10	-	10	pF	
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	-	5	-	21	-	-	-	-	pF	
HCT TYPES											
Propagation Delay, Input to Output (Figure 2)	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	19	-	24	-	29	ns
Propagation Delay, Data Input to Output Y	t_{PLH}, t_{PHL}	$C_L = 15\text{pF}$	5	-	7	-	-	-	-	-	ns
Transition Times (Figure 2)	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C_i	-	-	-	10	-	10	-	10	pF	
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	-	5	-	24	-	-	-	-	pF	

NOTES:

- C_{PD} is used to determine the dynamic power consumption, per gate.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

Test Circuits and Waveforms

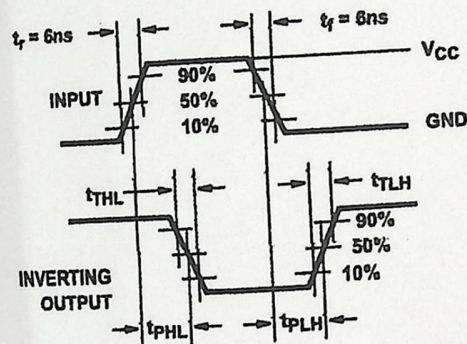


FIGURE 1. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

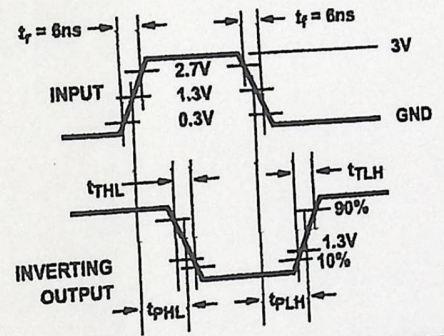


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

4.2.2 ADC0808 Analog to Digital Converter

- Why using ADC?

When the touch screen receives a touch, one or more of the receivers will change the value of the voltage they pass in response to that touch, but in the receivers we used, the change is not large enough to make the analog voltage while touching seems as a zero as a digital input, as example the voltage while touching or not will always be over 3V and this value digitally will be considered as one in all cases.

To solve this problem and determine if there is a touch or not even if the voltage always indicate logic one digitally, in our project we decided on handling this voltage amount by the software which is able to detect the change in the voltage even if it was very small, to pass this analog voltage to the software we need an IC that can convert the analog input into a digital one that can be pass to the PC through the parallel port.

This IC is called the analog to digital converter, an example is ADC0808, and it can convert the analog voltage value into a digital output.

Because of the large number of receivers we have, we need to switch between them one after another, reading one voltage value each time, the ADC0808 can receive 8 inputs, it contains an analog multiplexer that receives as input a 3 selection line to enable one of the analog inputs to the ADC, by this way each ADC can read 8 different analog voltages from 8 different receivers.

- Pins Layout and Description

Following is the pins layout and description of the ADC0808 analog to digital multiplexer.

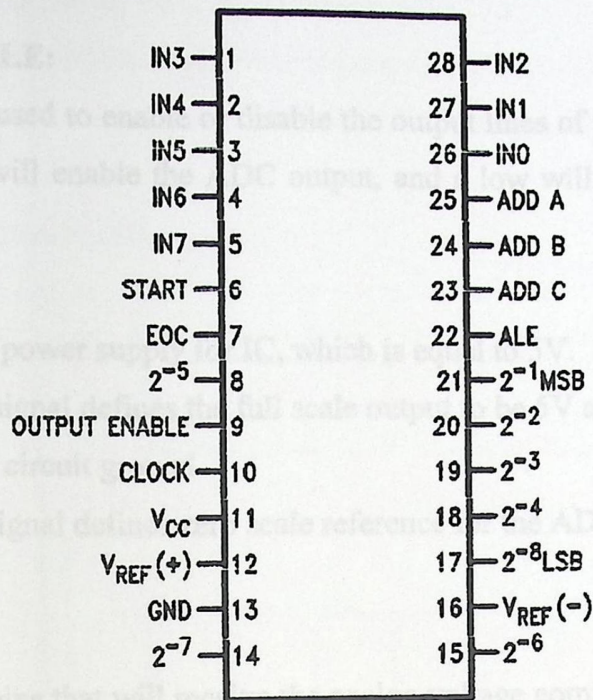


Figure 4.7: ADC0808 Pins Layout

- START:

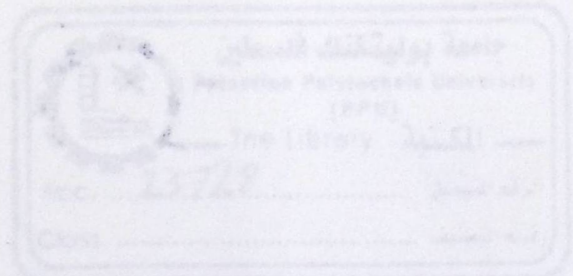
An input signal to enable the start of conversion process, ADC0808 IC will start the conversion on the high to low transition of the start signal.

- (Address Latch Enable) ALE:

This signal is used to enable the buffering of the address lines used as input to the internal analog multiplexer, such that the ALE will be high at the start of conversion to latch the address of the selected line from the multiplexer, and this address will be buffered at the pins of the ADC even if it is not provided by the selection lines.

- CLOCK:

The conversion process requires a clock with a specific frequency to work properly, this clock signal is provided by a timer on the clock pin of the ADC0808, and the frequency used is equal to 640KH.



- OUTPUT ENABLE:

This pin is used to enable or disable the output lines of the ADC, such that a high signal on the OE will enable the ADC output, and a low will make all the output lines goes low.

- VCC: This is the power supply for IC, which is equal to 5V.

- VREF (+): This signal defines the full scale output to be 5V as a digital output.

- GND: This is the circuit ground.

- VREF (-): This signal defines zero scale reference for the ADC.

- IN0 to IN7:

Those are the pins that will receive the analog voltage coming from the receivers; this voltage will be converted to a digital output.

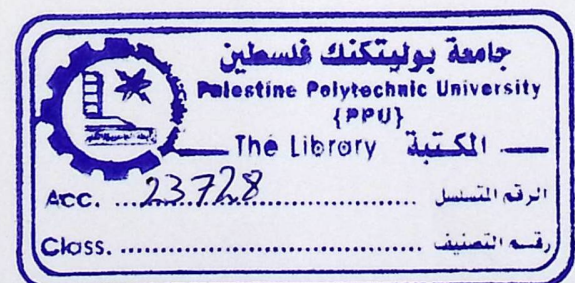
- (2^{-1}) to (2^{-8}) :

Those are the ADC's output lines that specify the digital value of the converted analog voltage at the input lines, the value on these lines is sent to the PC to be analyzed, (2^{-1}) is the least significant bit and (2^{-8}) is the most significant bit.

4.2.3 DM74LS138 Decoder

- Why using 74138 Decoder?

Because of the large number of receivers in the frame we needed multiple ADC's to cover them all, there are five ADC's in the interfacing circuit, each one is responsible for reading eight receivers, now we needed a way to switch between the five ADC's enabling one of them each time.



This switching can be done by using the 74LS138 decoder, it takes requires three selection lines as input and has eight possible combinations to choose from, we need only five of its output lines that are connected to the ADC's output enable signal.

- Pins Layout and Description

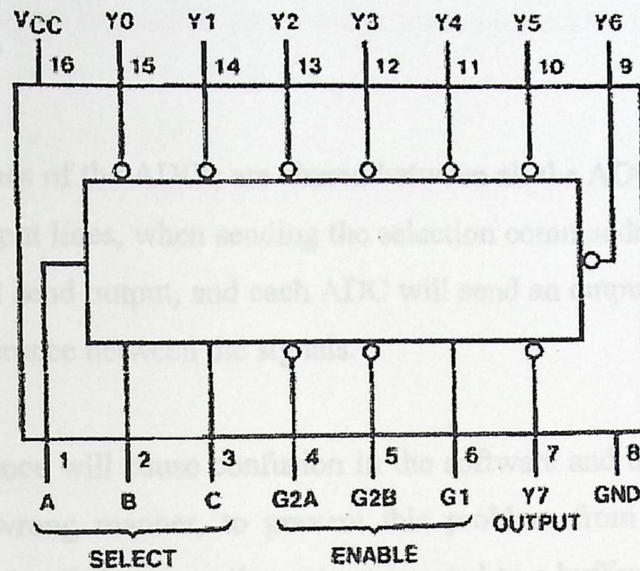


Figure 4.8: 74LS138 Pins Layout

- A - B - C:

Those pins select a specific output line to be activated, the output line are connected to the buffer's output enable pins.

- G2A, G2B, G1:

These are the enable lines of the decoder, to make the decoder always enabled the first two pins (G2A, G2B) are permanently connected to active low, and the third one is connected permanently to Active high signal.

- GND: this is the ground for IC.

- VCC: This pin is the voltage supply to the decoder that is connected to +5v.

- Y0 - Y7:

Thos pins are the decoder's output lines, each one of them can be activated by a specific input at the selection lines, they are inverted, that means they must enter an inverter to perform the functionality we need.

4.2.4 3-STATE Octal Bus Transceiver

- Why using Buffer?

The output lines of the ADC's are shared between all the ADCs and are connected to the parallel port input lines, when sending the selection commands from the PC, all the IC's are activated and send output, and each ADC will send an output on the output lines, this will cause interference between the signals.

This interference will cause confusion in the software and the voltage value will be calculated in a wrong manner, to prevent this problem from happening we used buffers, such that each ADC's output lines are connected to a buffer, that will receive the output enable signal from the decoder, when the buffer is disabled, it wont pass the input form the ADC, and this prevents the interference.

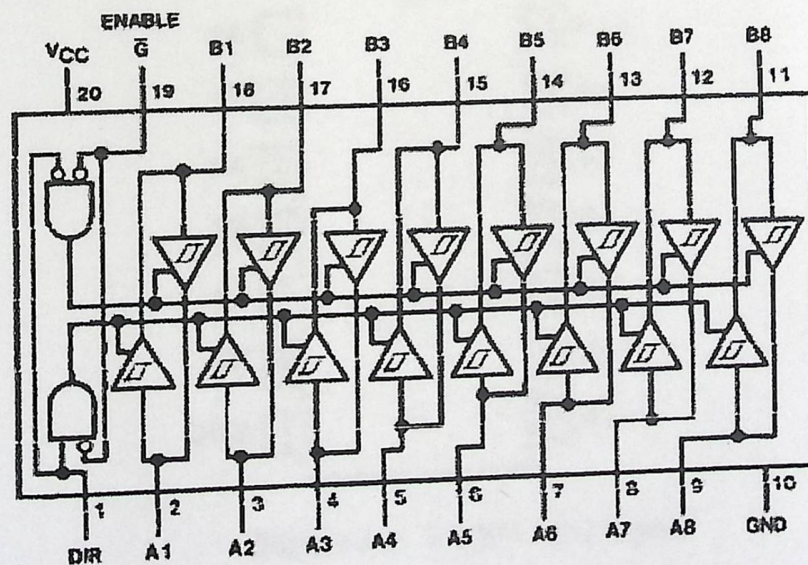


Figure 4.9: 3-STATE Octal Bus Transceiver

- Pins Layout and Description

- 1- DIR: this pin is used to specify the direction of passing the signal from A to B or the opposite.
- 2- A1 – A8: those pins can be used to pass the signal to B or receive the signal from A.
- 3- B1 – B8: those pins can be used to pass the signal to A or receive the signal from B.
- 4-GND: this is the ground signal to the IC.
- 5- VCC: the power supply to the IC.
- 6- G: this is an active low pin that enables or disables the output of the buffer according to the input it receives.

4.2.5 CD74HCT04 Logic Hex Inverter

- Why using 7404 Inverter?

The inverters are used because the parallel port pins that can be used for input are all activated by a grounded signal, but the signal coming from the ADC's are active high, so it first enters an inverter to be inverted before being passed to the PC.

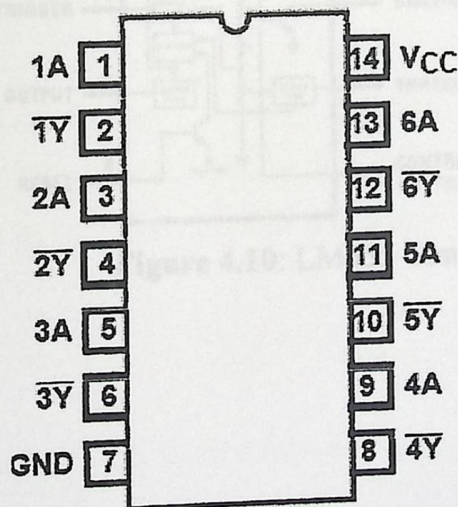


Figure 4.9: 74LS04 Pins Layout

- Pins Layout and Description

Each input signal to the inverter is inverted as a result of the inverting, these input signal are on the pins (1A,2A,3A,4A,5A,6A),and the output signal pins are (1Y,2Y,3Y,4Y,5Y,6Y).

4.2.5 LM555 Timer:

- Why using LM555 Timer?

The ADC's needs a clock input to perform the conversion process appropriately, this clock signal is provided by the output pin of the LM555 timer with a 680 KHz frequency.

- Pins and Timer Circuit

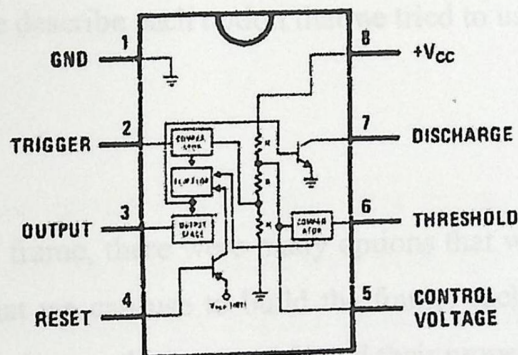


Figure 4.10: LM555 Timer

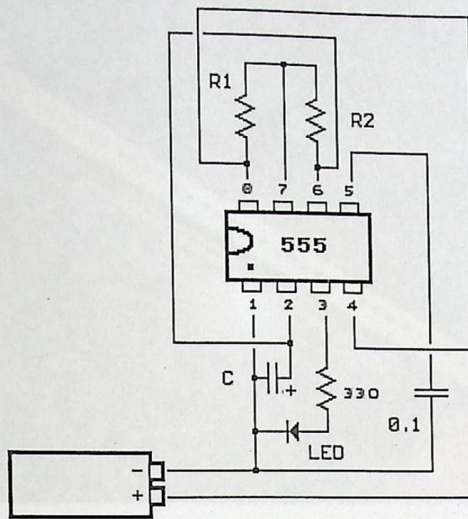


Figure 4.11: LM555 Timer Circuit

4.4 Hardware Options

In this section we describe each option that we tried to use to accomplish the project's objectives.

- Frame

In designing the frame, there were many options that we can choose from, there were many materials that we can use to build the frame, each one has advantages and disadvantages, the following are those materials and their properties.

1- Wood

This was the first of our options and the first method we thought about to build the frame.

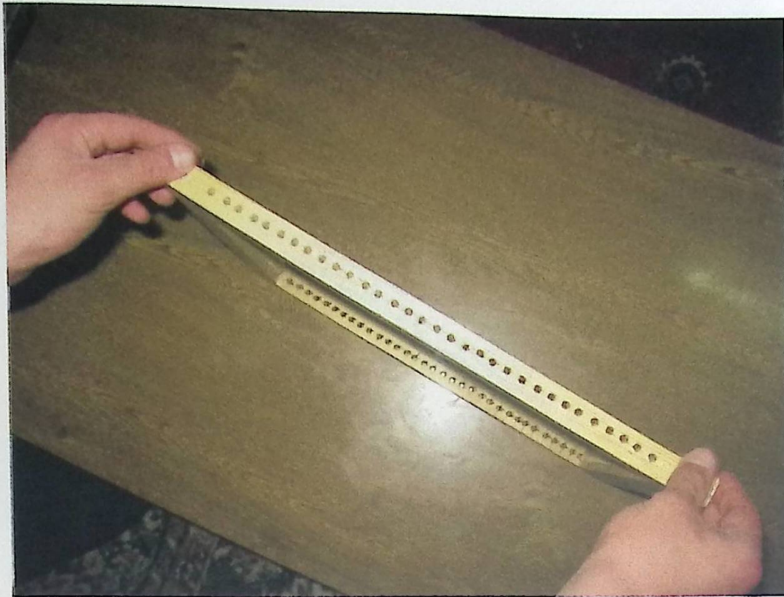


Figure 4.12: Wood Frame

- Advantages:

The wood has a light weight and can be easily formed to create the shape we need, also it is inexpensive and available.

- Disadvantages

Most of wood types contains fiber, the fiber causes an inaccuracy while perforating the wood, such that the LEDs canals were in accurate, some are large, some are not, so this was an indicator that the wood is not the best option.

- Aluminum

This was the alternative to the wood, and we used it in our project.

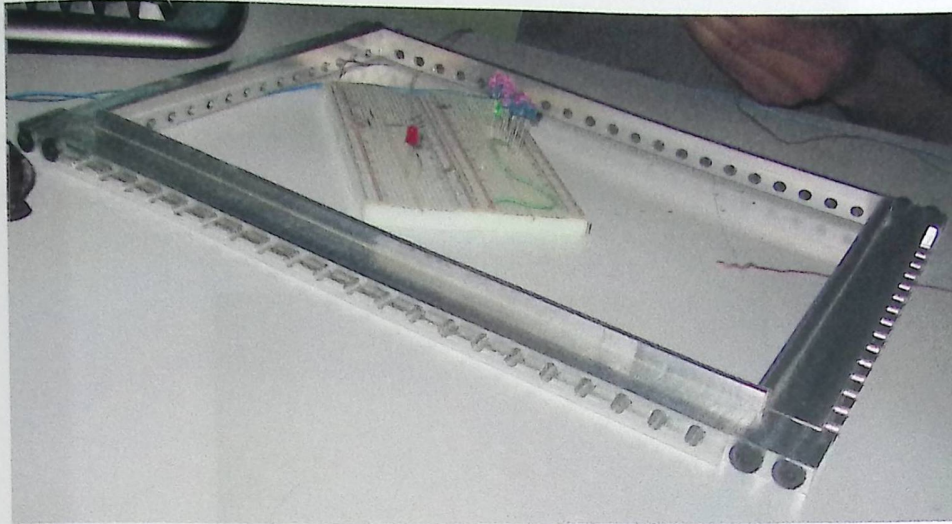


Figure 4.13: Aluminum Frame

- Advantages:

The aluminum is light in weight compared to steel or metal, it can be formed easily using an accurate machine to create the holes in forming the aluminum as we needed, it can be formed with high accuracy and this was a good point for this option.

- Disadvantages

The aluminum is expensive, and difficult to be found, it is reflective so there is the possibility of reflecting the infrared beam, which increases the interference.

- Infrared Senders

When connecting the infrared senders, we created many circuits until we found a circuit that can really work, in the first circuit the senders were connected in parallel with a traditional resistor on each sender, this option caused a high temperature in the resistor that caused them to be damaged, on the other hand the senders weren't sending with the same power.

On the other hand this option has the advantage of protecting the whole senders from being disabled when one sender is damaged, because they are connected in parallel,

the second option was to connect the senders in series, this option was better because the current the same on all senders so they all send with an equal power, to solve the temperature issue, we used a high power resistor, this resistor can handle the increase of temperature and the high heat.

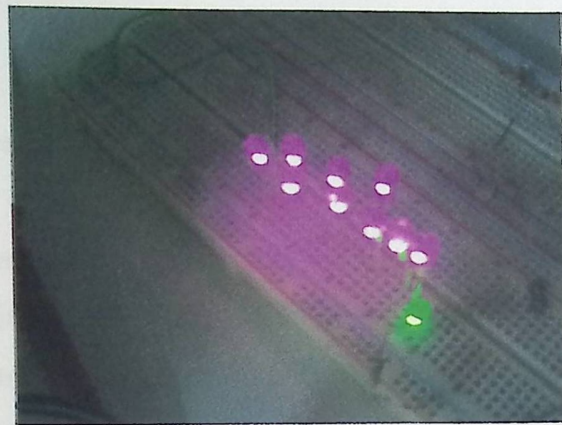


Figure 4.14: Infrared Senders Series Connection

- Infrared Receivers

In building the receivers circuit we created many circuits in attempt to find the best option that we can have.

- Receivers with transistor

In this option we used a transistor to function as a switch between a 1 and 0, but in this case the sensitivity of the receiver was weakened because the transistor was consuming a high current which affects the receiver.

- Receivers with an AC supply

The AC supply option didn't caused improvement on the receiver sensitivity, and also it caused the receiver to be off, because of the frequency and this is a problem to our project because the receivers must be enabled all the time.

- Receivers with power supply and resistors only

This is the option that worked in a proper manner in our project, and the receiver sensitivity was good enough to detect the change in the infrared beam in front of the receiver, the receivers are connected in parallel, each one with a 1k resistor.

- Senders and Receivers Alignment

In the case where the sender were all together on a side and the receivers were on the other side, this option caused a high interference between the receivers because each receiver was facing multiple senders, the alternative to this option was to put each receiver between two senders, in this way it will be facing only one sender in the opposite direction, this reduced the interference enough.

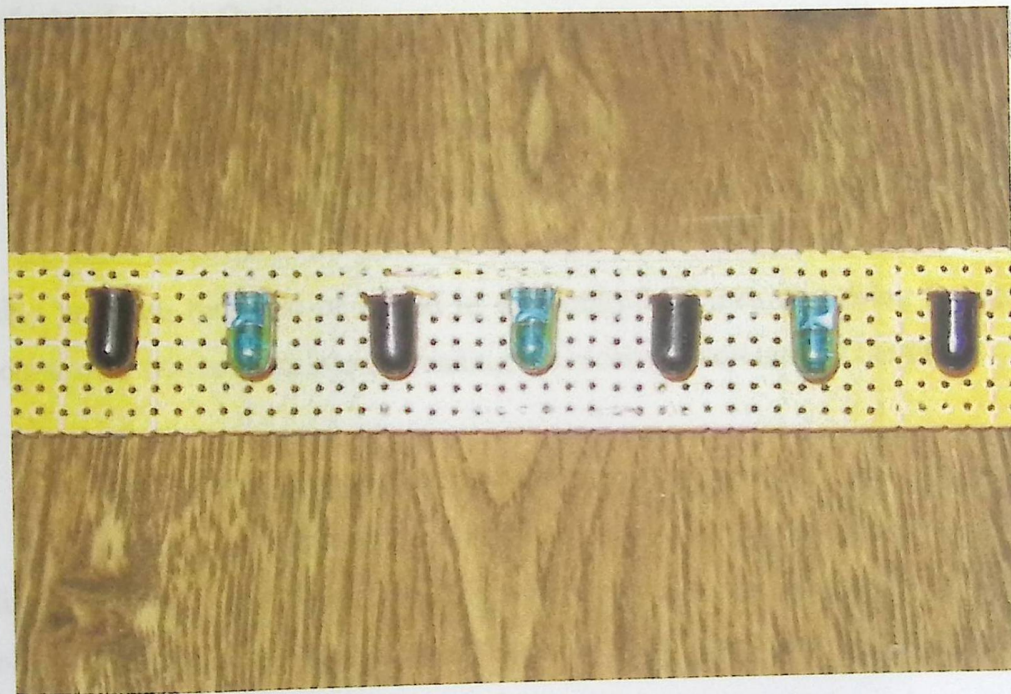


Figure 4.15: Senders and Receivers Alignment

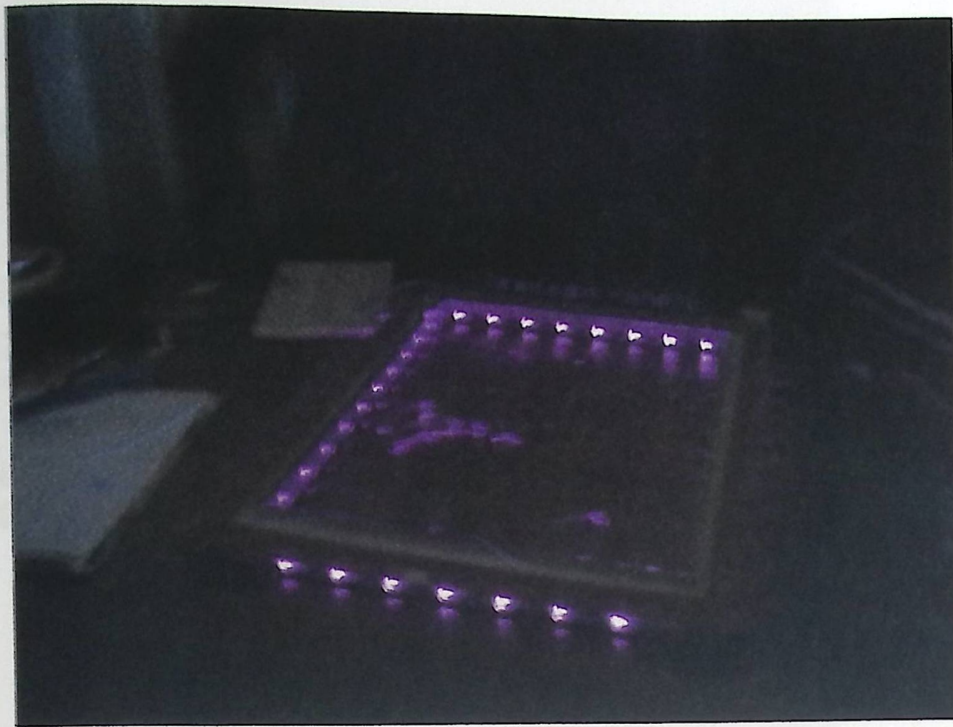


Figure 4.16: Infrared Beams

- Interfacing Circuit Options

In designing the interfacing we had two main options to work on, the first was to use a microcontroller unit that is mounted on a board with memory, input and output ports, the microcontroller we used called Intel 8051 microcontroller, we wrote an assembly program that will be stored in the controller's memory, using the option, the microcontroller was responsible for reading the receivers voltages all the time.

The microcontroller will read each voltage value, analyze it and if it detects a touch by the change in the receiver's voltage, it will interrupt the PC, send it the coordinates using the serial port, and the microcontroller will perform this functionality controlled by an assembly program that is stored in the controller's memory, it will run automatically when the controller is turned on.

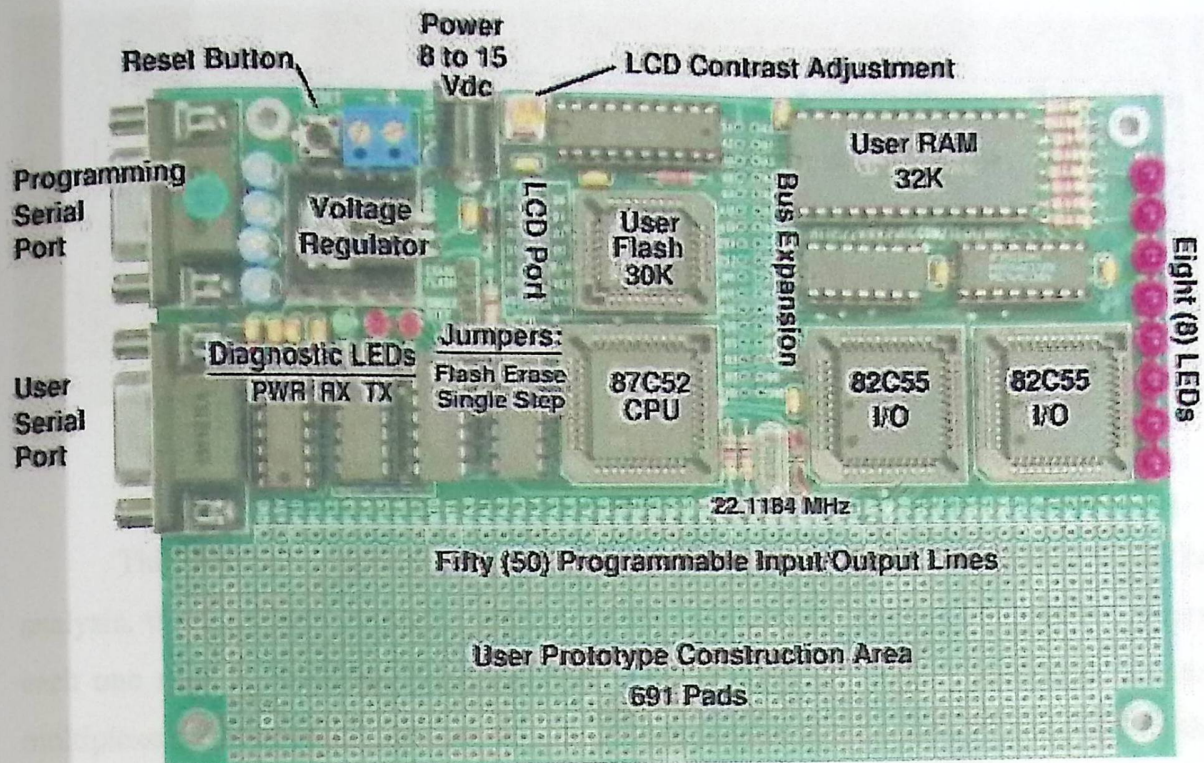


Figure 4.17: 8051 Development Board

This option didn't work, because of two main reasons; the first was the analog output of the receivers, the microcontroller can accept only digital input, on its input ports, on the other hand, another problem came out into the project, the microcontroller we used was taken from the collage, and we later discovered that there was a port damaged in the microcontroller, this caused a problem to us because we needed a large number of data inputs from the infrared frame to the microcontroller.

In trying to solve the problem, we thought about an alternative, which is to use a group of analog to digital converters, that reads the analog voltage on the receivers, convert it to a digital value, this value will be read by the PC on the parallel port, this option depends on the PC software driver to monitor the analog to digital converters, send control signals to them and read each receiver's voltage, storing each value to be analyzed.

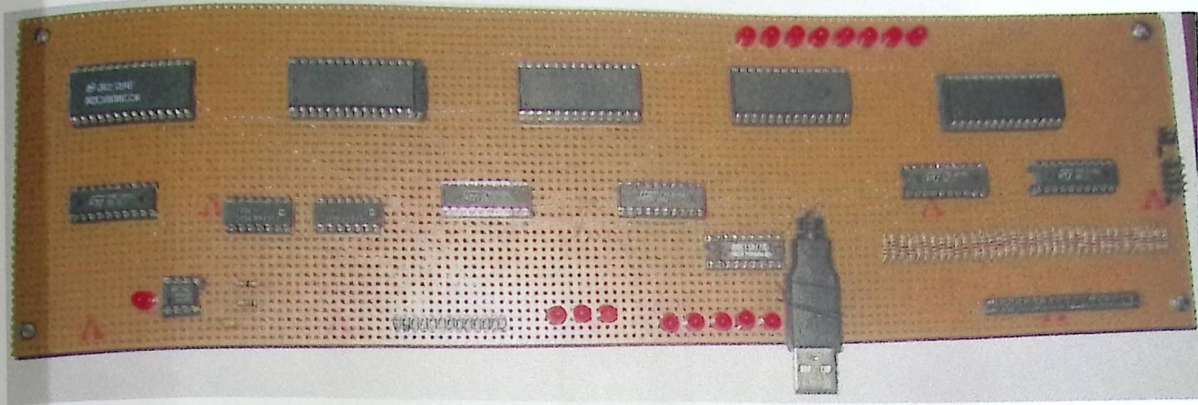


Figure 4.18: Interfacing Circuit

This the software will be responsible for the controlling, reading the data and the analysis, the interfacing circuit consists mainly of five the analog to digital converters, each one reading eight different receivers, switching between them using an internal multiplexer, and to switch between the ADC's we used a decoder that is controlled by the PC.

4.5 Software GUI Scenes

This section view the graphical user interface that the user is expected to interact with, the method used in the GUI design, the interfaces and the options that the user can control.

The software driver consists of many interfaces that contain different components and controls to control the software and change its options; in the following we specify each interface and its usage.

- Main Menu

This is the main menu of the software, it contains multiple buttons that the user can press, and these buttons were designed to fit the finger touch, each one of these buttons opens a menu to the left that contains controls and components to control the software behavior.



Figure 4.19: Main Panel

- Cursor Options

This interface contains controls to allow the user to set the cursor options.



Figure 4.20: Cursor Options Panel

- Click Options

This panel allows the user to set the click, right click and double click options.

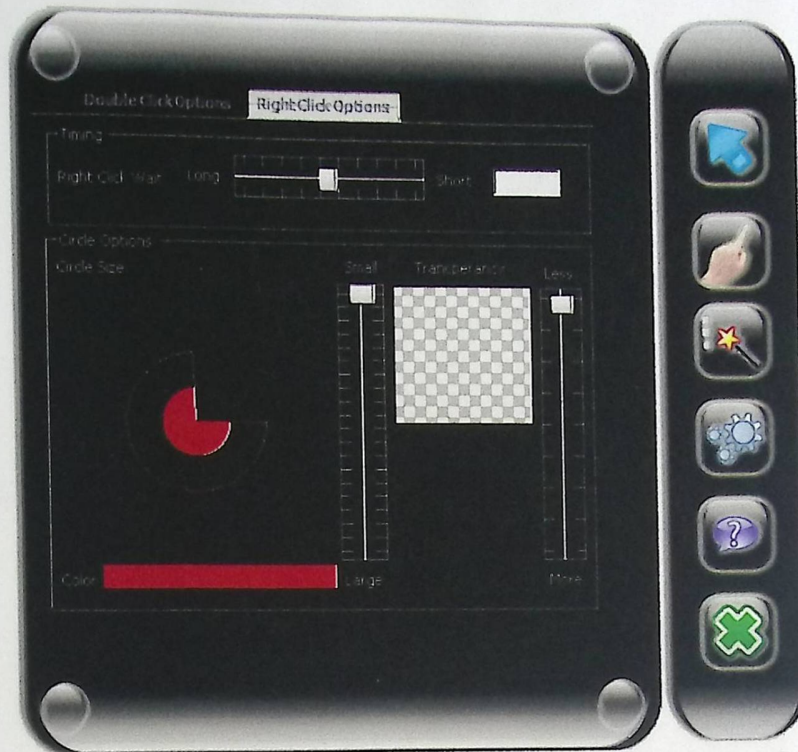


Figure 4.21: Click Options Panel

- Visibility Options

This panel allows the user to specify if a feature is visible or hidden.



Figure 4.22: Visibility Options Panel

- Settings

This panel allows the user to change the software settings.



Figure 4.23: Settings Panel

- Help

This button provides the user with a simple help to instruct the user of how to use the touch screen driver and how to customize his options.

- Leave

This button will show a message that asks gives the user the options to close the program, hide it or cancel the operation.

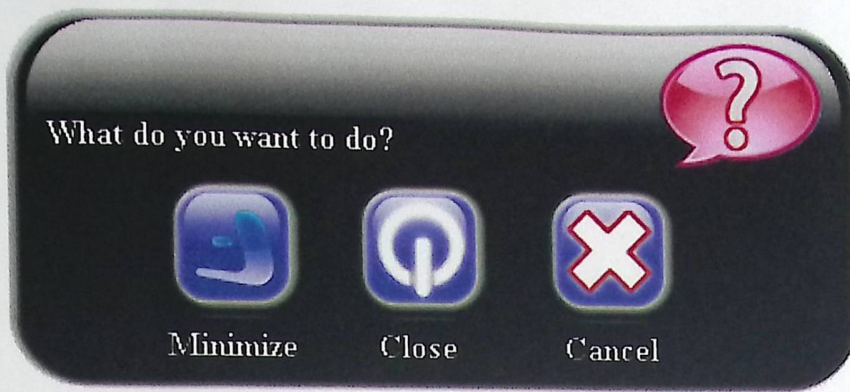


Figure 4.24: Leave Message

If the user decided to close, the software closes, if he decided to hide, the software main panel will be hidden and a button will be shown at the bottom of the screen to allow the user to restore the program again.



Figure 4.25: Software Restore Button

4.6 Summary

This chapter consists of three sections; the first one view the structural design of the whole project, and the main interfacing circuit details, the second section views the main hardware options in the project, the third section lists all the hardware components in detail with their specifications, the third section view the design of GUI scenes done in the software driver.

5.1 Overview

This chapter focuses on the implementation phase of the project, for hardware listing each component used, its interconnections, and also for software showing group flow charts that describe the software behavior and a pseudo code to show the implementation of the algorithms.

Chapter Five

Implementation

5.2 Hardware Implementation

5.1 Overview

5.2 Hardware Implementation

5.3 Software Implementation

5.4 Summary

The main hardware components in the system are:

Infrared Net Frame

The infrared net frame consists of the following components:

- Aluminum Frame
- Circuit Board
- Infrared LED Source
- Infrared Photo Diode
- Resistors
- High Power Resistor

The source, receiver and control are connected to a central board that is mounted on the aluminum frame, and which will receive digital data from the aluminum frame to reduce the interference between receivers on the other side which is placed between two receivers to act as an optical barrier to reduce any one receiver. This reduces the interference and prevents any receiver.

5.1 Overview

This chapter focuses on the implementation phase of the project, for hardware listing each component used, its implementation and specifications, and also for software showing group flow charts that describes the software behavior and a pseudo code to show the implementation of the flow charts.

5.2 Hardware Implementation

The infrared net based touch screen project consists of many hardware components that are connected to each other, here we will list each component specifying its circuit, how it is being designed and how it is connected to the rest of the system's hardware.

The main hardware components in the project are:

- Infrared Net Frame

The infrared net frame consists of the following components:

- Aluminum Frame
- Circuit Board
- Infrared LED Sender:
- Infrared Photo Diode
- Resistors
- High Power Resistors

The sender, receivers and resistors are mounted on a circuit board that is mounted on the aluminum frame, each sender and receiver is placed inside a canal in the aluminum to reduce the interference between receivers, on the other hand each sender is placed between two receivers so that in the opposite direction it faces only one sender, this reduces the interference and prevent the wrong detection.