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Title

Power Quality Improvement using Unified Power Quality Conditioner

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الإهداء

إلى من جرعن الكأس فارغاً ليسقيننا قطرة حب إلى من كلّت أناملهن ليقدمن لنا لحظة سعادة إلى من حصدن الأشواك عن دربنا ليمهدن لنا طريق العلم إلى من ارضعننا الحب والحنان إلى رموز الحب وبلسم الشفاء أمهاتنا إلى من حصدوا الشوك عن دربنا بايديهم العارية ومهدوا طريقنا للنجاح الذين خاضوا المعارك مع الحياة ليوفروا لنا السلام أبائنا الى الحبال التي تسندنا في هذه الحياة اخوتنا إلى العطوفات والى الزهور الفتية الى الام الثانية أخواتنا الى من كسبنا بمعرفتهم رجالا إلى رفاق الدرب والعلم إلى الاخوة التي لم تنجبهم امهاتنا زملائنا إلى من ضحوا بحريتهم من اجل حرية غيرهم الاسرى والمعتقلين الى من ضحوا بحياتهم دفاعا عن شرفنا ووطننا شهداء فلسطين إلى منارات العلم التي أضاءت ضريقنا للعمل وطريقنا للنجاح أساتذتنا إلى هذا الصرح العلمي الفتي والحبارجامعة بوليتكنك فلسطين إلى الشعب الذي عانى وصمد سقط ووقف الشعب الصامد شعب فلسطين إلي ارض الشهداء الارض التي كانت لنا فخر فلسطين الحبيبة بضع كلمات كتبناها لكم مهدينكم إيها يا من لكم في القلب مكانة وحنينا : بدأنا المسير بخطوةٍ مررنا بالسنين سريعاً ****** وددنا ان نطلب العلى وقفنا امام الصعاب سنينأ

****** لياتي اليوم الذي اصبحنا فيه من المهدينَ ****** ثمار جهدٍ نتاج عملٍ لاهلٍ و أحبابٍ داعمينَ ****** سنرفع رؤوس من بهم صعدنا قمم الحبال حاملين جهوداً ****** ليأتي الطريق لنهايةٍ بكم عبرناها طيل السنينَ ****** فشكراً للذي كان داعمى وكان لى نورا وحنيناً ****** امي بحبك اودعتني سهرتُ الليالي بعينك الياقوتةَ ****** ابي بعطفك الكثير جعلتني محاربا الصعاب لتكون فخورأ ****** استاذي كنت لي والداً اردت للفخر في عينيك سطوعاً ***** وأخي جبلٌ ملت عليه لاستند قدوتي صبوت لها وصولاً ****** اختى العطوفة فوائح عطفها تلك السنين أهديها بطولها ****** وقبل الناس نشكر الذي رفع السماء وأوجد الساعين ******* ربى لك الحمد بكثرةٍ أنت لناس خير الداعمينَ ****** فسلام لكم يا أحبتى أهديكم وروداً من عبق السنينَ

شکر وتقدیر

رقل اعملوا فسيرى الله عملكم ورسوله والمؤمنون) صدق الله العظيم إلهي لا يطيب الليل إلى بشكرك ولا يطيب النهار إلا بطاعتك. ولا تطيب اللحظات إلا بذكرك. ولا تطيب الأخرة إلا بعفوك. ولا تطيب الجنة الى برؤيتهِ جل جلاله..... لابد لنا ونحن نخطو خطواتنا الأخيرة في الحياة الجامعية من وقفة نعود إلى أعوام قضيناها في رحاب الجامعة مع اساتذتنا الكرام الذين قدموا لنا الكثير باذلين بذلك جهودا كبيرة في بناء جيل الغد لتبعث الامة من جديد... وقبل أن نمضي نقدم أسمى آيات الشكر والامتنان والتقدير والمحبة إلى الذين حملوا أقدس رسالة في إلى الذين مهدوا لنا طريق العلم والمعرفة إلى الذين مهدوا لنا طريق العلم والمعرفة ونحص بالتقدير والشكر إلى من قدم لنا يد العون وكان لنا سنداً والذي علمنا التفاول والضي إلى ونخص بالتقدير والشكر إلى من قدم لنا يد العون وكان لنا سنداً والذي علمنا التفاول والضي إلى الأمام، إلى من رعانا وحافظ علينا، إلى من وقف إلى جانبنا عندما ضللنا الطريق الأمام، إلى من رعانا وحافظ علينا، إلى من وقف إلى جانبنا عندما ضللنا الطريق

.....الدكتور فؤاد الزرو

Abstract

Power quality can be defined as any power problem faced in the frequency, current or voltage deviation which leads to mal operation of the customer's equipment. Mainly the use of power electronics devices that acts as the nonlinear load is responsible for the degradation in the poor power quality. Poor power quality results in various problems in the distribution systems like higher power losses, harmonics, sag and swells in the voltage, poor distortion. The recent developments in communications, digital electronics, and control system have rapidly increased the number of sensitive loads that require ideal sinusoidal supply voltage for their proper operation. So, it became necessary to include some sort of compensation in order to meet limits proposed by standards. Here Unified power quality Conditioner (UPQC) has been used to overcome the power quality problem. UPQC which is a combination of back to back connected series and shunt APFs through a common DC link voltage, the two APFs function differently. The shunt active filter is mainly advantageous in removing the current related problems and the improvement of power factor and regulation of DC link voltage. Whereas the series APF helps in correction of voltage related problems by acting as a controlled voltage source. The voltage that is injected in series with the load by series Active Power filter is made to follow a control law which results in a sinusoidal load voltage that is the sum of the voltage injected by the series inverter and the input voltage. Whereas the shunt APF acts as a current source that injects a compensating harmonic current in order to have sinusoidal, in-phase input current. Several control strategies have been reported in literature that determines the reference values of the voltage and the current. One of them the synchronous reference frame, d-q technique. this method synchronous reference frame method is used for the control of Series APF and is used for the control of shunt APF. UPQC has the capability of compensating the harmonic current, reactive power, voltage imbalance and voltage sag and swell. It also helps in reducing the energy losses that happens in the power systems.

الملخص

يمكن تعريف جودة الطاقة بأنها أي مشكلة طاقة تواجه في التردد أو التيار أو انحراف الحبهد مما يؤدي إلى سوء تشغيل معدات العميل. بشكل رئيسي ، استخدام أجهزة إلكترونيات الطاقة التي تعمل كحمولة غير خطية هي المسؤولة عن تدهور جودة الطاقة الرديئة. يؤدي ضعف جودة الطاقة إلى مشكلات مختلفة في أنظمة التوزيع مثل فقدان الطاقة الأعلى ، التوافقيات ، الانخفاض والارتفاع في الجهد ، تشوه في الاشارة . أدت التطورات الأخيرة في الاتصالات والإلكترونيات الرقمية ونظام التحكم إلى زيادة سريعة في عدد الأحمال الحساسة التي تتطلب جهد إمداد جيبي مثالي لتشغيلها بشكل صحيح. لذلك أصبح من الضروري إدراج نوع من التعويض من أجل تلبية الحدود التي اقترحتها المعايير. هنا تم استخدام الموحد لمشاكل جودة الطاقة (UPQC) للتغلب على مشكلة جودة الطاقة. UPQC التي هُو مزيج من انفيرترين على التوالي والتوازي APFs من خلال مكثف DC مشترك ، يعمل الانفيرترين APFs بشكل مختلف. الانفيرتر على التوازي مفيد بشكل رئيسي في إزالة المشاكل ذات الصلة الحالية وتحسين عامل الطاقة وتنظيم جهد المكثف . في حين أن الانفيرتر على التوالي APF تساعد في تصحيح المشاكل المتعلقة بالجهد من خلال العمل كمصدر جهد متحكم فيه. يتم توليد الحجهد الذي يتم حقنه بتوالي مع الحمل حسب الانفيرتر على التوالي ليتبع قانون التحكم الذي ينتج عنه جهد تحميل جيبي هو مجموع الحبهد الذي تم حقنه بواسطة الانفيرتر على التوالي و جهد المصدر . في حين يعمل الأنفيرتر على التوازي APF كمصدرجهد يضخ تيارًا توافقيًا تعويضيًا من أجل الحصول على تيار إدخال جيبي مثالي . تم ذكر العديد من استراتيجيات التحكم في فصل المراجعات تاريخية حول هذا الموضوع التي تحدد القيم المرجعية للجهد والتيار. واحد منهم هو الإطار المرجعي المتزامن ، تقنية d-q . تستخدم هذه الطريفة طريقة الإطار المرجعي المتزامن للتحكم في الانفيرتر الذي على التوالي APF وتستخدم للتحكم في انفيرتر الذي على التوازي UPQC.AP لديه القدرة على تعويض التيار التوافقي ، الطاقة التفاعلية ، عدم توازن الجهد و الانخفاض والارتفاع الموقت في الجهد. كما أنه يساعد في تقليل خسائر الطاقة التي تحدث في عنصر أنظمة الطاقة ويزيد أيضًا من سلامة التشغيل.

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List of Abbreviations

AC	Alternative Current
AF	attenuation factor
APF	active power filters
ASD	Adjustable speed drive
CSC	current source converter
CSI	Current Source Inverter
ECA	exponential composition algorithm
EMI	electromagnetic interference
FACTS	Flexible AC Transmission System
НЕРСО	Hebron Electric Power Company
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
IPFC	Interline Power Flow Controller
JDECO	Jerusalem District Electricity Company
РС	Personnel Computer
PCC	point common coupling

PI	Proportional Integral
PID	Proportional Integral Derivative
PLC	programmable logic controller
PQ	power quality
PWM	Pulse Width Modulation
SERC	Series converter
SHUC	Shunt Convertor
SRF	Synchronous Reference Frame
STATCOM	Static Synchronous Compensator
TCBR	Thyristor Controlled Braking Resistor
TCR	Thyristor Controlled Reactor
TCPAR	Thyristor Controlled Phase Angle Regulator
TCPST	Thyristor controlled phase shifting transformer
THD	total harmonic distortion
TSR	Thyristor Switched Reactors
TSC	Thyristor Switched Capacitor
UPFC	unified power flow controller
UPQC	unified power quality conditioner
VSI	voltage source inverters

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List of Symbols

Lf, Cf	Inductance and capacitance of lc filter
Lsh, Rsh	Inductance and resistance of Lsh inductor
RL,CL	Resistance and capacitance of nonlinear load
h	Harmonic order
d, q	Direct and quadrature components in synchronous reference frame
lpha , eta	Direct and quadrature components in stationary reference frame
1, <i>h</i>	Fundamental and harmonic components
i_1 , i_h	Fundamental and harmonic current
is, i_L	Source and load current
<i>Vdc_{ref}</i>	Reference DC capacitor voltage

Chapter 1

Introduction

1.1 Introduction

FACTS DEVICES :

In conventional AC transmission, the power transfer capability has been limited by various dynamic and static limits such as transient stability, voltage stability, thermal limits, etc. These inherent power system limits led to the underutilization of existing transmission sources[1].

Traditional methods of solving these problems use fixed and mechanically switched series and shunt capacitors, reactors and synchronous generators. However, the desired response has not been effective due to slow response, wear and tear of mechanical components[1].

With the invention of thyristor devices, power electronic converters are developed that led to implement FACTS controllers. These power electronic-based controllers can provide smooth, continuous, rapid and repeatable operations for power system control[2].

FACTS is an acronym for Flexible AC Transmission System and it is an application of power electronic devices to the electrical transmission system[2]. It is an AC transmission system that incorporates a power electronic controller and other static controllers to improve the controllability as well as power transfer capability. It improves the performance of electrical networks by managing active and reactive power[2].

The IEEE definition for the FACTS controller is stated as, it is a power electronic-based system and other static equipment that provides the control of one or more AC transmission parameters (such as voltage, impedance, phase angle ,and power)[1].

The possibilities offered by the FACTS technology include:[1]

• Power can be controlled for a desired amount such that it flows through prescribed transmission routes.

- Loading of the transmission lines near their thermal, steady-state and dynamic limits.
- Enhancing the power transfer capability between interconnected transmission lines.
- Increasing the quality of supply for sensitive industries.

• Enhancing transmission system reliability and availability by limiting the impact of multiple faults.

Why Compensation Techniques are used in the Power system ?

Power System network consists of three kinds of powers, namely, active, reactive and apparent power. Active power is the useful or true power that performs useful work in the system or load.

Reactive power is caused entirely by energy storage components and the losses due to reactive power may be considerable, although reactive power is not consumed by the loads. The presence of reactive power reduces the capability of delivering active power by the transmission lines. And the apparent power is the combination of active and reactive power. In order to achieve maximum active power transmission, the reactive power must be compensated. This compensation is necessary for:[3]

- Improving the voltage regulation
- Increasing system stability
- Reducing the losses associated with the system
- Improving the power factor
- Better utilization of machines connected to the system

The compensation techniques of the power system supply the inductive or capacitive reactive power to its particular limits in order to improve the quality and efficiency of the power transmission system. Two popular compensation techniques used in power system that are series as well as shunt compensation for the transmission lines using these FACTS devices[3].

In series compensation, line impedance is modified, which means net impedance is decreased and thereby increasing the transmittable active power. For shunt compensation, reactive current is injected into the line so as to regulate the voltage at the point of connection and reduced losses.[3]

Types of FACTS Controllers

FACTS controllers are classified as :

- Shunt connected controllers
- Series connected controllers
- Combined series-series controllers
- Combined shunt-series controllers

Series connected controllers :

These controllers inject a voltage in series with the line. If this voltage is in phase quadrature with the current, the controller consumes or supplies variable reactive power to the network. These controllers could be variable impedance such as a reactor or capacitor or a power electronic-based variable source. Examples of the series controllers include SSSC, TCSR, IPFC, TSSC, TCSC, and TCSR[1].



Figure 1.1: series connected controllers[1]

Shunt connected controllers :

These controllers inject a current into the system at the point of connection. If this current is in phase quadrature with the line voltage, a shunt controller consumes or supplies variable reactive power to the network.

Similar to series-connected controllers, these controllers could be a variable reactor or capacitor or a power electronic-based variable source. Examples of the shunt controllers include TCR, STAT-COM, TSR, TCBR, and TSC[1].



Figure 1.2: Shunt connected controllers[1]

Combined series-series controllers :

These controllers are the combination of individual series controllers that are controlled in a coordinated manner in multiple power transmission systems. Or these could be unified controllers in which separate series controllers are employed in each line for series reactive power compensation and also to transfer the real power among the lines via proper link.

An example of this controller is IPFC that balances the real and reactive power flow in the lines in order to maximize the power transmission[1].



Figure 1.3: combind series-series connected controllers[1]

Combined series-shunt controllers :

These are the combination of separate series and shunt controllers that are controlled in a coordinated manner or a unified power flow controller (UPFC) with series and shunt elements. These combined controllers inject current into the system with a series part of the controller and voltage in series in the line with shunt part of the controller. Examples of these controllers include TCPST, UPFC, TCPAR, and UPQC which will be the device that will study it.[2]



Figure 1.4: combind Shunt-Series connected controllers[1]

1.2 Motivation & Importance

In conventional AC transmission system, the ability to transfer AC power is limited by several factors like thermal limits, transient stability limit, voltage limit, short circuit current limit etc. These limits define the maximum electric power which can be efficiently transmitted through the transmission line without causing any damage to the electrical equipment and the transmission lines. This is normally achieved by bringing changes in the power system layout. However this is not feasible and another way of achieving maximum power transfer capability without any changes in the power system layout. Also with the introduction of variable impedance devices like capacitors and inductors, whole of the energy or power from the source is not transferred to the load, but a part is stored in these devices as reactive power and returned back to the source. Thus the actual amount of power transferred to the load or the active power is always less than the apparent power or the net power. For ideal transmission the active power should be equal to the apparent power. In other words, the power factor (the ratio of active power to apparent power) should be unity. This is where the role of Flexible AC transmission System comes. Regarding control approach, the compensation using passive devices is limited and can't be automatically controlled in conventional grid, however control techniques can be used in custom devices to compensate voltage and current in the urgent conditions.

1.3 Objectives

• enhancement of power quality using unified power quality conditioner device (UPQC), and gets purely uniform sinusoidal signals delivered from source to the load.

• to explore the techniques for removal of current harmonics and mitigate the voltage sag, swell, distortion.

• investigate shunt APF for compensating load current harmonics and so that current drawn from supply is completely sinusoidal.

• investigate series APF so to mitigate voltage dip and rise from source voltage and make load voltage perfectly balanced.

• running linear and nonlinear loads with existence of unified power quality conditioner using MATLAB SIMULINK.

1.4 literature survey

The prime objective of power utility companies is to provide their consumers an uninterrupted sinusoidal voltage of constant amplitude. In addition to this, adherence to different power quality standards laid down by different agencies has become a figure of merit for the power utilities. Unfortunately, this is becoming increasingly difficult to do so, because the size and number of non-linear and poor power-factor loads such as adjustable speed drives, computer power supplies, furnaces, power converters and traction drives are finding its applications at domestic and industrial levels. These nonlinear loads draw non-linear current and degrade electric power quality[4] The quality degradation leads to low power-factor, low efficiency, overheating of transformers and so on. A part from this, the overall load on the distribution system is rarely found to be balanced. In the past, efforts have been made to mitigate these identified power quality problems using con-

ventional passive filters. But their limitations have ignited the need of active and hybrid filters[5]

So most of researches nowadays tend toward subjects about custom devices. The Unified Power Quality Conditioner (UPQC) is one of the key custom power devices, which can compensate both current and voltage related problems simultaneously. As the UPQC is a combination of series and shunt APFs, two APFs have different functions. The series APF isolates voltage-based distortions. The shunt APF cancels current-based distortions. At the same time, it compensates reactive current of the load and improves power factor. There are many scientific papers that obtain control strategies of the unified power quality conditioner that's why the designed model of UPQC depends on the methodology that's followed[5].

UPQC is controlled by an exponential composition algorithm (ECA), which is proposed by the author. The performance of UPQC is examined with a nonlinear load and simulation studies using MATLAB/Simulink verify the satisfactory performance of UPQC and PID controller is used in generating reference. According to resulted data in this paper, the source meets only the real power demand of the load while the reactive power and harmonic demands and voltage sag are met by the UPQC. It's dealt with implementation of unified power quality conditioner (UPQC) to compensate for power quality issues voltage sag, voltage harmonics and current harmonics[2].

Paper [3] presents two control strategies for UPQC which are **Synchronous Reference Frame** (**SRF**) to mitigate voltage distortion and **I** cos θ theory to eliminate current harmonics.

Zero crossing detector, sample and hold circuits are used to generate unit vectors. The Synchronous Reference three phase voltages and currents had been generated and compared with the sensed signals and processed by hysteresis controllers to eliminating the distortion in the signals. The special features in the proposed control scheme is that the supply-neutral current (negative sequence) can be eliminated by mean of the fourth leg (two switches) in the shunt active filter. the current control is applied over the fundamental supply currents instead of the fast-changing APF currents, thus reducing the computational delay. In addition to the load or the filter neutral current is not sensed, hence reducing the current sensors. However, in[1] the total harmonic distortion can be extensively deeply minimized.

In [4] deals with the performance of unified power quality conditioner (UPQC) based on current source converter (CSC) topology and using UPQC to mitigate the power quality problems like harmonics and sag. The reference current and voltage generation for shunt and series converter is based on phase locked loop and synchronous reference frame theory. However the main fault in this model is that using reactor as dc link which has negative consequences on the design of the device due to momentary spikes and electromagnetic interference. The proposed UPQC-CSC design has superior performance for mitigating the power quality problems. Synchronous reference frame theory based control method was applied to control the working of unified power quality conditioner based on current source converter topology. The simulation results show that the device is capable of compensating the current harmonics under unbalanced and nonlinear load conditions, simultaneously mitigating voltage sag and swell .

Paper [5] deals with unified power quality conditioners (UPQC's), which aim at the integration of series-active and shunt-active filters. The proposed system can compensate the sag, swell and unbalance voltage, harmonics and also the reactive power. UPQC has the capability of improving power quality at the point of installation on power distribution systems or industrial power systems, and this paper, presented the compensation principle using PI and Fuzzy control strategies of the UPQC. The Fuzzy controller presents more interesting results according to THD values. The current active and reactive power theory (pq theory) (dq0) was used to determine the reference value of current and voltage.

The results of simulation in MATLAB/SIMULINK obtained show that the UPQC is a FACTS equipment able to compensate all disturbances of voltage and/or current with a great efficiency.

The study in [6] is based on a single-phase unified power quality conditioner (UPQC) to enhance power quality problem in single-phase systems. A simple control approach is implemented and validated through simulation as well as experimental studies. A laboratory prototype of UPQC is designed and developed using a digital signal processor. The performance of UPQC is validated experimentally under several operating conditions. It is found that the UPQC in single-phase system effectively compensates the important power quality issues, such as the load reactive power, load current harmonics, voltage harmonics, voltage sag, voltage swell and voltage flicker. Under distorted source voltage having total harmonics distortion (THD) of 14.1% with a non-linear load producing a distorted current (THD of 30.98%), the UPQC simultaneously compensates these harmonics resulting sinusoidal source current (THD of 3.77%) and load voltage (THD of 2.54%). The simulation results that UPQC with developed single-phase UVTG approach can effectively solve several power quality problems in single-phase system.

Chapter 2

Unified Power Quality Conditioner (UPQC)

A Unified Power Quality Conditioner (UPQC) is relatively a new member of the FACTS devices family. It is a comprehensive FACTS device, with integrated shunt and series active filters. The cost of the device, which is higher than other FACTS devices, because of twin inverter structure and control complexity, will have to be justified by exploring new areas of application where the cost of saving power quality events outweighs the initial cost of installation.

2.1 Block Diagram of Unified Power Quality Conditioner (UPQC)

The UPQC is realized by two voltage source inverters (VSI) back to back connected, which are represented by a combination of series and shunt active power filters (APF) with a common dc link connect between them shown in figure 2.1. Each Filter is realized by 6 IGBT transistors operate as switches.[7]

First of all UPQC has must been connected before the load to process the supply signals before providing them to the load aiming to form purely sinusoidal signal clear from distortion and harmonics[8].



Figure 2.1: Basic block diagram of UPQC[9]

2.1.1 Three Phase Six Pulse Voltage Source Inverter (VSI)

The three phase six pulse voltage source inverter is used to convert the dc power into ac power at adjustable frequency. And the inverter can be used for providing ac supply to 3 phase load or gadgets and it can be used as the converter in STATCOM, a FACTS device. Figure 2.2 shows the basic block diagram of conversion of power in industry or in power transmission system. VSI is an important part of STATCOM for conversion of power used in power system. Figure 2.3 shows the basic block diagram of STATCOM using six pulse VSI connected to power transmission system



Figure 2.2: Block diagram of VSI connected to 3-Phase load[9]



Figure 2.3: Block diagram of VCI connected as an element of STATCOM[9]

The IGBT based VCI, IGBTs are fully control device and they are turned on only for the duration during which a gate pulse is given to it. The Figure 2.4 shows the basic diagram of a six pulse three- phase inverter. In this model, six IGBTs are connected in such a way that each phase of 3-Phase balance load is connected in middle of two IGBTs and they are triggered properly in a particular sequence as the name with number given to each IGBT. And another side is connected to the DC voltage source. A six pulse VSI has less harmonic content than that of directly obtained single pulse ac[11].



Figure 2.4: Basic structure of three-phase six-pulse voltage source inverter[12]

2.1.2 Shunt Convertor (SHUC)



Figure 2.5: Shunt active power filter[12]

the shunt Active Power Filter APF of the three-phase makes the supply currents sinusoidal, balanced, and in phase with the voltage at the point common coupling PCC, it is realized using a three leg VSI or four-leg VSI to eliminate the neutral source current. Pulses comes out from a hysteresis controller to switch on transistors and modifying current signals that is fed to the load.

The job of shunt active power filter here to produce a harmonic with phase shift 180 then the harmonic current which generated from non-linear load So the idea is injecting harmonic current in the ac system similar in amplitude but opposite in phase when compared with load current waveform harmonic In normal conditions, the source is assumed as a perfect sinusoidal voltage i.e

$$V_s(t) = V_m \sin(\omega t) \tag{2.1}$$

When there is a non-linear load in system the load current will have both fundamental component and also harmonics of higher order. This current represent as:

$$il(t) = \sum_{n=1}^{\infty} I_n \sin(n\omega t + \Theta n)$$
(2.2)

Now, the load power is expressed as:-

$$P_{l}(t) = V_{s}(t) * il(t) = I_{1}V_{m}\sin^{2}(\omega t)\cos\Theta_{1} + I_{1}V_{m}\sin(\omega t)\cos(\omega t)\sin\Theta_{1} + \sum_{n=2}^{\infty}V_{m}\sin(\omega t)I_{n}\sin(n\omega t + \Theta n)$$
(2.3)

$$= P_s(t) + P_c(T)$$

In Eq.(2.3) the we define $p_s(t)$ as real power given by utility source, and $p_c(t)$ as the reactive power and the harmonic power, i.e.

$$P_s(t) = I_1 V sm \sin^2(\omega t) \cos(\Theta_1)$$
(2.4)

$$P_c(t) = I_1 V sm \sin(\omega t) \cos(\omega t) \sin \Theta_1 + \sum_{n=2}^{\infty} V_{sm} \sin(\omega t) I_n \sin(n\omega t + \Theta_n)$$
(2.5)

By discussion above know that APF will provide the reactive and harmonic power pc(t), the current supplied by source is given as :-

$$i_s(t) = p_s(t)/v_s(t) = I_1 \cos \Theta_1 \sin(\omega t) = I_s \sin(\omega t)$$
(2.6)

The current is(t) is and utility voltage is seen to be in phase and pure sinusoidal. At this time, the APF will provide the following compensation current in the circuit:

$$i_c(t) = i_l(t) - i_s(t)$$
 (2.7)

2.1.3 Series converter (SERC)



Figure 2.6: Series active power filter[12]

The purpose of this inverter is to maintain the supply voltage. To achieve that as supply voltage is distorted, it can be sensed and provided to a hysteresis controller as load voltage to be compared with reference load voltages that are generated in a control algorithm based on Synchronous Reference Frame (SRF). The hysteresis controller produces switching waveforms that switches transistors of VSI to compensate the distortion in the Voltage signal[12].

Similarly, the series active filter compensation objectives are accomplished by injecting voltages in series with the source voltages such that the load voltages are undistorted and balanced, and their magnitudes are kept at the desired level. This voltage injection is delivered by the DC-link capacitor and the series APF. Based on measured supply and load voltages the control technique produces the appropriate PWM signals for the series APF. In order to produce the injected voltage of desired magnitude, the actual voltage signal is compared with the reference voltage signal and the corresponding error signal is applied to the PWM controller for generation of appropriate switching signals. The DC-link capacitor is consecutively connected to the inverter outputs with positive and negative polarity. The output voltages of the series APF do not have the actual shape of the desired signals. However, it contains switching harmonics, which are filtered out by the series low pass filter. Therefore, the amplitude, phase shift, frequency and harmonic content of injected voltages are controllable[12].

2.1.4 Low Pass Filters

A low pass filter is a filter which passes low-frequency signals and blocks high-frequency signals. In other words, low-frequency signals go through much easier and with less resistance and highfrequency signals have a much harder getting through, which is why it is called low pass filter. Low pass filters can be constructed simply using resistors with either capacitors or inductors. A low pass filter composed of a resistor and a capacitor is called a low pass RC filter. And a low pass filter with a resistor and an inductor is called a low pass RL filter[13].

Passive Low Pass Filter

In the Passive Filter, basic first-order filter circuits, such as the low pass filters can be made using just a single resistor in series with a non-polarized capacitor connected across a sinusoidal input signal as shown in figure 2.7 RC Low Pass filter and figure 2.8 RL Low Pass filter.





Figure 2.8: RL Low Pass filter

The main disadvantage of passive filters is that the amplitude of the output signal is less than that of the input signal, i.e., the gain is never greater than unity and that the load impedance affects the filters characteristics.

With passive filter circuits containing multiple stages, this loss in signal amplitude called Attenuation can become quiet severe. One way of restoring or controlling this loss of signal is by using amplification through the use of Active Filters.

2.1.5 Use of Low Pass Filters in UPQC

Low Pass filters are used in control algorithm of UPQC. Such that a set of low pass filters are used in shifting the source Voltages by +90°. The filters have a 50 Hz cut-off frequency to obtain the magnitude of the fundamental source signal, according to equation 2.8, when the frequency equals cut off frequency the fundamental source signal can be obtained. The filter is designed with specified resistors to make the attenuation factor (AF) as required to provide the desired magnitude of the fundamental signal. The same scenario occurs in current for shunt APF. Processing of output of low pass filter depends on the control strategy that is followed in the design of UPQC.

Equation 2.8 : Output of Low Pass Filter.

$$Vout = A_F * vin/sqrt(1 + ((f_c/f))^2)$$
(2.8)

where

Vout : output of low pass filter.

AF : Attenuation factor or gain expressed as fc : Cut off frequency.

f : Frequency.

Vin : Input to the low pass filter.

2.1.6 DC Link Capacitor

In power conversion, when AC is converted to low voltage DC, or AC from one frequency to another, the AC is usually rectified and smoothed. Once this is accomplished, the power is then routed to an inverter to obtain the final output. The DC that is fed into the inverter is called the DC

link. As the name implies, the two sources are linked together with a filter capacitor.

The device helps protect the inverter network from momentary voltage spikes, surges and electromagnetic interference (EMI). The noise is the result of the pulsed inverter current and High Current DC Link Film Capacitors stray inductance on the DC bus. The selection of the proper DC link capacitor is important to achieve the proper performance of the system[14].

2.1.7 Series Transformer

a transformer between the source and the critical load or the source at the point of common coupling (PCC) connected in series with the line. The necessary voltage which is generated by series APF so that the voltage at load side is perfectly balanced and regulated i.e. Sinusoidal is injected into the transmission line with the help of these transformers. The series transformer turns ratio should be suitable so that injected voltage is suitable such that it injects a compensating voltage which will completely make the load side voltage balanced and also it reduces the current flowing through series inverter.

2.2 From three phase reference frame into Orthogonal rotating reference frame and vice versa.

For such a complex electrical machine analysis, mathematical transformations are often used to decouple variables and to solve equations involving time varying quantities by referring all variables to a common frame of reference. In the UPQC device the input signal is transformed from three vector reference frame into two orthogonal reference frame then into rotating reference frame(dq). This is referred to advantages of two reference frame in reducing the number of compensator's required. In a balanced system, control in abc-frame will require three compensator's while controlling system in dq-frame will only require two compensator's. Regarding controller in abc-frame, the reference signal is sinusoidal in nature and hence PI controllers can't be used as a compensator, and it's needed to design compensators to correctly follow the reference signal, which can be tough as complexity of system increases. Control in dq-frame is same as controlling DC quantities and hence a PI controller can be used as a compensator. Moreover, control of asymmetrical system is not possible in abc-frame however, it can be done in dq-frame.

How rotating reference frame are produced?

Using Clarke and Park transformation. Clarke transformation used to convert signals from three phase into two phase stationary frame and Park is used to convert vectors in balanced two-phase orthogonal stationary system into orthogonal rotating reference frame. Figure 2.9 and 2.10 shows Clark and Park transformations respectively.



Figure 2.9: Clarke transformation[15]



Figure 2.10: Park transformation [15]

Clarke transformation equations :

$$I_{\alpha} = \frac{2}{3} * (I_a) - \frac{1}{3} * (I_b - I_c)$$
(2.9)

$$I\beta = \frac{2}{\sqrt{3}} * (I_b - I_c)$$
 (2.10)

Where I_a , I_b , and I_c are three-phase quantities I_{α} and I_{β} are stationary orthogonal reference frame quantities

Park transformation equations:

$$I_d = I_{\alpha} * \cos(\theta) + I_{\beta} * \sin(\theta) \tag{2.11}$$

$$I_p = I_{\alpha} * \cos(\theta) - I_{\beta} * \sin(\theta)$$
(2.12)

where, I_d , I_q are rotating reference frame quantities I_α , I_β are orthogonal stationary reference frame quantities θ is the rotation angle After processing the signals and solve them mathematically, they must be transformed into three phase reference frame so inverse Park then inverse Clarke transformation should be applied on them.
Inverse Park equations:

$$V_{\alpha} = V_d * \cos(\theta) - V_q * \sin(\theta)$$
(2.13)

$$V_{\beta} = V_d * \cos(\theta) + V_q * \sin(\theta)$$
(2.14)

Inverse Clarke equations:

$$V_a = V_\alpha \tag{2.15}$$

$$V_b = (-V_{\alpha} + \sqrt{3} * V_{\beta})/2 \tag{2.16}$$

$$V_c = (-V_{\alpha} - \sqrt{3} * V_{\beta})/2 \tag{2.17}$$

2.3 State Space Model of UPQC

In the proposed model of UPQC simulation and experimental results for different operating conditions are presented in a single-phase power distribution system as shown in figure 2.11 to validate the control design and its real-time performance.

The distorted supply voltage V_s at the point of common coupling is modelled by the sum of two voltage sources, namely, its fundamental V_{sf} and its harmonics V_{sh} . The nonlinear load is modelled by a distorted current source I_L , which is also made up of its fundamental I_{LF} and its harmonics I_{Lh} that will change with different loadings. The supply current and the load voltage are denoted by I_s and V_s , respectively. Ideally, I_s and V_L should be sine waves of 50 Hz without any harmonic distortions, even though harmonics may exist in V_s and I_L . As such, this is one of the tasks to



Figure 2.11: Equivalent single-phase representation of the UPQC

be accomplished by the UPQC. V_z in Fig.2.11 models the voltage drop across the line impedance $R1 + j\omega L_1$. $u_1(\frac{V_{dc}}{2})$ and $u_2(\frac{V_{dc}}{2})$ model the series and shunt active filters of the UPQC, respectively. Their associated low-pass interfacing filters and losses are modelled by L_{se} , C_{se} , and R_{se} and L_{sh} , C_{sh} , and R_{sh} , respectively. i_{Csh} is the leakage capacitor current of the shunt low-pass interfacing filter. $u_1(\frac{V_{dc}}{2})$ and $u_2(\frac{V_{dc}}{2})$ represent the switched voltages across the series and shunt VSI outputs of the UPQC, respectively. V_{inj} denotes the injected voltage of the series active filter, while I_{inj} denotes the injected current of the shunt active filter. u_1 and u_2 are the two control variables. Kirchhoff's voltage and current laws are applied to the three current loops indicated in Fig2.11 to derive a state space model for the UPQC From loop1

$$V_s = i_1 R_1 + L_1 \frac{di_1}{dt} + v_{inj} + v_L$$
(2.18)

From loop2

$$u_1(\frac{V_{dc}}{2}) = R_{se}i_2 + L_{se}\frac{di_2}{dt} + v_{inj}$$
(2.19)

$$V_{inj} = \frac{1}{C_{se}} \int (i_1 + i_2) dt$$
 (2.20)

From loop 3

$$u_{2}(\frac{V_{dc}}{2}) - i_{inj}R_{sh} - L_{sh}\frac{di_{inj}}{dt} = v_{L}$$
(2.21)

$$i_s + i_{inj} - i_{Csh} = i_L \tag{2.22}$$

In addition,

$$i_1 = i_s \tag{2.23}$$

$$i_2 = i_s e \tag{2.24}$$

$$i_3 = i_{Csh} \tag{2.25}$$

where i_{se} is the current flowing through R_{se} and L_{se}

Rearranging above equations the following state space representation for the plant and its state vector can be derived:

$$x^* = A * x + B_1 (v_s i_L)^T + B2u$$
(2.26)

$$x = \begin{bmatrix} is \\ i_{se} \\ i_{inj} \\ v_{inj} \\ vc_{sh} \end{bmatrix}$$
(2.27)

$$A = \begin{bmatrix} -R_1/L_1 & 0 & 0 & -1/L_1 & -1/L_1 \\ 0 & -R_{se}/L_{se} & 0 & -1/L_{se} & 0 \\ 0 & 0 & -R_{sh}/L_{sh} & 0 & -1/L_{sh} \\ 1/C_{se} & 1/C_{se} & 0 & 0 & 0 \\ 1/C_{sh} & 0 & 1/C_{sh} & 0 & 0 \end{bmatrix}$$
(2.28)

$$B1 = \begin{bmatrix} -1/L_1 & 0\\ 0 & 0\\ 0 & 0\\ 0 & 0\\ 0 & -1/C_{sh} \end{bmatrix}$$
(2.29)

$$B2 = \begin{bmatrix} 0 & 0\\ (\frac{V_{dc}}{2}) * L_{se} & 0\\ 0 & (\frac{V_{dc}}{2}) * L_{sh}\\ 0 & 0\\ 0 & 0 \end{bmatrix}$$
(2.30)

 $u = [u1 \ u2]^T$ and the output equation is given by

$$Y = C * X + D1 * (v_s i_l)^T + D2 * u$$
(2.31)

where C=[0 0 0 0 1;1 0 0 0 0] D1=D2[0 0;0 0]

In this state-space model, the supply voltage v_s and the load current I_L are considered as exogenous inputs, which act like disturbances to the plant. The load voltage v_L and the supply current I_s are then considered as outputs of the plant, which are to be maintained as pure sine waves of 50 Hz, as well as to help in achieving a unity power factor at the supply side. The variables u_1 and u_2 are regarded as the control inputs to the plant. It is worth mentioning that the state-space model of the UPQC in equation (2.27) and (2.32) is a multi-input-multi-output system such that it does not treat the series and shunt active filters as two separate systems. Rather, a coordinated control is applied to operate the series and shunt active filters of the UPQC in a unified manner more effectively and efficiently.

2.4 UPQC PARAMETERS

The mathematical modeling of the UPQC is the designing of two voltage source converter (VSC) connected back to back. The design of three phase UPQC is the design of three leg series VSC and three leg shunt VSC which is shown in Fig.2.12 The parameters of the VSC should be designed deliberately for better performance [17]. The critical parameters that should be taken into consideration while designing UPQC are DC link voltage (Vdc), DC link capacitor (Cdc), shunt interfacing

inductance (Lf), series interfacing inductance (Lse), series capacitor (Cse) and the switching frequency (fsw). A. Shunt VSC Parameters Fig.2.12 shows the proposed configuration of one of the shunt VSC of 3-phase, 3-wire ac plant system. It is utilized a 3-leg VSC. The VSC, shunt interfacing inductors and theshunt ripple filter are estimated here for accurate selection. The DC capacitor associated at the basic DC bus goes about as a energy support and builds up a DC voltage for the ordinary operation of the shunt VSC and additionally arrangement of series VSC. The DC bus voltage (Vdc), DC bus capacitance (Cdc), interfacing inductors (Lf) and voltage and current rating of switches are determined according to the methods as follows. A three-leg VSC is utilized as a shunt and this topology has six IGBTs, three inductors and a dc capacitor. The compensation to be given by the shunt VSC chooses the rating of the VSC parts.

2.4.1 Estimation of DC Link Voltage

The minimum DC bus voltage of VSC of shunt have to be greater than twice of the crest of the phase voltage of the ac electrical system. The DC bus voltage is evaluated as[17],

$$u = \frac{V_c}{V_{Tri}} \tag{2.32}$$

$$V_{dc} = \frac{2\sqrt{2V_{LL}}}{\sqrt{3u}} \tag{2.33}$$

where V_{LL} is line to line voltage, and u the modulation index which can be calculated by the ratio of the magnitude of control voltage signal (V_c) and magnitude of the triangular signal V_{Tri} . which is generally kept constant. u is less than 1 under normal operating condition.

2.4.2 Estimation of DC Link Capacitor

In general magnitude of the capacitance (C_{dc}) can be evaluated as,

$$C_{dc} = \frac{Q}{V} \tag{2.34}$$

where Q charge storing and V is the potential difference. In the UPQC the charge can be evaluated as follows,

$$Q = alt_{rec} \tag{2.35}$$

In Fig 2.12 the estimation of DC capacitor (C_{dc}) of VSC of shunt relies on upon the instantaneous energy (ΔE) accessible to the shunt under transient condition. The principle of energy conservation can be evaluated actual magnitude of the capacitance. The practical value of the C_{dc} can be calculated as follows,

$$C_{dc} = 6 * \frac{\Delta E}{V_{dc.ref}^2 - V_{dc.act}^2} = 6 * \frac{V_{rms}(alt_{rec})}{V_{dc.ref}^2 - V_{dc.act}^2}$$
(2.36)

where $V_{dc.ref}$ is reference DC bus voltage, $V_{dc.act}$ is the actual DC bus voltage, V_{rms} is phase voltage, I is the phase current, a is the load factor and t_{rec} is the recovery time of the charge.

2.4.3 Estimation of Interfacing Inductor

An empirical formula has been selected for various values of the interfacing inductance (L_f) of a shunt and series VSC. It depends on the current ripple peak to peak (I_{rip}) , switching frequency (f_{sw}) , dc bus voltage (V_{dc}) . In normal condition the reactive inductance (X_f) value can be evaluated as follows,

$$X_f = 2 * \pi * f_{sw} * L_f \tag{2.37}$$

$$X_f = \frac{V_{dc}}{I_{rip}} \tag{2.38}$$

from equation (2.38) and (2.39) the interfacing inductor value can be explained as under normal condition,

$$L_f = \frac{V_{dc}}{2 * \pi * f_{sw} * I_{rip}}$$
(2.39)

If the overloading factor is 1.2, the numerical value of the L_f can be evaluated as follows,

$$L_f = \frac{V_{dc}}{2 * \pi * f_{sw} * 1.2 * I_{rip}}$$
(2.40)

2.4.4 Estimation of Switch (IGBT)

This could be selected on the basis of DC link voltage V_{dc} , I_{rip} and the peak source current (I_{speak}). The voltage rating of switch (IGBT) is the sum of DC link voltage and 10% of V_{dc} . The voltage switch rating V_{sw} and current switch rating I_{sw} can be evaluated as,

$$V_{sw} = V_{dc} + 10 \tag{2.41}$$

$$I_{sw} = 1.25 * (I_{rip} + I_{speak})$$
(2.42)

The first order high-pass filter tuned at half of the switching frequency is applicable to filter out the harmonics of the voltage at PCC. The time constant of the filter is one tenth of the fundamental time period (T), which can be evaluated as the *Rse Cse* $\ll T/10$, where *Rse* and *Cse* are the ripple filter resistance and its capacitance respectively.

2.4.5 Estimation of Series VSC Parameters

In Fig 2.12, proposed configuration of the UPQC of 3-phase, 3-wire ac electrical system, applies a 3-leg VSC isolated with a series voltage injection transformer. The VSC, isolated inductor, series voltage injection transformer and the filter are designed. The three single phase transformer is connected through 3-leg series VSC. Each transformer provides isolation between the converters and supply system. It also match the voltage and current rating of the converters with the power system. The design of the transformer shows that the windings voltage ratings are 220 V/ 110 V. (2:1) in ratio. The current rating depends on the considered load. The transformer windings on converter side are connected in delta to take care of core non-linearity. This helps remove the triplen harmonics that can occur due to independent magnetic fluxes of three single-phase transformers, which do not add up to zero.

Estimation of the Interfacing Inductor

The interfacing inductor $L_s e$ has been designed based on theswitching frequency of the series VSC and it can be estimated as follows,

$$L_{se} = \frac{V_{dc}}{\sqrt{3} * 4 * f_{sw} * I_{rip}}$$
(2.43)

Estimation of the Series Capacitor

The series capacitor injecting the current I_{Cse} with the two component, one is fundamental current I_{Cf} and second is switching current I_{Csw} . The corresponding to the fundamental current the

fundamental voltage V_{Cf} is produced which can be evaluated as follows,

$$V_{Cf} = I_{Cf} * X_{Cf} = \frac{I_{Cf}}{2 * \pi * f * C_{se}}$$
(2.44)

The series filter capacitor value can be estimated as follows,

$$C_{se} = \frac{I_{Cf}}{2 * \pi * f * V_{Cf}}$$
(2.45)



Figure 2.12: Proposed configuration of 3-phase 3-wire of the UPQC for ac electrical system

2.5 UPQC at low voltage

Why Low Voltage was chosen?

The unified power quality conditioner (UPQC) is considered as measurement device that needs high accuracy in determining power quality problems from sag, swell and distortion in the signal. In High voltage the required elements used needs very large parameters to realize these measurement procedures and control techniques. When a load is connected to the inverter output, the output voltage at the load side is sensed by means sensors and it is feedback to a comparator compares this load output with the reference signal (desired signal) and it produces the voltage error signal. The required sensors in low voltage (domestic grid) are lower in cost and smaller in size. Moreover, it can be realized and give the best accurate results. The dc link compensation can be reduced in low voltage, so the size of dc link capacitor would be smaller than one used in high voltage. In addition of protection procedure and devices used in low voltage have smaller parameters

and overall ratings. Also require low isolation cost. In the other hand, high and medium voltage needs a very high protection and measurement costs beside the parameter sizing and problem of physical realization of equipments.

2.6 Application of UPQC

Unified Power Quality Conditioner solves many of the power quality problems in the power grid. The most important of these problems are:

2.6.1 Harmonics distortion

Definition: Voltage or current waveforms assume non-sinusoidal shape. The waveform corresponds to the sum of different sine-waves with different magnitude and phase, having frequencies that are multiples of power-system frequency.

Causes: Classic sources: electric machines working above the knee of the magnetization curve (magnetic saturation), arc furnaces, welding machines, rectifiers, and DC brush motors. Modern sources: all non-linear loads, such as power electronics equipment including, switched mode power supplies, data processing equipment, high efficiency lighting.

Consequences: Increased probability in occurrence of resonance, neutral overload in 3-phase systems, overheating of all cables and equipment, loss of efficiency in electric machines, electromagnetic interference with communication systems, errors in measures when using average reading meters, nuisance tripping of thermal protections[18].

Total Harmonic Distortion THD Total harmonic distortion (THD) is a measurement that tells you how much of the distortion of a voltage or current is due to harmonics in the signal, should typically, but not always (i.e square wave), be as low as possible.[18]

Calculating Total Harmonic Distortion

THD is defined as the ratio of the equivalent root mean square (RMS) voltage of all the harmonic frequencies (from the 2nd harmonic on) over the RMS voltage of the fundamental frequency (the fundamental frequency is the main frequency of the signal, i.e., the frequency that you would iden-

tify if examining the signal with an oscilloscope). Equation 2.47 shows the mathematical definition of THD:

$$THD = \frac{V_{eqrmswithharmonic}}{V_1}$$
(2.46)

$$V_{n_rms} = \sum_{n=2}^{\infty} V_n^2 \tag{2.47}$$

 V_{n_rms} is the RMS voltage of the nth harmonic. V_1 is the RMS voltage of the fundamental frequency. n is the harmonic order.

Current harmonic compensator

The shunt active power filter of the UPQC can compensate all undesirable current components generated by non-linear load, including harmonics, imbalances due to negative and zero sequence components at the fundamental frequency. In order to cancel the harmonics generated by a nonlinear load, the shunt inverter should inject a current as governed by the following equation:[18][19]

$$IC(\omega t) = IL(\omega t) - IS(\omega t)$$
(2.48)

Where $IC(\omega t)$, $IL(\omega t)$ and $IS(\omega t)$ represent the shunt inverter current, reference load current, and actual source current, respectively.

Voltage Harmonics Compensation

The series active power filter of the UPQC can compensate the supply voltage related problems by injecting voltage in series with line to achieve distortion free voltage at the load terminal. The series inverter of the UPQC can be represented by following equation:

$$VC(\omega t) = VL(\omega t) - VS(\omega t)$$
(2.49)

Where $VC(\omega t)$, $VL(\omega t)$ and $VS(\omega t)$ represent the series inverter voltage, reference load voltage, and actual source voltage, respectively[18][19].



Figure 2.13: voltage harmonic & voltage compensation

2.6.2 Voltage fluctuations

Definition: a voltage fluctuation is a systematic variation of the voltage waveform or a series of random voltage changes, of small dimensions, namely 95 to 105% of nominal at a low frequency, generally below 25 Hz.

Causes: Arc furnaces, frequent start/stop of electric motors (for instance elevators), oscillating loads.

Consequences: most perceptible consequence is the flickering of lighting and screens, giving the impression of unsteadiness of visual perception[18].

Unified Power Quality Conditioner is made of shunt & series converter as described. The Series converter is used to overcome voltage fluctuations i-e flickers. It compensates the voltage to the desired magnitude taking distribution voltage as reference voltage. Series converter supplies a smooth voltage to the load and improves power quality of the systems[19].



Figure 2.14: voltage fluctuations & compansation voltage[22]

2.6.3 Voltage imbalance

Definition: A voltage variation in a three-phase system in which the three voltage magnitudes or the phase angle differences between them are not equal.

Causes: Large single-phase loads (induction furnaces, traction loads), incorrect distribution of all single-phase loads by the three phases of the system (this may be also due to a fault).

Consequences: Unbalanced systems imply the existence of a negative sequence that is harmful to all three phase loads. The most affected loads are three-phase induction machines[18].

To remove supply voltage imbalance from the load terminal voltage by a series voltage-source converter connected in series with the AC line. Control of series converter output voltage is usually performed by pulse-width modulation (PWM). The gate pulses required for converter are generated by fundamental input voltage reference signal. For balanced sinusoidal voltage and fixed amplitude.[20].



Figure 2.15: Voltage imbalance & compansation

2.6.4 Reactive power compensation

compensate reactive current of load, and improve the power factor by a voltage-source converter connected in shunt with the same AC line in UPQC and The shunt active filter is responsible for power factor . it maintains constant average voltage across the DC storage capacitor. The series active filter compensation goals are achieved by injecting voltages in series with the supply voltages such that the load voltages are balanced and undistorted, and their magnitudes are maintained at the desired level. This voltage injection is provided by dc storage capacitor and the series VSI .The gate pulses required for converter are generated by fundamental input current reference signal[20][22].

2.6.5 Voltage events

Voltage Sag

Definition: A decrease of the normal voltage level between 10 and 90% of the nominal rms voltage at the power frequency, for durations of 0.5 cycle to 1 minute.

Causes: Faults on the transmission or distribution network (most of the times on parallel feeders). Faults in consumer's installation. Connection of heavy loads and start-up of large motors.

Consequences: Malfunction of information technology equipment, namely microprocessor-based control Systems (PCs, PLCs, ASDs, etc) that may lead to a process stoppage. Tripping of contactors and electromechanical relays. Disconnection and loss of efficiency in electric rotating machines[18].

Voltage Swell

Definition: Momentary increase of the voltage, at the power frequency, outside the normal tolerances, with duration of more than one cycle and typically less than a few seconds.

Causes: Start/stop of heavy loads, badly dimensioned power sources, badly regulated transformers (mainly during off-peak hours).

Consequences: Data loss, flickering of lighting and screens, stoppage or damage of sensitive equipment, if the voltage values are too high[18].

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solution of voltage events

The dc link voltage of the Unified Power Quality Conditioner (UPQC) can significantly deviate from its reference during a transient event, caused by load connection/disconnection or/and supply side voltage sag/swell, though in the steady state the average dc link voltage is maintained at a certain present level. During such transients, due to considerable dc link voltage deviation, the magnitude of the series injected voltage cannot be constant and this has an effect on the load voltage magnitude, which fluctuates. An improved sinusoidal pulse width modulation (PWM) voltage controller for the series compensator is proposed which adjusts continuously the amplitude modulation ratio in response to the dc link voltage deviations. Also, an adaptive dc link voltage controller is proposed which limits the dc link voltage deviation during transients and assures a negligible steady-state error. There exist dc link voltage transients during which the average voltage across the dc link capacitor deviates from its reference value. Such transients can occur when a load is either connected or disconnected to/from the UPQC or a voltage sag/swell on the supply side takes place. The severity of the dc link voltage deviation depends on the depth of the source voltage sag/swell, the size of the load connected/disconnected to/from the UPQC, the dc link capacitor rating, and the performance of the dc link voltage controller .for example the situations when Vdc <0.7854 Vdcref should be avoided, otherwise, the magnitude of the fundamental component of the series inverter output voltage is lower than $Vdc_{ref}/2$. Thus, by some means, the dc link voltage drop has to be limited to 21.46% of Vdcref. Also, the dc link transient overvoltage has to be limited to some reasonable value[22].

Source current tracking method

After generating reference signal by means of Park and Clarke transformation mentioned in this chapter, a suitable modulation technique should be used for tracking the reference.

Feedback controller

Hysteresis controller is used because it's simple and robust. A hysteresis band is built by adding and subtracting suitable offset values to the reference. Source current (*Is*) is continuously compared with top and bottom bands to generate switching pulses. DC link is connected in aiding or opposing mode with value equal to source voltage *Vs* to control Is with a hysteresis band. When lower group of switches in on mode increases Is and upper ones decreases it. The dc offset is removed by interrupt service routine. The moving average filter is used to extract dc component of V_{dp} and V_{dp} , calculate the dc link voltage and can be FIR finite impulse response- filter to reduce noise. The signal is segmented into 360 samples denoted by T. Fundamental frequency considered for $V_{dc} link V_{qp}$ and V_{dp} . The sum of 360 samples is calculated and divided by number of samples according to following equations (2.51),(2.52) [23] :

$$sumn = sumn - 1 + samplen - samplen - 360$$
(2.50)

$$Avg = sumn/360 \tag{2.51}$$

Error between ref dc link Vdclink and average dc link voltage. Error passed through PI controller. Implementation of PI controller satisfied by the following equations(2.53) and (2.54)

$$u(t) = KpE(t) + Ki \int_0^T E(t)dt$$
(2.52)

u(t): controllerout put Kp: proportional constant Ki: Integral constant E(t): error(Vdc_{error}).

$$Irefmag(n) = KpVdc_{error}(n) + Ki \triangle t \sum_{(k=0)}^{(k=n)} V_dc_{error}(k)$$
(2.53)

$\triangle t$: sampling interval

The summation term of integral is calculated as a running sum in order to avoid numerous summing operations in every step. Therefore the final PI equation in discrete form can be written as shown

in equations (2.55) and (2.56)

$$Ki_{sum}(n) = Ki_{sum}(n-1) + K_i^{\dagger} V dc_{error}(n)$$
(2.54)

$$Iref_{mag}(n) = KpVdc_{error}(n) + Ki_{sum}(n)$$
(2.55)

 $K_i^{\scriptscriptstyle \parallel}$: the new integral constant

The Ziegler-Nichols PI tuning method can be followed to obtain the proportional and integral constants. Initially, integral constant Ki was set to zero. The value of the proportional constant was increased in small steps until an oscillatory response in the dc link voltage was observed. The proportional constant is fixed at around 60% of the value at which the DC voltage oscillations were observed. Once the value of the Kp is fixed, the Ki' term is introduced. The Ki'term is adjusted such that the DC link voltage reaches the set value in a reasonable time period, keeping the overshoot within the acceptable limit (within 400 V).



Figure 2.16: voltage sag & compansation



Figure 2.17: voltage swell & compansation



Figure 2.18: simulink model of simulation of sag, swell, unbalance & distortion

Chapter 3

UPQC model

The model has three stages first is the controller of UPQC, second one is the converters connected to the transformers and the third stage is the load which want to solve its problem. Refer to picture below the three stage is obvious to us.



Figure 3.1: UPQC model

3.1 converters

This section explained the second part that is converters with RLC filters and dc link that represent the dc source of inverters and the job of each one ,because the converters injection the signal that correct the signal source and get rid of the harmonics .the picture below represent MC-UPQC (multi-converter UPQC) and this model use to deal with two loads at two buses as shown in the model .



Figure 3.2: UPQC converters

Each inverter construct form 6 IGBT transistors each transistor take a pules from the controller to control its output and to have the injection signal that wants to correct the source signal and cancellation the disturbance and harmonic in the signal .this signal will passes in RLC filter the goal of these filters are employed to mitigate generated harmonics whereas high rating capacitors are employed to enhance the power factor of the electrical supply system. However, these passive filters have fixed compensation, bulky and produce resonance in power network. These demerits of the passive filters in power networks have encouraged the use power electronics-based equipment to enhance the power quality problem under dynamic condition. Such device is known as Active Power Filter (APF (inverters)) so each part of this model complementary to the other.



Figure 3.3: construct converters

3.2 UPQC Controllers

3.2.1 Shunt Controller

The shunt controller is shown in figure 3.4 lock diagram of shunt controller.



Figure 3.4: Block diagram of shunt controller

The reference dc voltage is compared with actual dc Voltage. The Three phase sequence is transformed into rotating reference frame dq0. This had been performed by Park and Clarke transformation equations as shown in figure 3.5 modelling of Park and Clarke equations.



Figure 3.5: modelling of Park and Clarke equations

3.2.2 Phase Locked Loop PLL

The key to the operation of a phase locked loop, PLL [24], is the phase difference between two signals, and the ability to detect it. The information about the error in phase or the phase difference between the two signals is then used to control the frequency of the loop.

To understand more about the concept of phase and phase difference, it is possible to visualise two waveforms, normally seen as sine waves, as they might appear on an oscilloscope. If the trigger is fired at the same time for both signals they will appear at different points on the screen.

The linear plot can also be represented in the form of a circle see figure 3.6. The beginning of the cycle can be represented as a particular point on the circle and as a time progresses the point on the waveform moves around the circle. Thus a complete cycle is equivalent to 360° or 2π radians. The instantaneous position on the circle represents the phase at that given moment relative to the beginning of the cycle.[24]

The concept of phase difference takes this concept a little further. Although the two signals we



Figure 3.6: circle representation of phase plot

looked at before have the same frequency, the peaks and troughs do not occur in the same place.

There is said to be a phase difference between the two signals. This phase difference is measured as the angle between them. It can be seen that it is the angle between the same point on the two waveforms. In this case a zero-crossing point has been taken, but any point will suffice provided that it is the same on both. This phase difference see figure 3.7 can also be represented on a circle because the two waveforms will be at different points on the cycle as a result of their phase difference. The phase difference measured as an angle: it is the angle between the two lines from the centre of the circle to the point where the waveform is represented.

Components of phase locked loop

• Phase comparator / detector: As the name implies, this circuit block within the PLL compares the phase of two signals and generates a voltage according to the phase difference between the two signals, the proposed PLL in this project is a frequency detector not sensitive detector.

• Voltage controlled oscillator, VCO: The voltage controlled oscillator is the circuit block that generates the radio frequency signal that is normally considered as the output of the loop. Its frequency can be controlled over the operational frequency band required for the loop.

• Loop filter: This filter is used to filter the output from the phase comparator in the phase locked loop, PLL. It is used to remove any components of the signals of which the phase is being compared from the VCO line, i.e. the reference and VCO input. It also governs many of the characteristics



Figure 3.7: Shunt Controller



Figure 3.8: phase difference between two signals

of the loop including the loop stability, speed of lock, etc.

PID controller parameters Kp,Ki and Kd are 180, 3200 and 1 respectively.[26]

Operation of PLL



Figure 3.9: Basic Block diagram of PLL

The basic concept of the operation of the PLL is relatively simple, although the mathematical analysis and many elements of its operation are quite complicated.

Three-phase distorted supply voltages are sensed and given to PLL which generates two quadrature unit vectors (sinwt,coswt).

The diagram for a basic phase locked loop shows the three main element of the PLL: phase detector, voltage controlled oscillator and the loop filter see figure 3.8 Basic Block diagram of PLL.

In the basic PLL, reference signal and the signal from the voltage controlled oscillator are connected to the two input ports of the phase detector. The output from the phase detector is passed to the loop filter and then filtered signal is applied to the voltage controlled oscillator.

The Voltage Controlled Oscillator, VCO, within the PLL produces a signal which enters the phase detector. Here the phase of the signals from the VCO and the incoming reference signal are compared and a resulting difference or error voltage is produced. This corresponds to the phase difference between the two signals.

The error signal from the phase detector passes through a low pass filter which governs many of the properties of the loop and removes any high frequency elements on the signal.

Once through the filter the error signal is applied to the control terminal of the VCO as its tuning voltage. The sense of any change in this voltage is such that it tries to reduce the phase difference and hence the frequency between the two signals. Initially the loop will be out of lock, and the error voltage will pull the frequency of the VCO towards that of the reference, until it cannot reduce the error any further and the loop is locked.

When the PLL, phase locked loop, is in lock a steady state error voltage is produced. By using an amplifier between the phase detector and the VCO, the actual error between the signals can be reduced to very small levels. However some voltage must always be present at the control terminal of the VCO as this is what puts onto the correct frequency.

The fact that a steady error voltage is present means that the phase difference between the reference signal and the VCO is not changing. As the phase between these two signals is not changing means that the two signals are on exactly the same frequency. After that the signal can be converted from three phase reference frame into rotating frame dq0. Then the signal passes through the second order filter.

Second order filter: According to the state space model equations that were derived in the State space model section in chapter 2 the Matlab Simulink environment provide us with a second order filter blocks that perform the code1 in Appendix A: Based on the filter type selected in the block menu, for the proposed UPQC model the Second order filter block selected to implement the following transfer function:

Low-pass filter:

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta \,\omega_n s} \tag{3.1}$$

High-pass filter:

$$H(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3.2}$$

S=Laplace operator

 ω_n =natural frequency;

 ζ =damping ratio (called Zeta);

The key characteristics of the second order filter block are:

• Input accepts a vectorized input of N signals, implementing N filters. This feature is particularly useful for designing controllers in three-phase systems (N = 3).

• Filter states can be initialized for specified DC and AC inputs.

• It enables you to compute and plot filter response.

The Block is filled with controller parameters:

• Natural frequency ω_n

• And damping ratio zeta = 0.707

Damping ratio was found according to the following equation:

$$\mathbf{Q} = 1/(2 * \boldsymbol{\zeta});$$

$$\mathbf{Q} = f/\Delta f$$
 ;

Q: quality factor

 Δf : Bandwidth of the signal

Bandwidth of the signal The lower frequency and upper frequency are found at 70.7% of the max value of signal -rms so that Bandwidth of the required signal is 70.72Hz.



Figure 3.10: step response of high pass filter



Figure 3.11: step response of low pass filter

The error is found from the deference between actual dc and reference dc value is found in each case by the program in each case, and it's compensated into the filtered d component. The produced signal (Iabc load) is subtracted from unfiltered d component. Then the dq0 is transformed again into appropriate three phase reference frame abc. Then the difference between the reference signal and shunt current Iabc is taken continuously if they are greater than zero this activate the VSC2 for shunt compensation.

3.2.3 Series Controller

The series controller is shown in figure 3.12 Block diagram of series controller.

Zero-Order Hold block The Zero-Order Hold block is a bus-capable block. The input can be a virtual or nonvirtual bus signal. No block-specific restrictions exist. All signals in a nonvirtual bus input to a Zero-Order Hold block must have the same sample time, even if the elements of the associated bus object specify inherited sample times.

Controller operation Three phase voltage frame ($Vabc1_load$) is converted into dq0 by the same technique. The PLL is used for the same purpose in shunt controller (extraction of two quadrature components) coswt and sinwt to keep the system in sequence. Then the reference signal produced again by inverse conversion of PARK and Clarke mentioned in chapter 2 see figure 3.13. The reference signal is used to generate pulse using 3 arm 6 pulses PWM generator see figure 3.14 that generates appropriate pulses for series convertor to compensate in series.



Figure 3.12: Block diagram of series controller



Figure 3.13: inverse conversion of PARK and Clarke

The three phase reference is compared with triangular waveform to generate three pulses for three IGBT transistors. Three phase reference is multiplied by negative gain (-1) to generate the three pulses of opposite three IGBT transistors.



Figure 3.14: 3 arm 6 pulses PWM generator [27]

3.3 Linear and non-linear loads

3.3.1 Linear load

A Linear Loads have a current waveform that is proportional to the amount of voltage applied. If the voltage doubles the current doubles as well, maintaining a near perfect sinewave, creating no harmonics. Examples of the types of linear loads are: incandescent lamps, heaters, power factor improvement capacitor and resistors.

The linear load contained in this project is the RL Load Series, which is the sensitive load on the network and that must be protected from any network disturbances and harmonics caused by the non-linear load.



Figure 3.15: linear load, RL load

RL Series

A circuit of 2 component a resistor and an inductor connected in series.

$$VL + VR = 0 \tag{3.3}$$

$$L\frac{di(t)}{i(t)} + Ri(t) = 0$$
(3.4)

$$\int \frac{di(t)}{i(t)} = -\int \frac{R}{L} dt$$
(3.5)

$$\ln i(t) = -\frac{R}{L}t + c \tag{3.6}$$

$$i(t) = e^{\left(\frac{-R}{L}t+c\right)} \tag{3.7}$$

$$i(t) = Ae^{\left(\frac{R}{L}t\right)}$$
(3.8)

3.3.2 non-linear loads

A Non-linear load in which the current is not proportional to the voltage. Non-linear loads are closely related to modern electronic equipment that often depends on the power supply in the line-operated switch mode. These loads create a consistent deformation that can have harmful effects on your equipment. Examples of non-linear loads include: variable frequency drives (VFDs), arc furnaces, and other uninterruptible power sources. These days the number of nonlinear loads in power systems is increasing dramatically. These nonlinear loads inject harmonic currents and voltages. Due to widespread usage of nonlinear loads in distribution systems, the harmonic distortion of the current and voltage increase. Power quality of distribution networks is severely affected due to the flow of harmonics. These harmonics can cause serious problems in power systems, excessive heat of appliances, components aging and capacity decrease, fault of protection and measurement devices, lower power factor and consequently reducing power systems. and the amount of the

harmonics caused by the nonlinear loads in residential, commercial and office loads and also estimates the loss of energy due to nonlinear loads harmonics.

Computers, office automation, inverter air conditioning systems, adjustable speed heating ventilation, uninterruptible power supplies (UPSs), personal computers (PCs), and entertaining devices cause drastic amount of for example, inverter air-conditioning system is one of the newest types of non-linear load among customer appliances. Traditional air conditioners contain a compressor driven by a single-speed induction motor and exhibit cooling capacity whereas compressor speed of inverter air conditioner is controlled by an inverter driven variable-speed motor. The drive circuit draws a non-sinusoidal, harmonic-rich current when supplied with sinusoidal voltage from the service power network. Such harmonic currents are known to produce undesirable effects in power systems. It is unlikely that one inverter air conditioner would draw enough harmonic current to have a perceptible effect on the power distribution system. However, if many such inverter air-conditioner loads are connected to a given distribution feeder then large amount of harmonic current drawn by these air conditioners would cause significant power quality disturbances.

The non-linear load that was used in this project is a diode bridge rectifier and was connected to the network to study harmonics, voltage problems (voltage sag, voltage swell) and other problems on the network and test the model of the device that was designed and connected on the network between the source and the load to solve these problems that may Caused by this load.



Figure 3.16: non-linear load, diode bridge rectifier

Harmonic Power for Nonlinear Loads:

If a signal contains harmonics, the Individual Harmonic Distortion (IHD) for any harmonic order is defined as the percentage of the harmonic magnitude respect to the fundamental value.

$$V_h(\%) = 100 * \frac{V_h}{V_1} \tag{3.9}$$

$$I_h(\%) = 100 * \frac{I_h}{I_1} \tag{3.10}$$

for determining the level of harmonic content in an alternating signal, the term "Total Harmonic Distortion" (THD) of the current and voltage signals are used widely.

THD is defined as the ratio of the root-mean-square of the harmonic contents to the root-mean square value of the fundamental quantity, expressed as a percentage of the fundamental. So, the current and voltage THD of a harmonic polluted waveform can be expressed as:

$$THD_I = \frac{\sqrt{\sum_{h=2}^{\infty} I_n^2}}{I_1} * 100$$
(3.11)

$$THD_V = \frac{\sqrt{\sum_{h=2}^{\infty} V_n^2}}{I_1} * 100$$
(3.12)

The apparent power of a signal containing harmonics is calculated by the equation 3.13.

$$S^{2} = (VI)^{2}$$

$$= (V^{2} * (1 + THD_{V})) * (I^{2} * (1 + THD_{I}))$$

$$= (S_{1} * (1 + THD_{V}^{2})) * (1 + THD_{I}^{2})$$
(3.13)

Nonlinear loads can be considered as harmonic real power sources that inject harmonic real power into the distribution system which is product of the harmonic voltage and harmonic current of the same orders. Although this power is much smaller than the fundamental real power, the presence of the distortion power caused by harmonics will result in increased losses flowing through the utility supply system.

For a linear load, the loss of the utility is $I_1^2 * R$. With current distortion discussed above, the loss would be as:

$$Loss = RI^{2} = R(I1^{2} + \sum_{n=2}^{\infty} In^{2}) = RI_{1}^{2}(1 + THD_{I}^{2})$$
(3.14)

For a three-phase utility, the total losses are:

$$P = R_P I_P^2 + R_N I_N^2 (3.15)$$

Where I_P is the phase current of the balanced network and IN is the neutral line current. The harmonic losses are:

$$Loss = R_P I_P^2 + R_N I_N^2$$

$$R_P \sum_{h=1}^{\infty} (I_{ah}^2 + (I_{bh}^2 + (I_{ch}^2) + R_N \sum_{h=1}^{\infty} (I_{Nh}^2)$$
(3.16)

Where I_{ah} , I_{bh} , and I_{ch} are the order h currents in phase A, B and C respectively, and I_{Nh} is the order h harmonic neutral current. R_P and R_N are the phase and neutral resistances. The loss of the neutral current can be considerable so that it can be the main part of the harmonic power loss. Two typical problems can overload the neutral conductor. One is unbalanced single phase loads and the other one occurs when the line to neutral voltage is badly distorted by the triple harmonic voltage drop in the neutral current.

After simulating the non-linear load on the MATLAB Simulink program and extracting the current signal of this load, it is a current wave that has many problems and harmonics, and this is the wave that affects the source and makes its wave non-sinusoid and creates many problems in the electricity network.



Figure 3.17: Non-linear load current wave

3.4 Simulation Results

UPQC performance is tested under this environment with variation conditions such as current harmonics, voltage harmonics, voltage sagging and bloating compensation. Difference and change in the values of the THD Before and after installing the UPQC device, the THD value will be higher than the value after installing the UPQC device on the network. Note : all figures represent the voltage with time or the current with time to be the axis clear for readers .

3.4.1 Distorted Utility voltage

The distortion in utility voltage is introduced deliberately by injecting 5th, 7th order voltage harmonics, keeping major content of triplen harmonics. The resulting highly distorted source voltage 1&2 waveform is shown in the Fig 18 &Fig 19, THD of source1 of 22.08 %, THD of source2 of 35.18%. the current drawn by loads with such distorted voltage would be highly distorted, as viewed from the Fig 29.c . Here THD of the load current ILoad1 36.45% due to the distorted voltage present at source1. The harmonic spectrum of load1 current Iload1 under distorted voltage is shown in the Fig 22.when connected the UPQC and start compensation the voltage wave becomes sinusoidal as shown in Fig 20&Fig 21



Figure 3.18: Vsource1 without UPQC



Figure 3.19: Vsource2 without UPQC







Figure 3.21: Vsource2 with UPQC



Figure 3.22: Total harmonic distortion for load1cureent before harmonic compensation

3.4.2 Voltage harmonic compensation

the series APF is put into the operation. The series APF starts compensating voltage harmonics immediately by injecting sum of the harmonics, making load voltage at load1&load2 distortion free, as shown in Fig 25.c&Fig 26.c.Here load1 voltage THD is improved from 21.76% to 1.10%. This improved voltage at load1, load2 voltage THD is improved from 47.22% to 3.45% and improves source current THD value too. Here source1 voltage THD further reduced to 0.08% and
source2 voltage THD further reduced to 0.03%. The harmonic spectrums of voltage at load1 and current at source1 and when UPQC is ON, are shown in Fig 27 and Fig 28, respectively.



Figure 3.23: Vsource1, Vseries1, Vload1 Respectively Without UPQC



Figure 3.24: Vsource2, Vseries2, Vload2 Respectively Without UPQC



Figure 3.25: Vsource1, Vseries1, Vload1 Respectively With UPQC



Figure 3.26: Vsource2, Vseries2, Vload2 Respectively With UPQC







Figure 3.28: Total harmonic distortion for source1 current UPQC is ON

3.4.3 Current harmonic compensation

Both APF's are put into operation at different instant, shunt APF was put into operation first. After maintaining dc link voltage at set reference value as shown in Fig 31, the shunt APF starts compensating current harmonics as well as reactive current generated by non-linear load simultaneously. The current injected by shunt APF is nothing but the sum of harmonics current and reactive current. Before connected the UPQC the current at source1 is highly distorted as shown in Fig 29.a, the THD of current load1 is (36.45 %), after connected the UPQC it becomes sinusoidal and in phase with utility voltage with the use of shunt APF, as shown in the Fig 30.a . The THD of current source1 improved from 36.45 % to 4.54 %.



Figure 3.29: Isource1, Ish, Iload1 Respectively without UPQC



Figure 3.30: Isource1, Ish, Iload1 Respectively with UPQC



Figure 3.31: Vdc in compensation with UPQC

3.4.4 Voltage Events

Voltage sag compensation

The simulation results for voltage sag compensation are shown in the Fig 32.a the shunt APF is put into the operation. Series APF is put into operation. Now a sag (25%) is introduced on the system at time t=0.45 sec this sag lasted till time t=0.55 sec, as shown in the Fig 32.After time t=0.55 sec, the system is again at normal working condition. And after compensation The voltage wave becomes sinusoidal as shown in Fig 33.a. During this voltage sag condition, the series APF is providing the required voltage by injecting in phase compensating voltage (25%) equals to the difference between the reference load voltage and voltage at source, as shown in the Fig 32.b.The load voltage profile in the Fig 32.c shows that UPQC is maintaining it at desired constant voltage level at load bus. While series APF is providing the required real power to the load, the shunt APF is maintaining the dc link voltage at constant level such that the series APF can provide the needed real power to the load. In other words, the required load power is provided by the source only, by delivering more current. This extra power flows from source to shunt APF, shunt APF to series APF via dc link and from series APF to the load, but without any delay in the operation. Fig 31 shows there is slightly reduction in dc link voltage, whereas the load current profile in Fig 30.c shows that there is no effect of voltage sag on the loads since this current is always in steady state even during voltage sag on the load bus.



Figure 3.32: Vsource2 with sag, Vseries2, Vload2 Respectively with UPQC



Figure 3.33: Vsource2 with sag, Vseries2, Vload2 after compensation

Voltage swell compensation

A swell (25%) is now introduced on the system during the time t=0.45 sec to t=0.55 sec, as shown in the Fig 34. a. Under this condition the series APF injects an out of phase. Compensating voltage (25%) in the line through series transformers, equal to the difference between the reference load voltage and voltage at source, as shown in the Fig 32.b.after compensation The voltage wave becomes sinusoidal as shown in Fig 35.aThe load voltage profile in the Fig 35.c shows the UPQC is effectively maintaining the load bus voltage at desired constant level. The UPQC controller acts in such a way that source delivers the reduced current. In other words, the extra power due to the voltage swell condition is fed back to the source by taking reduced fundamental source current. The shunt APF maintains the dc link voltage at almost constant level, slightly increases due to the swell on the system as shown in Fig 31.



Figure 3.34: Vsource2 with swell, Vseries2, Vload2 Respectively with UPQC



Figure 3.35: Vsource2 with swell, Vseries2, Vload2 after compensation

THD Results

In chapter tow It had been shown how to calculate THD. However, MATLAB SIMULINK provides the Fourier transform and calculate the THD in the proposed model of UPQC the THD is given before and after compensation for the V source 1 as shown in figures 3.36 & 3.37 respectively



Figure 3.36: Vsource1 before harmonic compensation



Figure 3.37: Vsource1 after harmonic compensation





Figure 3.38: V source 2 before harmonic compensation



Figure 3.39: Vsource1 after harmonic compensation





Figure 3.40: Vload1 before harmonic compensation



Figure 3.41: Vloda1 after harmonic compensation





Figure 3.42: Vload2 before harmonic compensation



Figure 3.43: Vload2 after harmonic compensation

Chapter 4

Conclusion & Recommendation

4.1 Conclusion

The performance of UPQC with the proposed loads has been evaluated. Running linear and nonlinear loads with existence of unified power quality conditioner using MATLAB SIMULINK has been carried out to show its impact and controller's operation based on state space model in each case. The simulation results for current harmonics compensation, voltage harmonics compensation, voltage sag & swell compensations are given. These simulation results show the controller is operating effectively giving improved results (see figures in the previous chapter). It can be noticed that the THD has been enhanced in each situation, Voltage sag & swell are compensated during the period 0.45-0.55.

4.2 Recommendation

• Fact devices is the recent trend of recent factories, so it's recommended to work in developing these devices.

• Plan to enhance the shunt converter by using four legs (8 IGBT) transistors, the fourth leg is used in order to eliminate harmonic current in the neutral line that gives better result and less harmonic distortion in the signal.

• The state space model is the convenient way for building the control algorithm because it simpli-

fies the control process in a single phase dynamic circuit.

• It's recommended that to equip UPQC in the point of common coupling of grid with solar plant source that has PV systems because it injects a lot of harmonic to the grid and this can be solved by UPQC.

Bibliography

- "Flexible AC Transmission System(FACTS)", Electronics Hub, 2019. [Online]. Available: https://www.electronicshub.org/flexible-ac-transmission-systemfacts/. [Accessed: 22-Nov- 2019].
- [2] Sindhu S., M. Sindhu and T. Nambiar, "An Exponential Composition Algorithm Based UPQC for Power Quality Enhancement", Procedia Technology, vol. 21, pp. 415-422, 2015. Available: 10.1016/j.protcy.2015.10.062.
- [3] Y. Pal, A. Swarup and B. Singh, "A Novel Control Strategy of Three-phase, Four-wire UPQC for Power Quality Improvement", Journal of Electrical Engineering and Technology, vol. 7, no. 1, pp. 1-8, 2012. Available: 10.5370/jeet.2012.7.1.1.
- [4] R. Dharmalingam, S. Dash, K. Senthilnathan, A. Mayilvaganan and S. Chinnamuthu, "Power Quality Improvement by Unified Power Quality Conditioner Based on CSC Topology Using Synchronous Reference Frame Theory", The Scientific World Journal, vol. 2014, pp. 1-7, 2014. Available: 10.1155/2014/391975.
- [5] C. Benachaiba, O. Abdelkhalek, S. Dib, M. Allali and D. Dib, "The Unified Power Quality Conditioner (UPQC): The Principle, Control and Application", Journal of Electrical Engineering & Technology, vol. 1, no. 4, pp. 503 512, 2002. Available: 10.1109/PCC.2002.998518 [Accessed 12 November 2019].
- [6] V. Khadkikar, A. Chandra, A. Barry and T. Nguyen, "Power quality enhancement utilising single-phase unified power quality conditioner: digital signal processor-based experimental validation", IET Power Electronics, vol. 4, no. 3, p. 323, 2011. Available: 10.1049/ietpel.2010.0031.

- [7] Y. Pal, A. Swarup and B. Singh, "Applications of UPQC for Power Quality Improvement", IEEE Transactions On Power Systems conference, 2010. [Accessed 8 October 2019].
- [8] Y. Pal, A. Swarup and B. Singh, "A Novel Control Strategy of Three-phase, Four-wire UPQC for Power Quality Improvement", Journal of Electrical Engineering and Technology, vol. 7, no. 1, pp. 1-8, 2012. Available: 10.5370/jeet.2012.7.1.1.
- [9] Multi Converter Based Power Quality Improvement in Renewable Energy System Using UPQC Compensator - Scientific Figure on ResearchGate. Available from: https://www.researchgate.net/figure/Block-Diagram-of-UPQC-connected-in-series-with-theline-using-series-transformers-acts-fig1-282332145 [accessed 7 Oct, 2019]
- [10] Modeling of six pulse voltage source inverter based statcom with PWM and conventional triggering - Scientific Figure on ResearchGate. Available from: https://www.researchgate.net/figure/Block-diagram-of-VSI-connected-to-3-Phase-load-fig1-320141990 [accessed 8 Oct, 2019]
- [11] S. Sharma, A. Pandey and N. Saxena, "Modeling of Six Pulse Voltage Source Inverter based STATCOM with PWM and Conventional Triggering", Indonesian Journal of Electrical Engineering and Informatics (IJEEI), vol. 5, no. 2, 2017. Available: 10.11591/ijeei.v5i2.271.
- [12] Q. Trinh and H. Lee, "Improvement of unified power quality conditioner performance with enhanced resonant control strategy", IET Generation, Transmission & Distribution, vol. 8, no.
 12, pp. 2114-2123, 2014. Available: 10.1049/iet-gtd.2013.0636.
- [13] "Low Pass Filter- Explained", Learningaboutelectronics.com, 2019. [Online]. Available: http://www.learningaboutelectronics.com/Articles/Low-pass-filter.php. [Accessed: 08- Oct-2019].
- [14] 2019. [Online]. Available:https://www.electronics-tutorials.ws/filter/filter_5.html. [Accessed: 08- Oct- 2019].
- [15] Electrocube.com, 2019. [Online]. Available: https://www.electrocube.com/documents/DC_ Link_ Tech_ Bulletin_ vF_ 092816.pdf. [Accessed: 09- Oct- 2019].

- [16] Microsemi.com, 2019. [Online]. Available: https://www.microsemi.com/documentportal/doc_view/132799-park-inverse-park-and-clarke-inverse-clarke-transformations-msssoftware-implementation-user-guide. [Accessed: 22- Nov- 2019].
- [17] K. Kwan, P. So and Y. Chu, "An Output Regulation-Based Unified Power Quality Conditioner With Kalman Filters", IEEE Transactions on Industrial Electronics, vol. 59, no. 11, pp. 4248-4262, 2012. Available: 10.1109/tie.2012.2193852.
- [18] Bhardwaj, M. and Gupta, A. (2014). Design and Implementation of UPQC to Solve Power Quality Problems. International Journal of Engineering and Technical Research (IJETR), 2(10), pp.2321-0869.
- [19] N. Khan and M. Shakeel, "Design of a Unified Power Quality Conditioner (UPQC)", International Journal of Science and Engineering Investigations, vol. 5, no. 59, 2016. [Accessed 22 November 2015].
- [20] G. Accetta, G. D'Antona, D. Della Giustina and R. Faranda, "Power Quality improvement in LV smart grid by using the Open UPQC device", Renewable Energy and Power Quality Journal, pp. 540-545, 2013. Available: 10.24084/repqj11.363.
- [21] V. Khadkikar, A. Chandra, O. Barry and T. Nguyen, "Application of UPQC to Protect a Sensitive Load on a Polluted Distribution Network", IEEE, vol. 3, no. 10, p. 6, 2006.
- [22] "Multilevel UPQC Fed Grid Connected Hybrid System for Sag and Swell Mitigation", International Journal of Recent Technology and Engineering, vol. 8, no. 211, pp. 2452-2458, 2019. Available: 10.35940/ijrte.b1287.0982s1119.
- [23] V. Khadkikar, A. Chandra, A. Barry, and T. Nguyen, "Application of UPQC to protect a sensitive load on a polluted distribution network," 2006 IEEE Power Engineering Society General Meeting, 2006.
- [24] e. notes, "PLL Phase Locked Loop: How it Works Electronics Notes", Electronics-notes.com, 2020. [Online]. Available: https://www.electronics-notes.com/articles/radio/pll-phase-lockedloop/tutorial-primer-basics.php. [Accessed: 25- Apr- 2020].
- [25] Gairoux, P. and Sybille, G., 2007. 3-Phase PLL. Power System Laboratory: IREQ Hydro-Quebec.

- [26] "Parallel Side Research of UPQC Based on RBF Neural Network-Tuning PID Control-East China Electric Power 2013 03", En.cnki.com.cn, 2020. [Online]. Available: http://en.cnki.com.cn/Article_en/CJFDTotalHDDL201303047.htm. [Accessed: 25- Apr- 2020].
- [27] Gairoux, P. and Sybille, G. PWM Generator. Power System Laboratory: IREQ Hydro-Quebec.

Appendix A

Matlab code

str = sprint f('Fo = Wo =2 * pi * Fo;*switchFilterType* case1,%Lowpass X = [01234];Y = [-2 - 2 - 3 - 4 - 4];n2 = 0; n1 = 0; n0 = Wo *Wo; d2 = 1; d1 = 2 * Zeta *Wo; d0 = Wo * Wo;Ystep = 1;case2,%Highpass X = [01234];Y = [-4 - 4 - 3 - 2 - 2];n2 = 1; n1 = 0; n0 = 0;d2 = 1; d1 = 2 * Zeta *Wo; d0 = Wo * Wo;Ystep = 2;case3, %Band pass X = [012345];

Y = [-3 - 3 - 2 - 2 - 3 - 3];n2 = 0; n1 = 2 * Zeta *Wo; n0 = 0;d2 = 1; d1 = 2 * Zeta *Wo; d0 = Wo * Wo;Ystep = 3;*case*4,%*Bandstop*(*Notch*) X = [012345];Y = [-2 - 2 - 3 - 3 - 2 - 2];n2 = 1; n1 = 0; n0 = Wo *Wo; d2 = 1; d1 = 2 * Zeta *Wo; d0 = Wo * Wo;Ystep = 4;end % numc = [n2n1n0];denc = [d2d1d0];

tf2ss(numc,denc);%Conversiontodiscr nstates = size(Ac, 1);invexp = inv(eve(nstates) -(Ts/2) * Ac);Ad = invexp * (eve(nstates) +(Ts/2) * Ac);Bd = invexp * Bc;Cd = Cc * invexp * Ts;Dd = Cc * invexp * Bc *(Ts/2) + Dc;%ifInitialize == 1%Computeinitial conditions and the second seco $u1 = Vac_Init(1) * exp(j *$ $Vac_{I}nit(2) * pi/180);$ $u2 = Vdc_Init * exp(j * 90 *$ pi/180);u = u1 + u2;u0 = imag(u);%inputatt =0; I = eye(size(Ac));

=

[Ac, Bc, Cc, Dc]

$$\begin{split} sl1 &= l * j * (2 * pi * wn^2)^{(1/2)} * exp((-z*wn wn.*w*j; \\ Vac_nin(3)); &+ 1/2 * (4 * z^2 * wn^2 - 4 * case4, %Bandstop(Notch) \\ sl2 &= l * j * 0; &wn^2)^{(1/2)} * t) - 1/(- Ystep &= 1 + 2 * z/wn * \\ x &= inv(sl1 - Ac) * Bc * u1 + z * wn - 1/2 * (4 * z^2 * wn^2 - exp(-z * wn * t)/(z - 1)/(z \\ inv(sl2 - Ac) * Bc * u2; & 4 * wn^2)^{(1/2)} * exp((- + 1) * (wn^2 - z^2 * x0) \\ x0c &= imag(x); & z * wn - 1/2 * (4 * z^2 * wn^2 - wn^2)^{(1/2)} * sin((-wn^2 * x0) \\ x0d &= (l - Ac * Ts/2) * & 4 * wn^2)^{(1/2)} * t); \\ else & case2, %Highpass & numFreq &= wn^2 + x0 \\ end & t)/(z - 1)/(z + 1) * cos((- \% \\ \% & wn^2 * (z - 1) * (z + 1))^{(1/2)} * t); \\ else & case2, (Highpass & numFreq &= (wn^2 - w.^2) + 2 * ifPlotResponse &= t) + exp(-z * wn * t)/(z - Zeta * wn * j * w; \\ 1\%Plot frequencyandstepresponsd)/(z & RepFreq = (wn^2 - w.^2) + 2 * ifPlotResponse &= t) + exp(-z * wn * t)/(z - Zeta * wn * j * w; \\ 1\%Plot frequencyandstepresponsd)/(z & RepFreq = nunFreq./denFreq; ifZeta == 1 & +1) * z^2 * cos((-wn^2 * (z - Mag = abs(RepFreq); z = 1 + 1e - 12; 1) * (z + 1))^{(1/2)} * t) + z/ Pha = angle(RepFreq) * else & wn * exp(-z * wn * t)/(z - 180/pi; z = Zeta; 1)/(z + 1) * (wn^2 - \% \\ end & z^2 * wn^2)^{(1/2)} * t = y + wn^2 (z - 1) * (z + subplot(2, 1, 1)) \\ t = [0 : 1/(z * wn)/1000 : 1))^{(1/2)} * t); & plot(f, Mag) \\ 7/(z * wn)]; & numFreq = -w^2; & grid \\ f = param1(1) : case3, %Bandpass & title('BodeDiagram') \\ yaaram1(3) : param1(2); & Ystep = 2 * z * wn/ ylabel('Magnitude') \\ w = 2 * pi * f; & (4 * z^2 * wn^2 - 4 * subplot(2, 1, 2) \\ switchFilterType & wn^2)^{(1/2)} * (1/2) * (cxp((-z * wn plot(f, Pha) \\ case1, %Lowpass & + 1/2 * (4 * z^2 * wn^2 - 4 * ylabel('Phase(deg)') \\ Ystep = wn^2 * (1/wn^2 + 1/ wn^2)^{(1/2)} * t) - exp((- xidet) + idet)'Frequency(Hz)') \\ (4 * z^2 * wn^2 - 4 * z * wn - 1/2 * (4 * z^2 * grid \\ wn^2)^{(1/2)} * (1/(-z * wn wn^2 - 4 * wn^2)^{(1/2)}) * figure(2) \\ + 1/2 * (4 * z^2 * wn^2 - 4 * t)); numFreq = 2 * Zeta * plot(t, real(Ystep)) \\ \end{cases}$$

*

grid ylabel('Amplitude') xlabel('Time(s)') title('StepResponse') end power_initmask();