Palestine Polytechnic University
College of Applied Science

Prayer Electronic Calendar

Graduation Project

Prepared By :-

Abed AL-Rahman AL-Sharabaty
Mohammad ALqurnh
Nidal Idaiss

Supervisor:
Dr. Ra'ed Amro

27-5-2007

Prayer Electronic Calendar

Prepared By

Abed AL-Rahman AL-Sharabaty
Mohammad ALqurnh
Nidal Idaiss

Supervisor:
Dr. Ra'ed Amro

Graduation Project

Presented to Applied Electronics in the College of Applied Sciences

Palestine Polytechnic University

As a requirements for the Degree of Bachelors in Science in Applied Electronics

Palestine Polytechnic University
2007

Palestine Polytechnic University
Hebron – Palestine

Prayer Electronic Calendar

Prepared By

Abed AL-Rahman AL-Sharabaty
Mohammad ALqurnh
Nidal Idaiss

According to the instructions of the supervisors of this project and the acceptance of the members of the examining committee, the project is submitted to the department of applied electronics in applied science as partial full fillment for the bachelor degree.

Chief of the Department Signature

Name:.....

Supervisor Signature

Name:.....

27-5-2007
Dedication

Electronic Prayer Calendar

Prepared By

Abed AL-Rahman AL-Sharabaty
Mohammad ALqurnh
Nidal Idaiss

Supervisor:
Dr. Ra'ed Amro

Palestine Polytechnic University-2007

Abstract

This project is very useful to Muslims, since the prayer is the most important thing in our religion, and its importance to announce for praying at the accurate time .Our project displays the real time along with and the time of the announcing for the five prayers along the year , and when the real time becomes equal of any prayer time ,the athan will work .

ملخص المشروع

هذا المشروع عبارة عن مؤقته صلاة الكترونية تعرض الوقت الحقيقي للساعة بالإضافة لعرض أوقات الصلاة الخمسة وبشكل دوري على مدار السنة, وعند حلول موعد الأذان لأي صلاة فإنها تقوم بالأذان.

Table of Contents:-

Chapter One "Introduction"

Chapter Two "Project Component"

Chapter Three "Project System"

Chapter Four "Practical Realization"

List of Figures

List of Table

Chapter One

Introduction

Chapter One

Introduction

Motivation

Digital timing alarm has several and important applications in the nowadays technological life. It has the advantage of accuracy and flexibility.

The accurate execution of ALathan (pray - time) is of religious importance. However, and due to human error this is not always achieved. Furthermore, the increasing number of mosques makes the synchronization process of ALathan necessary, This would satisfy the Islam demand to displine.

1.1 Importance of the Project

This project which we called " prayer electronic calendar" is very useful to us as Muslims, because the prayer is the most important thing in our religion, and it's importance to announce for prayers at the accurate time. Also, this system of storing , controlling and displaying data could be used and applied for other purposes such as the timing of lectures in the university.

1.2 Main Idea of the Project

The general idea of the project is to store the time of prayer in a storage unit and uses the microprocessor to read this time and display it at a seven segment after comparing it with the real date and real time. The next step is to determine- by the comparing programs- the exact time of the prayer, then work on the interruption of the ALathan devices.

1.3 Literature Review

The idea of using the announcement system was applied in many countries and in some cities in Palestine. But this system was based on the principle of connecting all mosques of the city to one athan by using the wire system ,If our project is applied in the mosque, we can perform the announcement in the city at the accurate time.

During our preparation for this project, we found a project with similar idea. However, this project (Digital Muezzin) was presented in August-2003. For more details see [1].

To achieve this purpose, certain computer programs can be used to calculate the time of prayer by determining the position of the city , the month and date, and enter it using specific equations. But, this program is designed to deal with computers.

1.4 Main Parts of the Project

The project is divided into two main parts. The first one is the hardware part and its elements, This part includes the selection of suitable integrated chips (ICs) for the project and connecting them in one circuit. The second part is the programming of the system which will execute all the goals of this project.

1.5 Cost of the Project

Table 1.1 : Cost of the Project

Parts	Quantity	Price (NIS)
8085	1	15
DS1643	1	40

Resistance	170	34
IC 74373	28	70
IC 7447	2	12
1C4514	1	2
IC 74138	2	6
7-Segment Display	24	276
Board	80cm	75
Wire	25m	20
Capacitors	30	15
EPROM27C128	1	30
Optocouplers	2	6
J-K Flip Flop	2	6
Total		700 (NIS)

1.6 Project Contents

The report contains four chapters: In chapter one we give a general outlook about the project and its importance. In chapter two, we talk about the system model by using the block diagrams, figures and discussing the main idea of the principle. In chapter three, we discuss the operating system and the flowcharts of the project program. Chapter four , contains the practical realization of the project.

Chapter Two

Project Components

Chapter Two

Project Components

2.1 Project Components

Our Project will display the pray times at seven segments and play the athan at its time. To built the project, we need special components including the following :-

- ✓ Power Supply
- ✓ Microprocessor (8085)
- ✓ Dallas real time clock (DS1643)
- ✓ EPROM (27C128).
- ✓ IC74138 (Decoder)
- ✓ IC7447 (Decoder)
- ✓ IC 4514(Decoder)
- ✓ IC74373 (Latch)
- ✓ Seven Segment
- ✓ Resistance
- ✓ Capacitors
- ✓ Sound Storage unit
- ✓ Optocouplers
- ✓ J-K Flip Flop
- ✓ Relay

2.2 General Block Diagram:

As we mentioned in the previous chapter, the project is consisted of two parts, hardware and software. The hardware system will be discussed in this part by using the block diagrams.

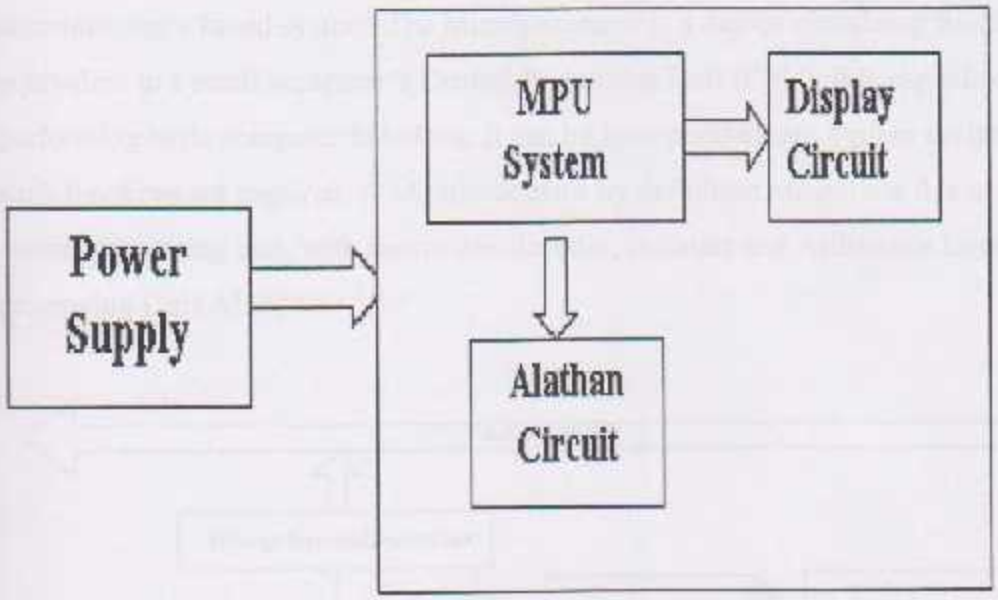


Figure 2.1: General Block Diagram

2.3 First part (Power Supply)

There are many types of power supply. Most are designed to convert high voltage AC main electricity to a suitable low voltage supply for electronic circuits and other devices. For our system model we need a 5VDC power supply.

2.4 Second Part (Microprocessors System)

Microprocessors are widely used as controlling components in all kinds of instruments. In this cases the microprocessor with its peripheral extensions is the most responsible component for the functionality of the project. If the microprocessor fails, the complete instrument will fail.

Therefore, it is very important to understand the major blocks inside the microprocessor based system. The Microprocessor is a device containing functions equivalent to a small computer's Central Processing Unit (CPU). It is capable of performing basic computer functions. It can be incorporated into system designs where such functions are required. A Microprocessor by definition means that this is only the central processing unit, with instruction decoder, registers and Arithmetic Logic processing Unit(ALU).

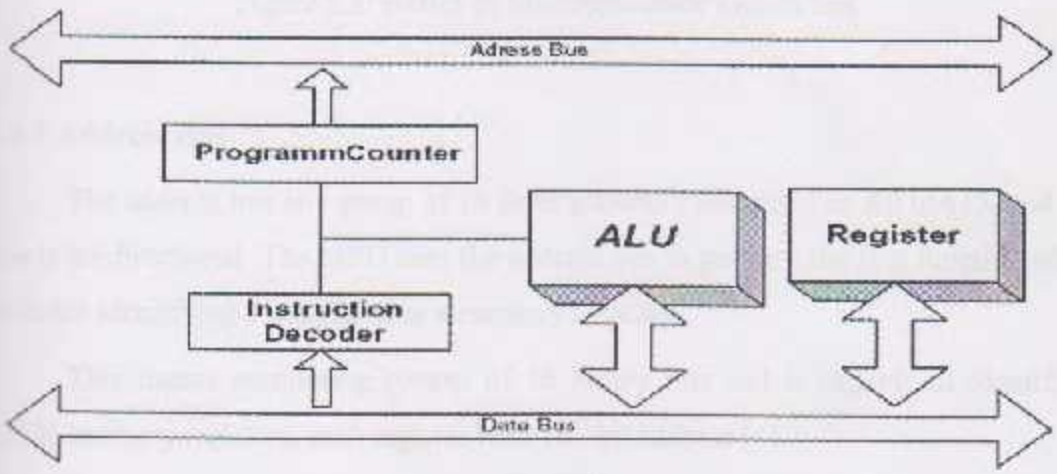


Figure 2.2: Block Diagram of Microprocessor System

The 8085 MPU performs the operation using three sets of communicating lines. They are: the address bus, the data bus, and the control bus, These buses are shown as groups in the figure 2.3.

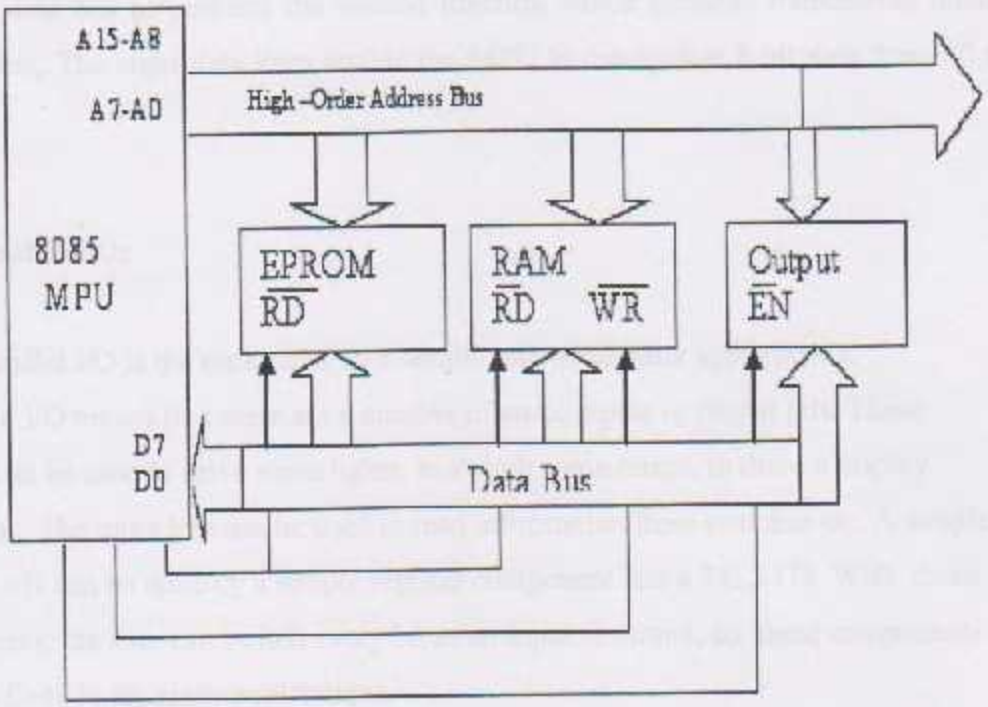


Figure 2.3: Basics of Microprocessor system bus

2.4.1 Address Bus

The address bus is a group of 16 lines generally identified as A0 toA15, and this bus is unidirectional .The MPU uses the address bus to perform the first function which includes identifying a peripheral or a memory location.

This means numbering system of 16 binary bits and is capable of identifying 65536 memory registers, each register with 16 –bit address [4].

2.4.2 Data Bus

The data bus is a group of eight lines used for data flow. These lines are bidirectional data flow between the MPU, memory and peripheral device. The MPU uses the data bus to perform the second function which includes transferring binary information, The eight data lines enable the MPU to manipulate 8-bit data from 00 to FF.

2.4.3 Parallel I/O:

Parallel I/O is the most used in a simple microcomputer applications. A parallel I/O means that there are a number of static inputs or output bits. These outputs can be used to drive some lights, to switch some relays, to drive a display And so on. The input bits can be used to read information from switches etc. A simple parallel I/O can be done by a simple register component like a 74LS373. With these components, the user can switch every bit as an input or output, so, these components are very flexible for many applications.

In this type of I/O mapping the MPU used eight address lines to identify an I/O device, which is known as peripheral-mapping. The 8-address lines can have 256 addresses; thus the MPU can identify 256 input devices and 256 output devices. [4]

2.4.4 The Memory

Every microprocessor system needs a memory block. In general, there are two types of memory:

* Program memory.
* Data memory.

Program memory is used to hold the application of the program. This must have a memory which doesn't lose its information when the power is shut down. At power up,

the CPU begins to read the instructions from this memory. In most microprocessor applications, the program memory is a READ ONLY MEMORY (ROM). There are different types of ROM available. The most used one is the Electrically Programmable ROM (EPROM). This chip could be programmed with a special programmer and could be erased by applying ultra-violet light.

Data memory is used for the dynamic data which is generated by the application program and for the STACK. The stack is a portion of memory where the CPU saves its own internal registered data for calling a subroutine

2.4.5 The Mapping of the Project

In our project we need to use three kinds of memory. The EPROM to store the program and pray times. We need two registers to store one time of ALathan which means that we need to use 3650 register to store time of Alathan for the five times of prayer along the year. Also we want to use the DS1643 as an 8K x 8 nonvolatile static RAM with a full function Real Time Clock, because it has an internal real time clock which called Dallas. So the address of the memory will be:

1-EPROM address

The EPROM is a 8k memory chip that requires 13 address lines from A12 to A0; therefore only three high –order address lines (A15, A14, A13) must be decoded. To assign the starting address, 0000H, the logic levels of A15-A13 should be zero. By using the output O0 of the decoder to select the EPROM memory chip, address lines A15-A14 must be at logic 0 . The address range of the EPROM is as follows:

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	=0000H
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	=1FFFH

2-The RAM Address

The 8K RAM requires 13 address lines from A12 to A0, and the memory chip will be selected by the output O1 of the decoder.

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The address range will be from 2000H to 3FFFH, and the table2 is for the address of the real time registers.

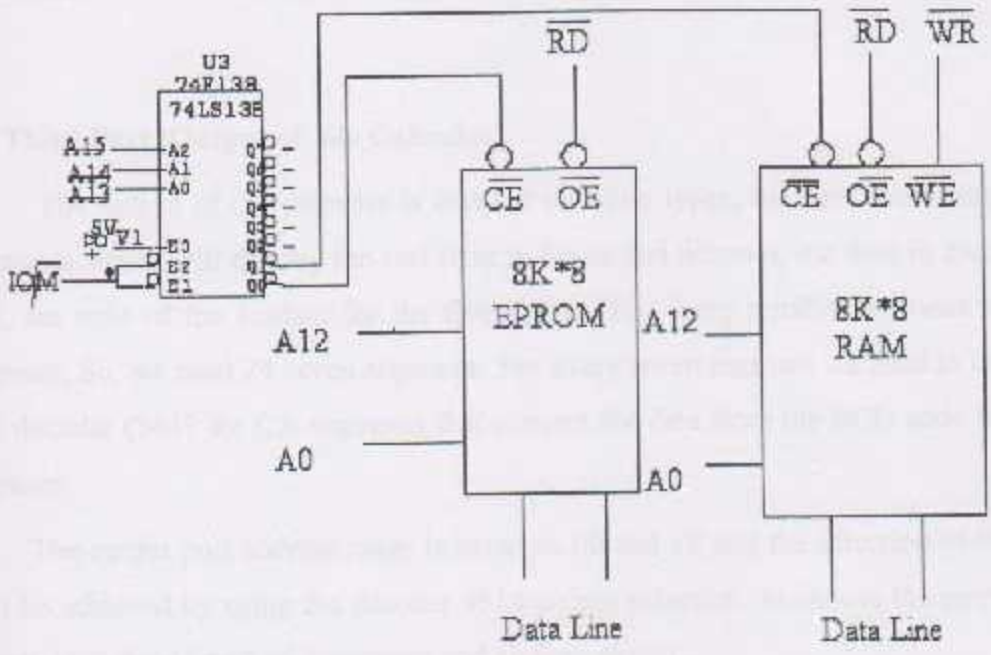


Figure 2.4: Block Diagram of the Mapping

The real time clock information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and second's data in 24-hour BCD format.

Table 2.1: Address of The Real Time

ADDRESS	DATA								FUNCTION	RANGE
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
3FFF	—	—	—	—	—	—	—	—	Year	00-99
3FFE	X	X	X	—	—	—	—	—	Month	01-12
3FFD	X	X	—	—	—	—	—	—	Date	01-31
3FFC	X	FT	X	X	X	—	—	—	Day	01-07
3FFB	X	X	—	—	—	—	—	—	Hour	00-23
3FFA	X	—	—	—	—	—	—	—	Minutes	00-59
3FF9	$\overline{OSC}$	—	—	—	—	—	—	—	Seconds	00-59
3FF8	W	R	X	X	X	X	X	X	Control	A

$\overline{OSC}$ = STOP BIT R = READ BIT FT = FREQUENCY TEST
W = WRITE BIT X = UNUSED

2.5 Third Part (Output of the Calendar)

The output of the calendar is divided into two types; the first one is the seven segments which will display the real time in hours and minutes, the date in month and day, the time of the alathan for the five prayer. For every number we need a seven segment, So, we need 24 seven segments. For every seven segment we need to use latch and decoder (7447 for CA segment) that convert the data from the BCD code to seven segment.

The output port address range is between 00 and FF and the selection of the port will be achieved by using the decoder 4514 output selection to choose the output port which includes 15 port of 7-segmant and alathan circuit .

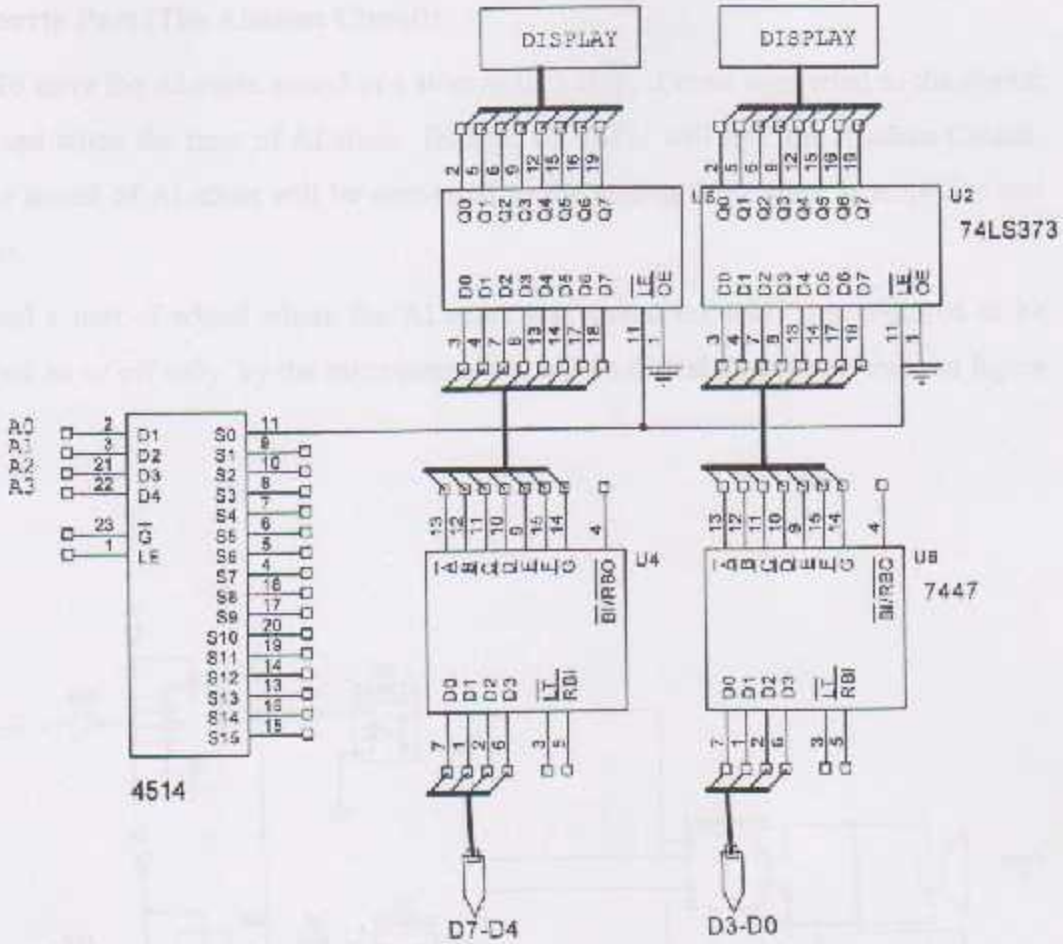


Figure 2.5: The Output Ports with 4514 Decoder

The input lines of the decoder were connected to the low address lines A0-A3 and its output (O0-O13) were connected to the enable of the segments latches. So, every two segments will dial as one port. The output lines selection O14,O15 were used to enable the ALathan circuits.

2.6 Fourth Part (The Alathan Circuit)

To store the ALathan sound in a storage unit chip, it must converted to the digital form, and when the time of ALathan fetches, the MPU will INT the Alathan Circuit, and the sound of ALathan will be converted to the analog form, then to amplifier and speaker.

We used a unit of sound where the ALathan was stored on, and it is required to be switched on or off only by the microprocessor with a digital circuit as shown in figure 2.6 .

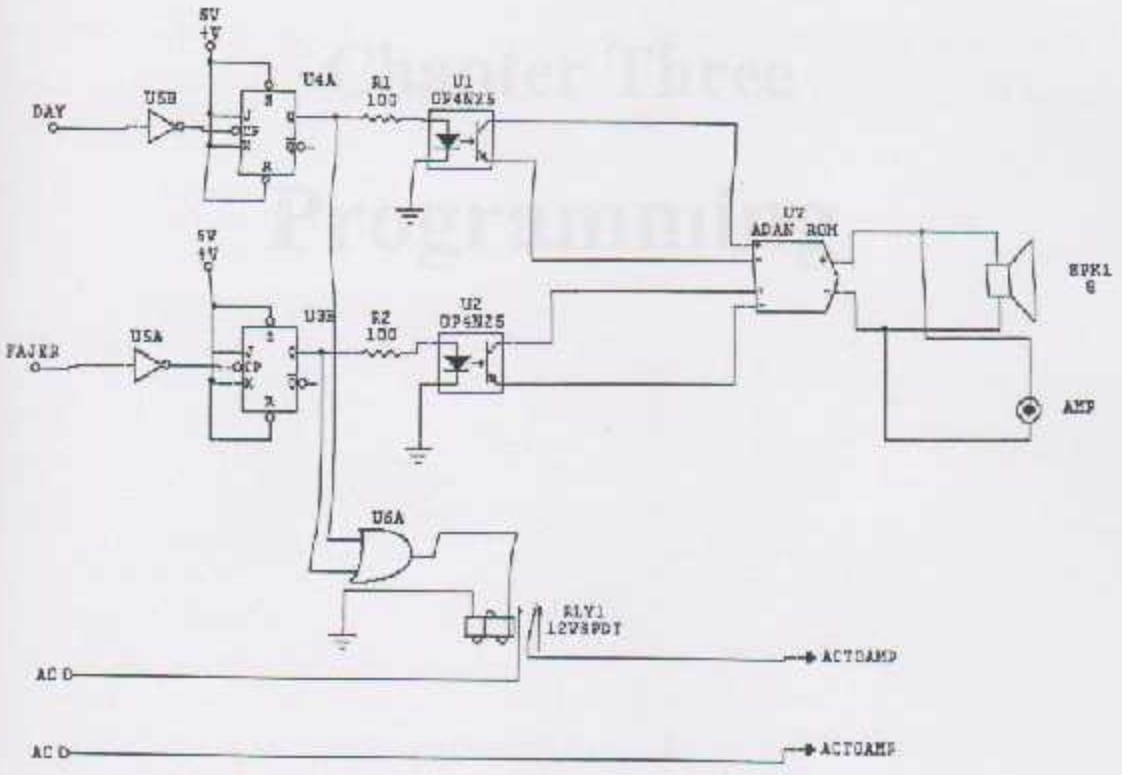


Figure 2.6: The ALathan Circuit

Chapter Three

Programming

Chapter Three
Programming

3.1 Project Operating System

The system of our calendar is very simple. The 8085 MPU will execute the program instructions, which include reading the real date time from the Dallas clock. Then, it reads the time of alathan of that date from the memory and display it. The time of hour in the Dallas and EPROM is in the 24-H system, so the program will convert it to 12-H system (AM& PM). Then, it displays it at the seven segments. After that it reads the real time from the Dallas clock, and compares it with the time of AL-Athan of that date which is stored in the EPROM. If the match occurs, it will interrupt the AL-athan circuit to play.

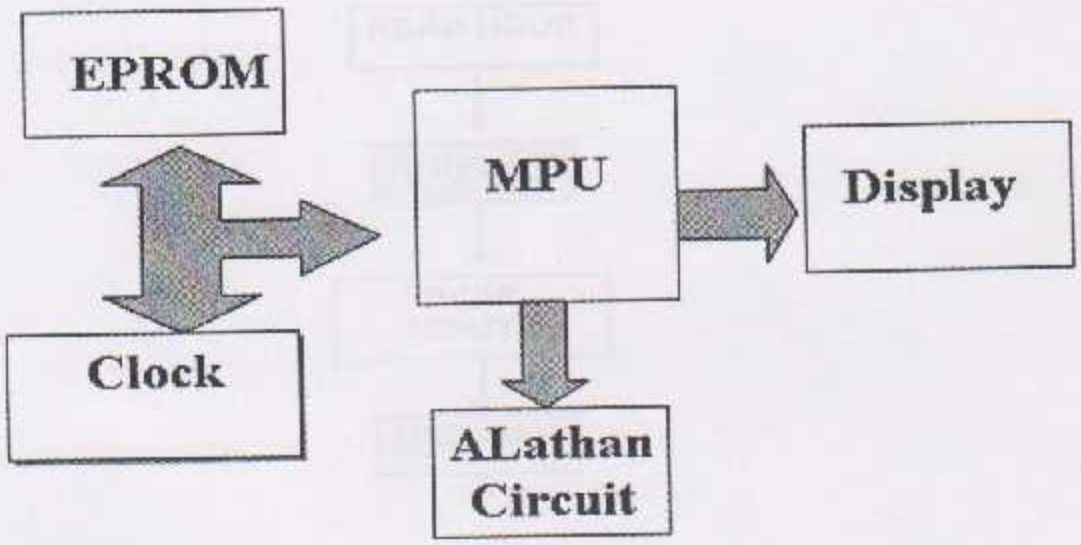


Figure 3.1 : Project System

3.2 Flowchart for the Project Program

3.2.1 Displaying the Real Time

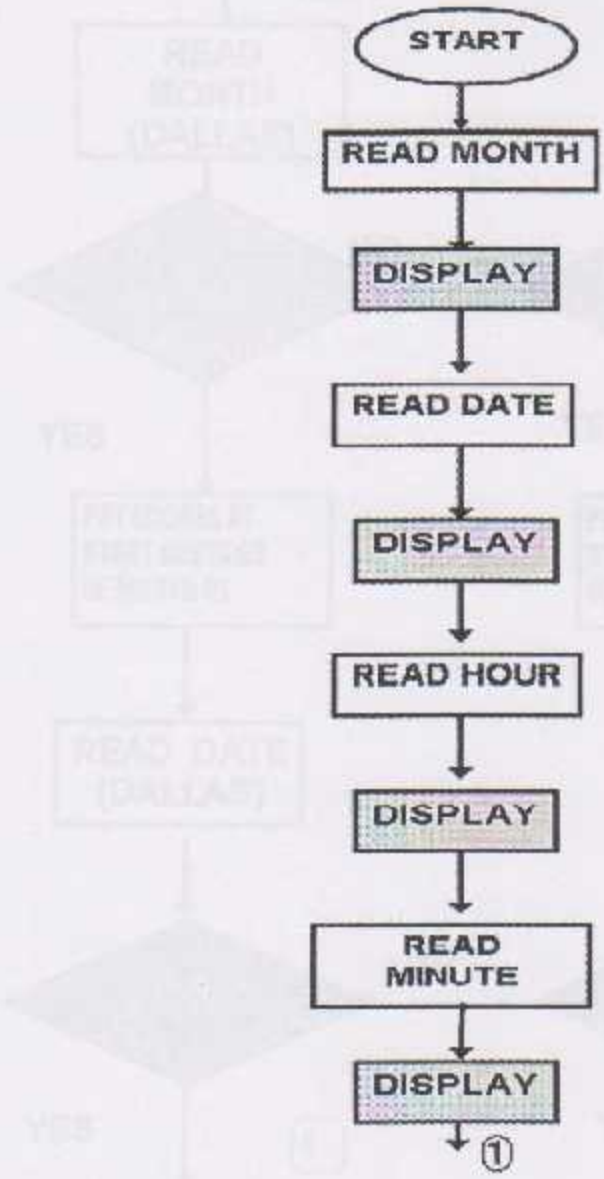


Figure 3.2: Displaying the Real Time

3.2.2 Determining the Start Address of Month

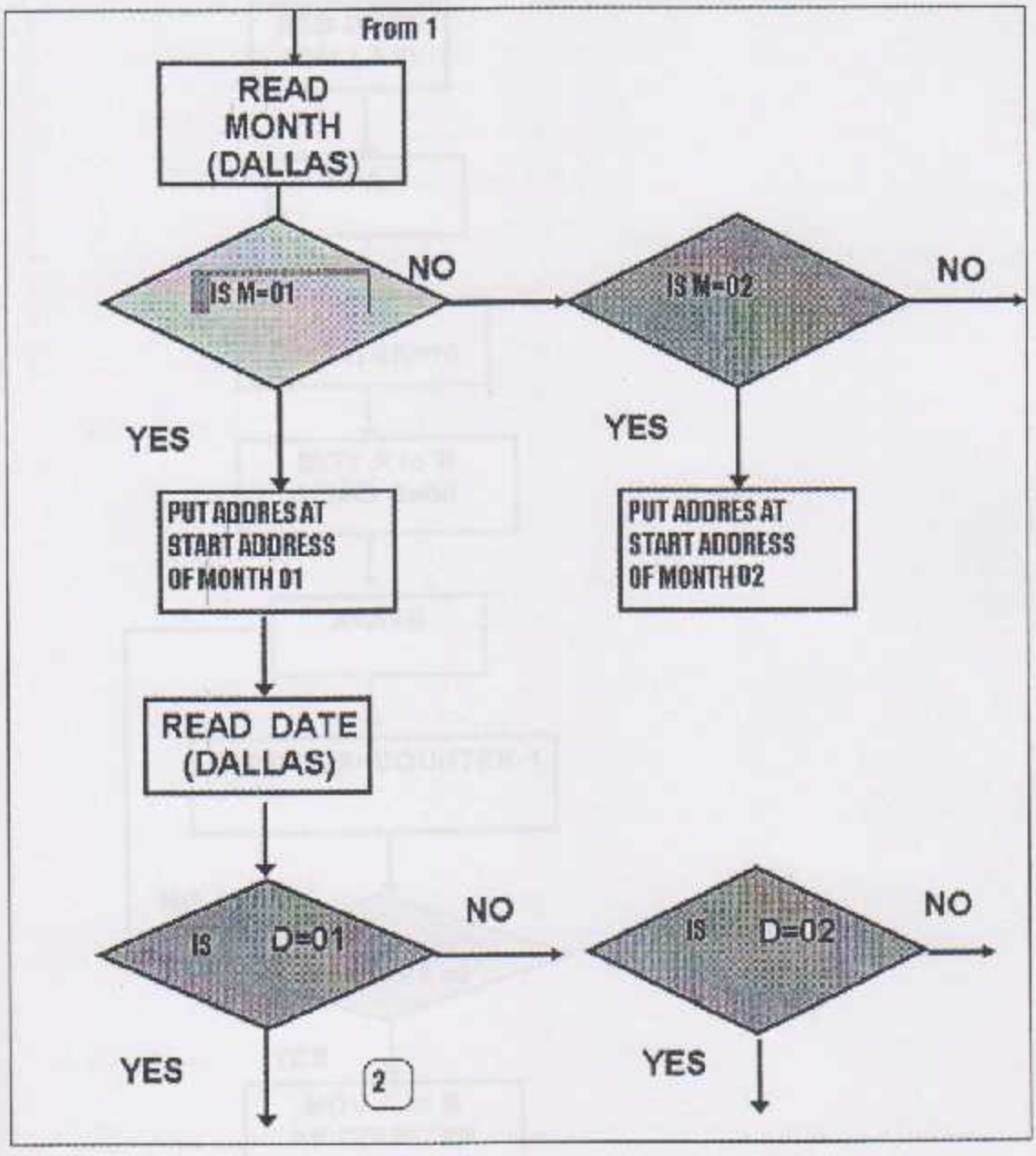


Figure 3.3: Determining the Start Address of Month

3.2.3 Determine the Start Address of Day

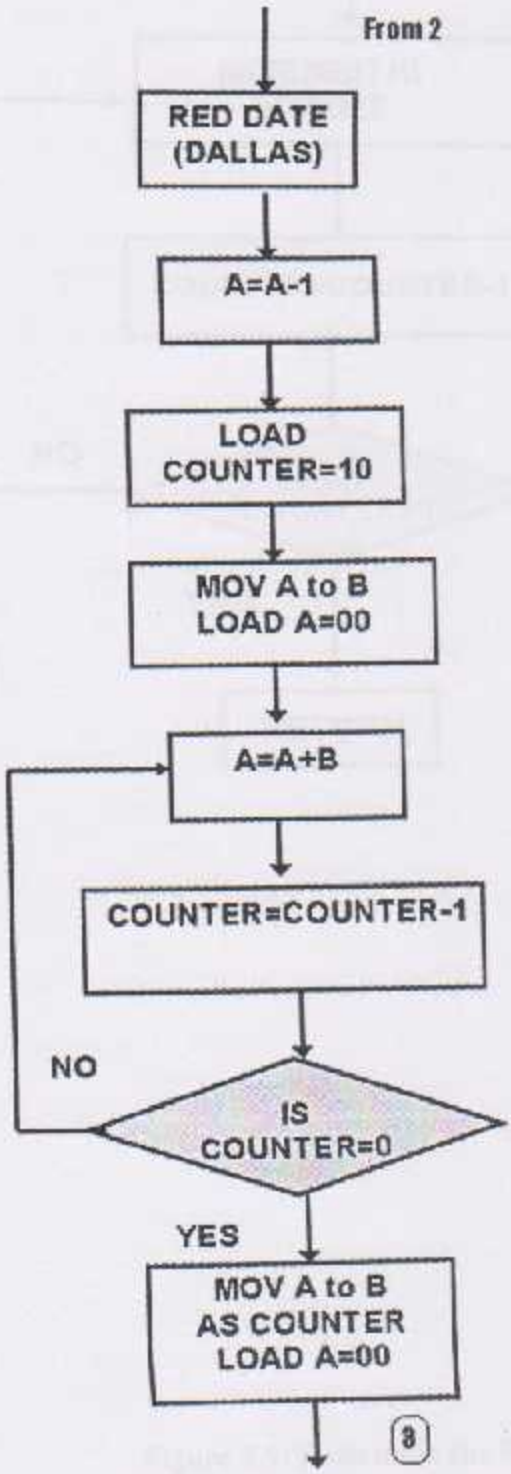


Figure 3.4: Determine the Start Address of Day

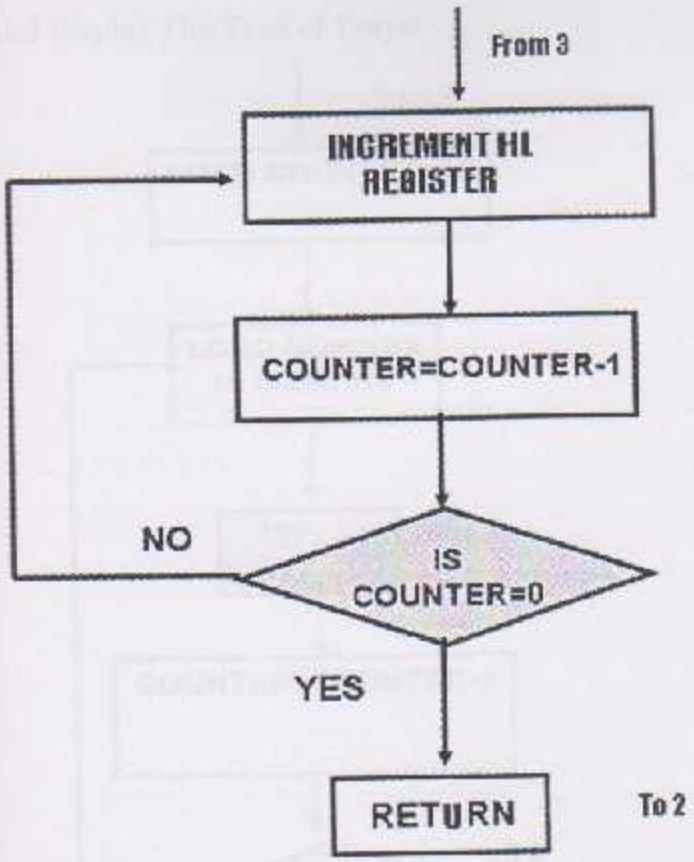


Figure 3.5: Determine the Start Address of Day

3.2.3 Display The Time of Prayer

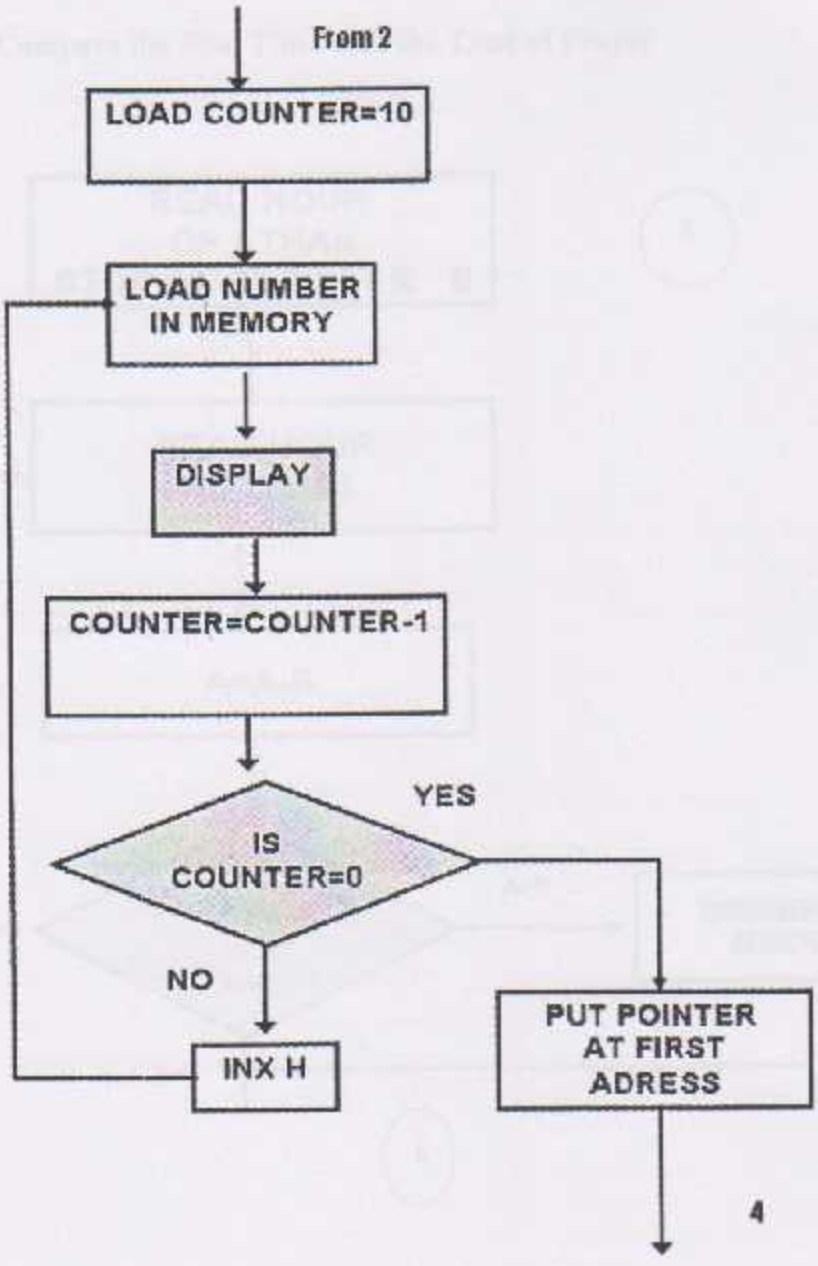
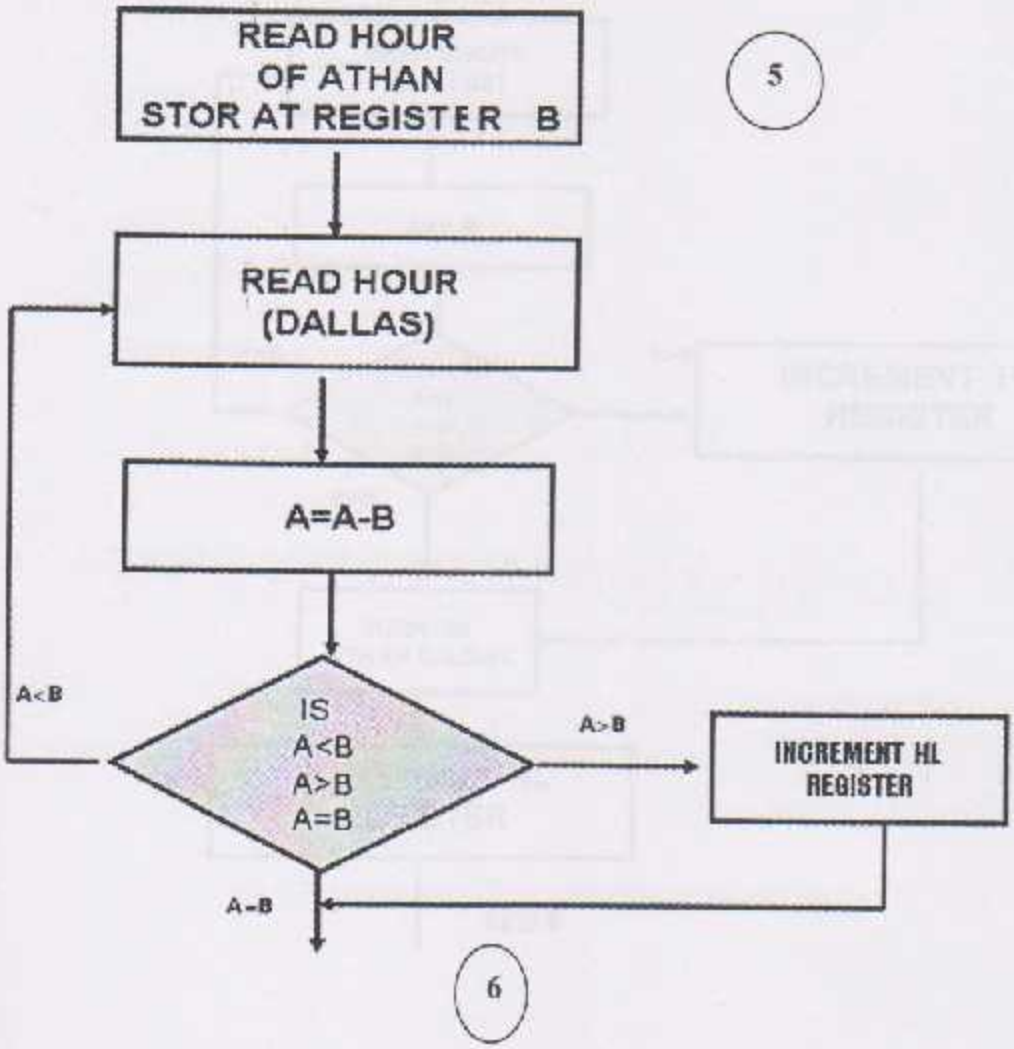


Figure 3.6: Display the Time of Prayer

3.2.4 Compare the Real Time with the Time of Prayer



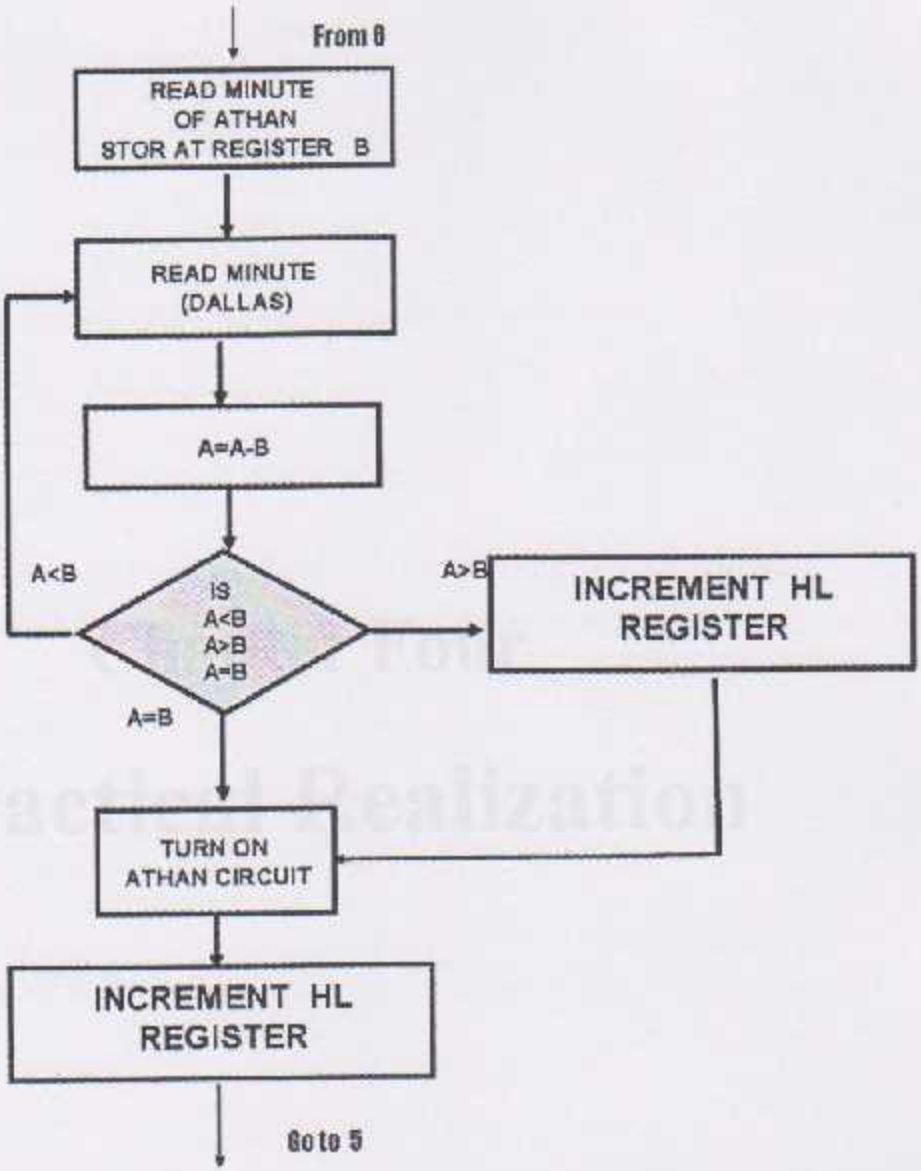


Figure 3.7: Compare the Real Time With the Time of Prayer

Chapter Four

Practical Realization

Chapter Four

Practical Realization

This chapter contains the practical realization of the project and the steps of executing the project . We divided the work into four parts.

4.1 Display Circuit

First, we made a test on the display circuit design using the circuit maker simulation as the schematic 4. 1 and the simulation was done successfully. The second test was done by connecting the sample parts of the display circuit at the bred board. After that we connected the display circuit at one board.

4.2 Control Circuit

This circuit is the most important part in the project. It was connected carefully as shown in schematic design 4. 2 by using the wire raping method, and the following tests were done.

1- The MPU Testing

Firstly the control circuit connection was tested using the ohmmeter to ensure that the connection is correct. Then, the output signals of the MPU like ALE signal was tested by using the oscilloscope.

2-The EPROM Testing

The other testing was for the EPROM by writing the following testing program and testing the output signal of the SOD (pin 4) of the microprocessor. A square wave was achieved which mean that the EPROM is working properly.

```
MVI   A,0C
SIM
MVI   A,40
SIM
JUMP  0000H
```

3- Real Time Clock Testing

First, the clock was adjusted manually at the bred board using logic switches to enter the values to the time registers as given in table 4.1.

Table 4.1: Adjusting Clock

A3	A2	A1	A0	VALUE	STEP
1	0	0	0	80	Enable Control Registers
1	0	0	1	00	Initialize Seconds =0
1	0	1	0	Minutes	Initialize Minutes
1	0	1	1	Hour	Initialize Hour
1	1	0	0	Day	Initialize Day
1	1	0	1	Date	Initialize Date
1	1	1	0	Month	Initialize Month
1	1	1	1	Year	Initialize Year
1	0	0	0	00	Start counter

After that, the Dallas was tested with the system by applying the program which reads the value of time and display it at the segment:-

```
START:  LDA  3FFD
        OUT  00H
        LDA  3FFE
        OUT  01H
        LDA  3FFB
        OUT  02H
        LDA  3FFA
        OUT  03
        JMP  START
```

4.3 The Athan Circuit

The ALathan circuit was designed and simulated at circuit maker. Then, it was tested at the bred board before connecting it to the control circuit.

4.4 Problems

The most problems was through programming the project .Since we deal with two cods of number (BCD&HEX) and it is necessary to convert from one to another in some operation .

4.5 Result

The project was worked successfully as we designed, the time of pray was displayed accurately.

4.6 Recommendations :

1-It is more effective to use a printed board circuit for this project because it is more effective for a lot of wire connection.

2- A big LCD could be used instead of the large number of seven segments. And it is more better for personal user.

References:

[1]"Digital Muezzin"; Ahmad Hamdan, Belal Amro, Graduation Project for Palestine Polytechnic University, Hebron Palestine, 2003.

[2] www.alldatashet.com.

[3] http://www.kpsec.freeuk.com/.

[4] Ramesh S.Gaonkar,"Microprocessor Architecture, Programming and Applications with 8085, Fifth Edition.

[5] www.maxim-ic.comxim-ic.com.

Appendix

The Software

We store the times of prayer at the EPROM with the starting address 1000H. Then, we write the program of the project which was implemented the flow chart in the previous chapter and download it to the EPROM at the starting address 0000H.

Assembly Program

```
START:  LDA  3FFEH      Read Value of Month From DALLAS
        ANI  1FH
        OUT  03H
        LDA  3FFDH      Read Value of Date From DALLAS
        ANI  3FH
        OUT  02H
        CALL SUMUR
        LDA  3FFBH      Read Value of Hour From DALLAS
        CALL HOUR
LAB:    OUT  00H
        LDA  3FFAH      Read Value of Minutes From DALLAS
        ANI  EF
        OUT  01H
        CALL MONTH      Function of Determine the Month
```

```
MONTH:  LDA  3FFEH
        ANI  1FH
        CPI  01H
        JZ   ONE
```

```
        CPI   02H
        JZ    TWO
        CPI   03H
        JZ    THREE
        CPI   04H
        JZ    FOUR
        CPI   05H
        JZ    FIVE
        CPI   06H
        JZ    SIX
        CPI   07H
        JZ    SEVEN
        CPI   08H
        JZ    EIGT
        CPI   09H
        JZ    NINE
        CPI   10H
        JZ    TEN
        CPI   11H
        JZ    ELEVEN
        CPI   12H
        JZ    TWELV

ONE  :  LXI   H,1000H     Put pointer at  Starting Address( M=1)
        CALL  ADRES
        RET

TWO:    LXI   H,1136H     Put pointer at  Starting Address( M=2)
        CALL  ADRES
        RET

THREE:  LXI   H,1258H     Put pointer at  Starting Address( M=3)
        CALL  ADRES
        RET

FOUR:   LXI   H,138EH     Put pointer at  Starting Address( M=4)
        CALL  ADRES
        RET

FIVE:   LXI   H,14BAH     Put pointer at  Starting Address( M=5)
        CALL  ADRES
        RET
```

```
SIX:      LXI   H, 15F0H      Put pointer at Starting Address( M=6)
          CALL  ADRES
          RET

SEVEN:    LXI   H, 171CH      Put pointer at Starting Address( M=7)
          CALL  ADRES
          RET

EIGHT:    LXI   H, 1852H      Put pointer at Starting Address( M=8)
          CALL  ADRES
          RET

NINE:     LXI   H, 1988H      Put pointer at Starting Address( M=9)
          CALL  ADRES
          RET

TEN:      LXI   H, 1AB4H      Put pointer at Starting Address( M=10)
          CALL  ADRES
          RET

ELEVEN:   LXI   H, 1BEAH      Put pointer at Starting Address( M=11)
          CALL  ADRES
          RET

TWELV:    LXI   H, 1D16 H     Put pointer at Starting Address( M=12)
          CALL  ADRES
          RET

ADRES:    LDA   3FFDH         Function to Determine the Address of
          ANI   3FH           that Day
          OUT   02H
          SUI   01H           Order of Day=(date – 1)* 10
          MVI   C,10H
          MOV   B,A
          MVI   A,00H
ADDE:     ADD   B
          DCR   C
          JNZ   ADDE
          MOV   B,A
CPI       00H
          JNZ   ***
```

```
        LXI   H,1000H
        JMP   DAD
***:    INX   H
        DCR   B
        JNZ   ***
DAD:    CALL  OUT
        RET


OUT:    MOV   D,H          Function to Display the Time of Pray
        MOV   E,L
        CAL   SUMUR
        MOV   A,M
        CAL   HOUR
OUT1:   OUT   04H          Display Time of Fajer
        INX   H
        MOV   A,M
        OUT   05H
        INX   H

        MOV   A,M
        CALL  HOUR
OUT2:   OUT   06H          Display Time of Dohor
        INX   H
        MOV   A,M
        OUT   07H
        INX   H
        MOV   A,M
        CALL  HOUR
OUT3:   OUT   08H          Display Time of Asor
        INX   H
        MOV   A,M
        OUT   09H
        INX   H
        MOV   A,M
        CALL  HOUR
OUT4:   OUT   0AH          Display Time of Magreb
        INX   H
        MOV   A,M
        OUT   0BH
        INX   H
```

```
        MOV  A,M
        CALL HOUR
OUT5:   OUT  0CH          Display Time of Esha
        INX  H
        MOV  A,M
        OUT  0DH
        MOV  H,D
        MOV  L,E
        RET
TIME:   MOV  B,M          Determine the Time of Alathan
DALL:   LDA  3FFAH
        ANI  EF
        OUT  01H
        LDA  3FFBH
        CPI  01H
        JZ   START
        SUB  B
        JM   DALL         If Real Time Less than Time of Pray Time
        JP   NEX          If Real Time Larger than Time of Pray Time
        INX  H
        MOV  B,M
MINUT:  LDA  3FFAH
        ANI  EF
        OUT  01H
        SUB  B
        JM   MINUT
        JP   II
        CALL ATHAN
        JMP  II
NEX :   INX  H
II  :   INX  H
        JMP  TIME


ATHAN:  LDA  1FFBH        Function of Alathan Circuite
        ANI  3FH
        CPI  06H          Determine if the Athan is Fajer or not
        JC   FAG
        OUT  0FH
        CALL DELAY3
        RET
FAG:    OUT  0EH
```

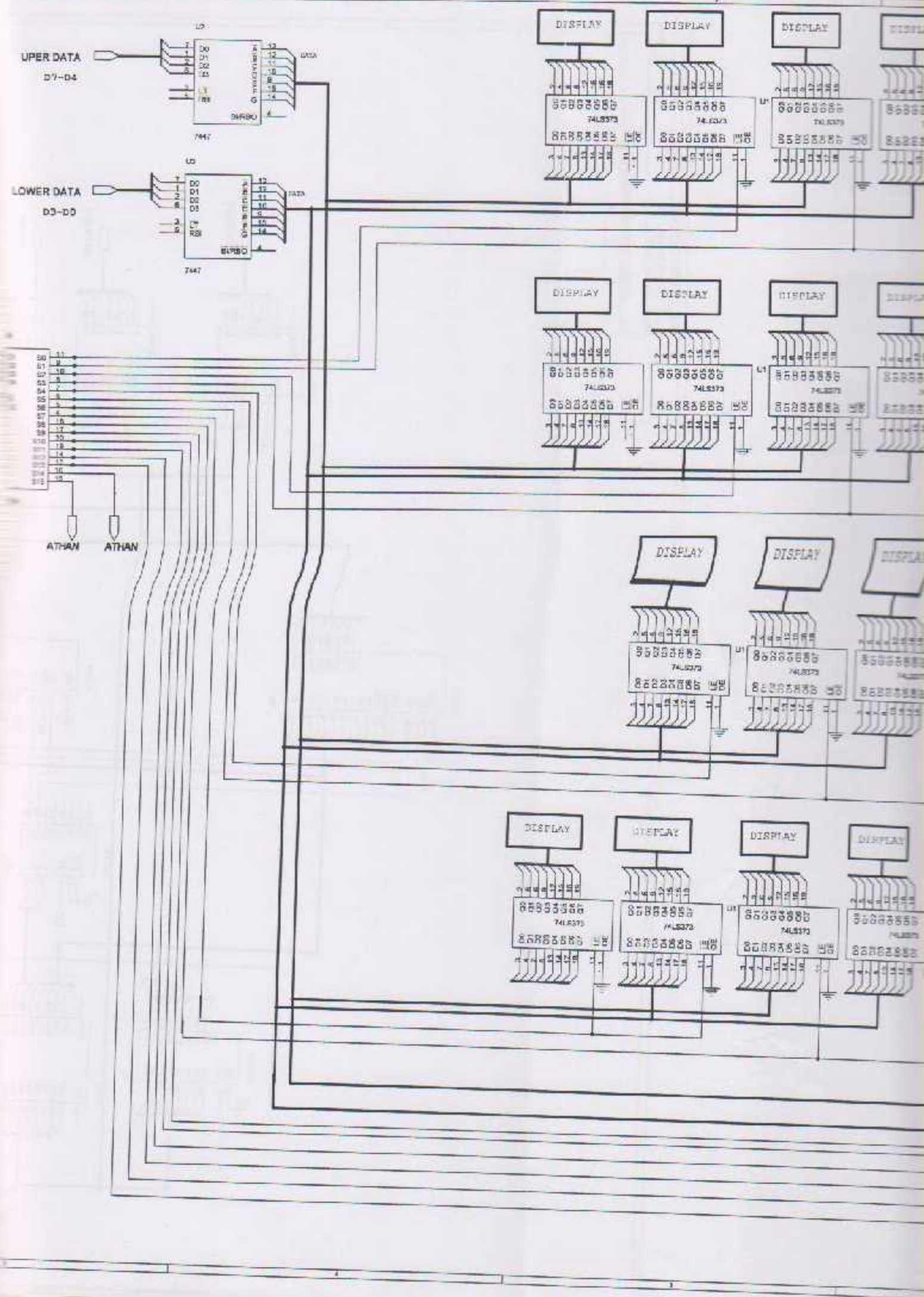
```
        CALL DELAY4
        RET
```

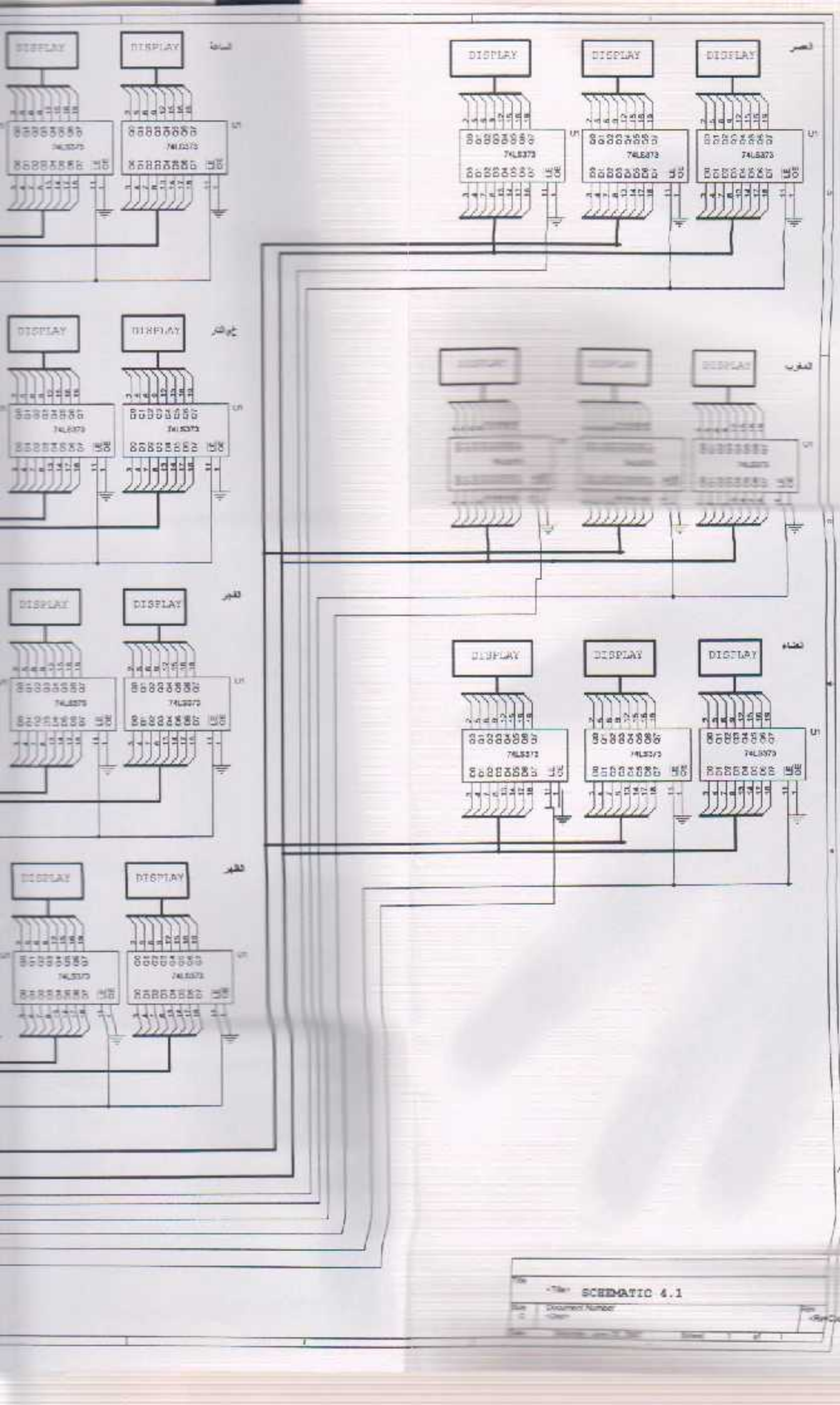
ction For The Sumer &Winter Time

```
ER:     LDA3FFE         Read Value of Month
        ANI   1FH
        CPI   04H       Compare if The Month Between 04 &10
        JZ    COM
        JC    SHAT
        CPI   10H
        JNC   SHAT
        JZ    DAY
        JC    PLUS
        LDA   3FFD
        ANI   3FH
        CPI   07H
        JZ    PLUS
        JNC   PLUS
        JC    SHAT      (**)
        LDA   3FFD
        ANI   3FH
        CPI   23H
        JZ    SHAT
        JNC   SHAT
        MVI   C,01            Add One Hour to the Time
        JMP   RET
        MVI   C,00
        RET
```

on For 24/12 System.

```
        ADD   C
        CPI   12H             Convert From 24to AM/PM
        JC    LAB
        JZ    LAB
        SUI   12H
        RET
```


UPER DATA
D7-D4
LOWER DATA
D3-D0
U3
U2
7447
DISPLAY
74LS373
U1
ATHAN
ATHAN


DISPLAY
74LS373
U1
العصر
المغرب
العشاء
الفجر
الظهر
الساعة
يوم الشهر
SCHEMATIC 4.1

MICROCHIP

27C128

128K (16K x 8) CMOS EPROM

EATURES

- igh speed performance
  - 120 ns access time available
- MOS Technology for low power consumption
  - 20 mA Active current
  - 100 µA Standby current
- actory programming available
- uto-insertion-compatible plastic packages
- uto ID aids automated programming
- eparate chip enable and output enable controls
- igh speed "express" programming algorithm
- rganized 16K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line package
  - 32-pin PLCC Package
  - 28-pin SOIC package
- ape and reel
- ailable for the following temperature ranges:
  - ommercial: 0°C to +70°C
  - ndustrial: -40°C to +85°C
  - utomotive: -40°C to +125°C

ESCRIPTION

icrochip Technology Inc. 27C128 is a CMOS t (electrically) Programmable Read Only Mem- The device is organized as 16K words by 8 bits tes). Accessing individual bytes from an ss transition or from power-up (chip enable pin w) is accomplished in less than 120 ns. CMOS and processing enables this part to be used in ms where reduced power consumption and high ity are requirements.A complete family of pack- offered to provide the most flexibility in applica- For surface mount applications, PLCC, SOIC, or ackaging is available. Tape and reel packaging ailable for PLCC or SOIC packages. UV eras- ions are also available.

family of packages is offered to provide the ility in applications. For surface mount appli- PLCC or SOIC packaging is available. Tape ackaging is also available for PLCC or SOIC

PACKAGE TYPES

DIP/SOIC

PLCC

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

- and input voltages w.r.t. Vss .....-0.6V to +7.25V
- voltage w.r.t. Vss during ramming .....-0.6V to +14V
- age on A9 w.r.t. Vss .....-0.6V to +13.5V
- ut voltage w.r.t. Vss .....-0.6V to Vcc +1.0V
- ge temperature .....-65°C to +150°C
- ent temp. with power applied .....-65°C to +125°C

* Stresses above those listed under "Maximum Ratings" ause permanent damage to the device. This is a stress rat- and functional operation of the device at those or any nditions above those indicated in the operation listings of ification is not implied. Exposure to maximum rating con- extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A13	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Enable
VPP	Programming Voltage
O0 - O7	Data Output
Vcc	+5V Power Supply
Vss	Ground
NC	No Connection; No Internal Connections
NU	Not Used; No External Connection is Allowed

E 1-2: READ OPERATION DC CHARACTERISTICS

Vcc = +5V (±10%)
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C
Extended (Automotive): Tamb = -40°C to +125°C

Parameter	Part*	Status	Symbol	Min.	Max.	Units	Conditions
ages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	Vcc+1 0.8	V V	
age	all	—	ILI	-10	10	µA	VIN = 0 to Vcc
ages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
age	all	—	ILO	-10	10	µA	VOUT = 0V to Vcc
ance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
tance	all	—	COUT	—	12	pF	VOUT = 0V; Tamb = 25°C; f = 1 MHz
Current,	C I,E TTL input	TTL input TTL input	ICC1 ICC2	— —	20 25	mA mA	Vcc = 5.5V; VPP = Vcc f = 1 MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; IOUT = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to Vcc; Note 1
Current,	C I, E all	TTL input TTL input CMOS input	ICC(S)	— — —	2 3 100	mA mA µA	 $\overline{CE}$ = Vcc ± 0.2V
Current voltage	all all	Read Mode Read Mode	IPP VPP	 Vcc-0.7	100 Vcc	µA V	VPP = 5.5V

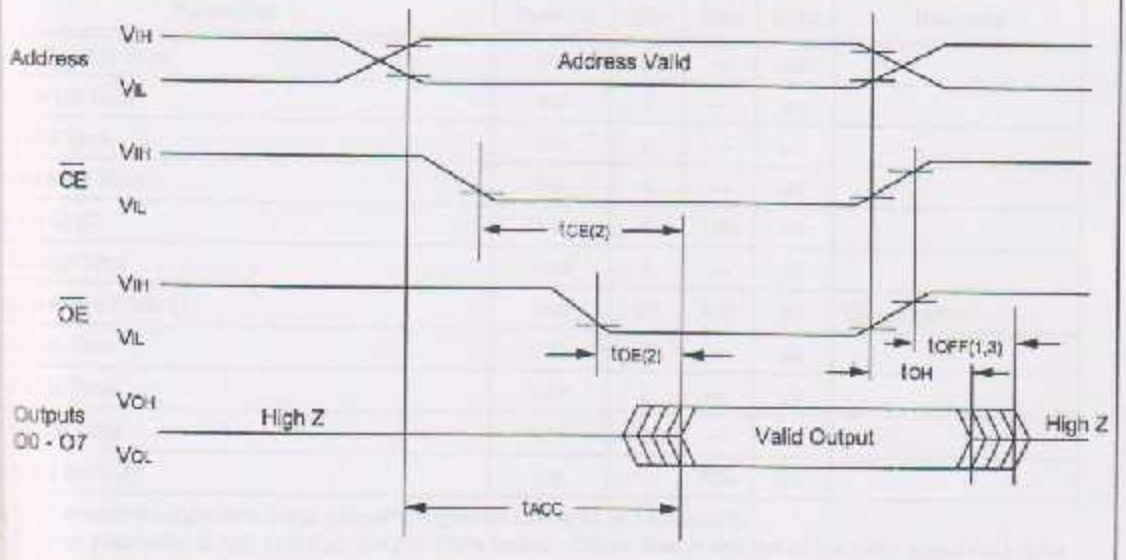
mercial Temperature Range; I, E=Industrial and Extended Temperature Ranges
ical active current increases .75 mA per MHz up to operating frequency for all temperature ranges.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform:	V_{IH} = 2.4V and V_{IL} = 0.45V,	V_{OH} = 2.0V V_{OL} = 0.8V
Output Load:	1 TTL Load + 100 pF	
Input Rise and Fall Times:	10 ns	
Ambient Temperature:	Commercial:	Tamb = 0°C to +70°C
	Industrial:	Tamb = -40°C to +85°C
	Extended (Automotive):	Tamb = -40°C to +125°C

Parameter	Sym	27C128-12		27C128-15		27C128-17		27C128-20		27C128-25		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC	—	120	—	150	—	170	—	200	—	250	ns	$\overline{CE}$=$\overline{OE}$=V_{IL}
$\overline{CE}$ to Output Delay	tCE	—	120	—	150	—	170	—	200	—	250	ns	$\overline{OE}$=V_{IL}
$\overline{OE}$ to Output Delay	tOE	—	65	—	70	—	70	—	75	—	100	ns	$\overline{CE}$=V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	tOFF	0	50	0	50	0	50	0	55	0	60	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever occurs first	tOH	0	—	0	—	0	—	0	—	0	—	ns	

FIGURE 1-1: READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

LE 1-4: PROGRAMMING DC CHARACTERISTICS

Ambient Temperature: Tamb = 25°C ± 5°C
VCC = 6.5V ± 0.25V, VPP = 13.0V ± 0.25V

Parameter	Status	Symbol	Min	Max.	Units	Conditions
ut Voltages	Logic"1" Logic"0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
ut Leakage	—	ILI	-10	10	µA	VIN = 0V to VCC
put Voltages	Logic"1" Logic"0"	VOH VOL	2.4	 0.45	V V	IOH = -400 µA IOL = 2.1 mA
Current, program & verify	—	ICC2	—	20	mA	Note 1
Current, program	—	IPP2	—	25	mA	Note 1
oduct Identification	—	VH	11.5	12.5	V	

VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP

E 1-5: PROGRAMMING AC CHARACTERISTICS

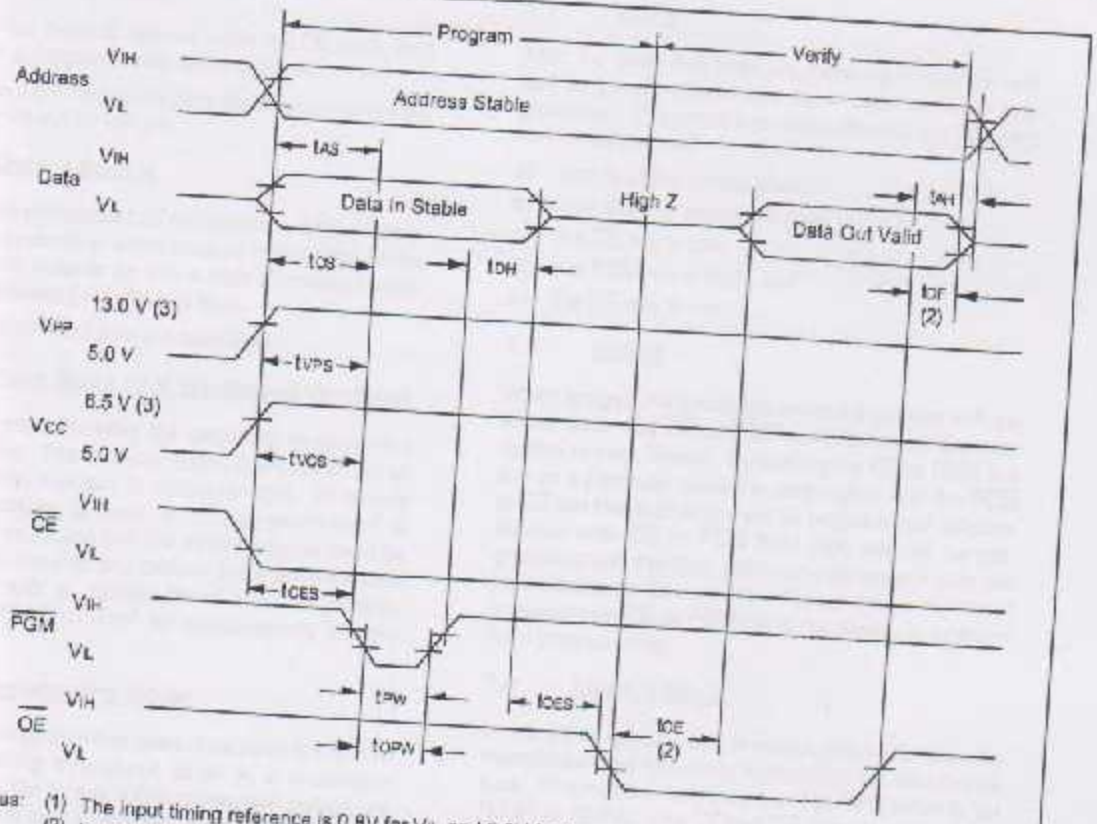
ram, Program Verify
ram Inhibit Modes

AC Testing Waveform: VIH=2.4V and VIL=0.45V; VOH=2.0V; VOL=0.8V
Ambient Temperature: Tamb=25°C± 5°C
VCC= 6.5V ± 0.25V, VPP = VH = 13.0V ± 0.25V

Parameter	Symbol	Min	Max	Units	Remarks
s Set-Up Time	tAS	2	—	µs	
t-Up Time	tDS	2	—	µs	
Hold Time	tDH	2	—	µs	
Hold Time	tAH	0	—	µs	
ay (2)	tDF	0	130	ns	
t-Up Time	tVCS	2	—	µs	
Pulse Width (1)	tPW	95	105	µs	100 µs typical
Time	tCES	2	—	µs	
Time	tOES	2	—	µs	
Time	tVPS	2	—	µs	
from OE	tDF	—	100	ns	

For express algorithm, initial programming width tolerance is 100 µs ±5%.
This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS (1)



Notes: (1) The input timing reference is 0.8V for VIL and 2.0V for VIH.
(2) tDF and tOE are characteristics of the device but must be accommodated by the programmer.
(3) VCC = 6.5V ±0.25V, VPP = VH = 13.0V ±0.25V for Express algorithm.

TABLE 1-6: MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	VPP	A9	O0 - O7
Read	VIL	VIL	VIH	VCC	X	DOUT
Program	VIL	VIH	VIL	VH	X	DIN
Program Verify	VIL	VIL	VIH	VH	X	DOUT
Program Inhibit	VIH	X	X	VH	X	High Z
Standby	VIH	X	X	VCC	X	High Z
Output Disable	VIL	VIH	VIH	VCC	X	High Z
Identity	VIL	VIL	VIH	VCC	VH	Identity Code

X = Don't Care

Read Mode

The Timing Diagrams and AC Characteristics)
Read Mode is accessed when
the $\overline{CE}$ pin is low to power up (enable) the chip
the $\overline{CE}$ pin is low to gate the data to the output
pins

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (tOE).

1.3 Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (VIH) and a program mode is not defined.

When these conditions are met, the supply current will drop from 20 mA to 100 µA.

1.4 Output Enable

This feature eliminates bus contention in microprocessor-based systems in which multiple devices may drive the bus. The outputs go into a high impedance state when the following condition is true:

- The $\overline{OE}$ and $\overline{PGM}$ pins are both high.

1.5 Erase Mode (U.V. Windowed Versions)

Windowed products offer the capability to erase the memory array. The memory matrix is erased to the all 1's state when exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000µW/cm^2 for approximately 20 minutes.

1.6 Programming Mode

The Express Algorithm has been developed to improve the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1-3.

Programming takes place when:

a) VCC is brought to the proper voltage,
b) VPP is brought to the proper VH level,
c) the $\overline{CE}$ pin is low,
d) the $\overline{OE}$ pin is high, and
e) the $\overline{PGM}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A13 and the data to be programmed is presented to pins O0-O7. When data and address are stable, $\overline{OE}$ is high, $\overline{CE}$ is low and a low-going pulse on the $\overline{PGM}$ line programs that location.

1.7 Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) VCC is at the proper level,
b) VPP is at the proper VH level,
c) the $\overline{CE}$ line is low,
d) the $\overline{PGM}$ line is high, and
e) the $\overline{OE}$ line is low.

1.8 Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ or $\overline{PGM}$ need be under separate control to each device. By pulsing the $\overline{CE}$ or $\overline{PGM}$ line low on a particular device in conjunction with the $\overline{PGM}$ or $\overline{CE}$ line low, that device will be programmed; all other devices with $\overline{CE}$ or $\overline{PGM}$ held high will not be programmed with the data, although address and data will be available on their input pins (i.e., when a high level is present on $\overline{CE}$ or $\overline{PGM}$); and the device is inhibited from programming.

1.9 Identity Mode

In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc. and device type. This mode is entered when Pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type*	VIH	1	0	0	0	0	0	1	1	83

* Code subject to change

DALLAS SEMICONDUCTOR

DS1643
Nonvolatile Timekeeping RAM

FEATURES

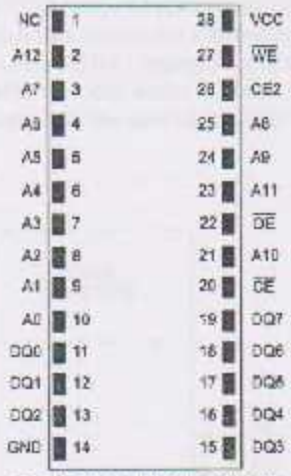
- Form, fit, and function compatible with the MK48T08 Timekeeping RAM
- Integrated NV SRAM, real time clock, crystal, power–fail control circuit and lithium energy source
- Standard JEDEC bytewide 8K x 8 static RAM pinout
- Clock registers are accessed identical to the static RAM. These registers are resident in the eight top RAM locations.
- Totally nonvolatile with over 10 years of operation in the absence of power
- Access times of 120 ns and 150 ns
- Quartz accuracy ±1 minute a month @ 25°C, factory calibrated
- BCD coded year, month, date, day, hours, minutes, and seconds with leap year compensation valid up to 2100
- Power–fail write protection allows for ±10% V_{CC} power supply tolerance

ORDERING INFORMATION

DS1643–XXX 28–pin DIP module

–120 120 ns access
–150 150 ns access

PIN ASSIGNMENT



28–PIN ENCAPSULATED PACKAGE
(720 MIL EXTENDED)

DESCRIPTION

The DS1643 is an 8K x 8 nonvolatile static RAM with a full function real time clock which are both accessible in a bytewide format. The nonvolatile time keeping RAM is pin and function equivalent to any JEDEC standard 8K x 8 SRAM. The device can also be easily substituted in ROM, EPROM and EEPROM sockets providing read/write nonvolatility and the addition of the real time clock function. The real time clock information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24 hour BCD format. Corrections for the day of the month and leap year are made automatically. The RTC clock registers are double buffered to avoid access of incorrect data that can occur during clock update cycles. The double buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1643 also contains its own power–fail circuitry which deselects the device when the V_{CC} supply is in an out of tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low V_{CC} as errant access and update cycles are avoided.

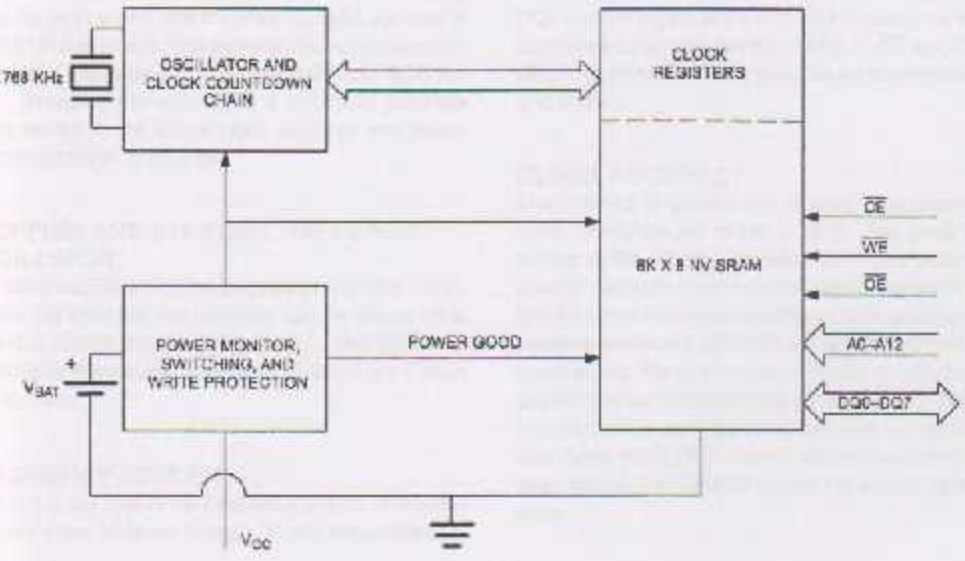
PIN DESCRIPTION

A0–A12	–	Address Input
$\overline{CE}$	–	Chip Enable
$\overline{OE}$	–	Output Enable
$\overline{WE}$	–	Write Enable
NC	–	No Connection
V_{CC}	–	+5 Volts
GND	–	Ground
DQ0-DQ7	–	Data Input/Output

CLOCK OPERATIONS–READING THE CLOCK

While the double buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1643 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a one is written into the read bit, the seventh most significant bit in the control register. As long as a one remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double buffered system continue to update so that the clock accuracy is not affected by the access of data. All of the DS1643 registers are updated simultaneously after the clock status is reset. Updating is within a second after the read bit is written to zero.

DS1643 BLOCK DIAGRAM Figure 1



DS1643 TRUTH TABLE Table 1

V_{CC}	$\overline{CE}$	CE2	$\overline{OE}$	$\overline{WE}$	MODE	DQ	POWER
5 VOLTS ± 10%	V_{IH}	X	X	X	DESELECT	HIGH Z	STANDBY
	X	V_{IL}	X	X	DESELECT	HIGH Z	STANDBY
	V_{IL}	V_{IH}	X	V_{IL}	WRITE	DATA IN	ACTIVE
	V_{IL}	V_{IH}	V_{IL}	V_{IH}	READ	DATA OUT	ACTIVE
	V_{IL}	V_{IH}	V_{IH}	V_{IH}	READ	HIGH Z	ACTIVE
<4.5 VOLTS >V_{BAT}	X	X	X	X	DESELECT	HIGH Z	CMOS STANDBY
<V_{BAT}	X	X	X	X	DESELECT	HIGH Z	DATA RETENTION MODE

SETTING THE CLOCK

The 8–bit of the control register is the write bit. Setting the write bit to a one, like the read bit, halts updates to the DS1643 registers. The user can then load them with the correct day, date and time data in 24 hour BCD format. Resetting the write bit to a zero then transfers those values to the actual clock counters and allows normal operation to resume.

STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB for the seconds registers. Setting it to a 1 stops the oscillator.

FREQUENCY TEST BIT

Bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic "1" and the oscillator is running, the LSB of the seconds register will toggle at 512 Hz. When the seconds register is being read, the DQ0 line will toggle at the 512 Hz frequency as long as conditions for access remain valid (i.e., $\overline{CE}$ low, $\overline{OE}$ low, CE2 high, and address for seconds register remain valid and stable).

CLOCK ACCURACY

The DS1643 is guaranteed to keep time accuracy to within ±1 minute per month at 25°C. The clock is calibrated at the factory by Dallas Semiconductor using special calibration nonvolatile tuning elements. The DS1643 does not require additional calibration and temperature deviations will have a negligible effect in most applications. For this reason, methods of field clock calibration are not available and not necessary. Attempts to calibrate the clock that may be used with similar device types (MK48T08 family) will not have any effect even though the DS1643 appears to accept calibration data.

DS1643 REGISTER MAP – BANK1 Table 2

ADDRESS	DATA								FUNCTION	
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1FFF	–	–	–	–	–	–	–	–	YEAR	00–99
1FFE	X	X	X	–	–	–	–	–	MONTH	01–12
1FFD	X	X	–	–	–	–	–	–	DATE	01–31
1FFC	X	FT	X	X	X	–	–	–	DAY	01–07
1FFB	X	X	–	–	–	–	–	–	HOUR	00–23
1FFA	X	–	–	–	–	–	–	–	MINUTES	00–59
1FF9	$\overline{OSC}$	–	–	–	–	–	–	–	SECONDS	00–59
1FF8	W	R	X	X	X	X	X	X	CONTROL	A

$\overline{OSC}$ = STOP BIT
W = WRITE BIT
R = READ BIT
X = UNUSED
FT = FREQUENCY TEST

NOTE:
All indicated "X" bits are not dedicated to any particular function and can be used as normal RAM bits.

RETRIEVING DATA FROM RAM OR CLOCK

The DS1643 is in the read mode whenever $\overline{WE}$ (write enable) is high and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within t_{AA} after the last address input is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times and states are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, valid data will be available at the latter of chip enable access (t_{CEA}) or at output enable access time (t_{OEA}). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$ and $\overline{OE}$. If the outputs are activated before t_{AA}, the data lines are driven to an intermediate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain valid, output data will remain valid for output data hold time (t_{OH}) but will then go indeterminate until the next address access.

WRITING DATA TO RAM OR CLOCK

The DS1643 is in the write mode whenever $\overline{WE}$ and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring transition of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return inactive for a minimum of t_{WR} prior to the initiation of another read or write cycle. Data in must be valid t_{DS} prior to the end of write and remain valid for t_{DH} afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{CE}$ is low prior to $\overline{WE}$ transitioning low the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the outputs t_{WEZ} after $\overline{WE}$ goes active.

DATA RETENTION MODE

When V_{CC} is within nominal limits (V_{CC} > 4.5 volts) the DS1643 can be accessed as described above by read or write cycles. However, when V_{CC} is below the power-fail point V_{PF} (point at which write protection occurs) the internal clock registers and RAM is blocked from access. This is accomplished internally by inhibiting access via the $\overline{CE}$ and CE2 signals. When V_{CC} falls below the level of the internal battery supply, power input is switched from the V_{CC} pin to the internal battery and clock activity, RAM, and clock data are maintained from the battery until V_{CC} is returned to nominal level.

INTERNAL BATTERY LONGEVITY

The DS1643 has a self contained lithium power source that is designed to provide energy for clock activity, and clock and RAM data retention when the V_{CC} supply is not present. The capability of this internal power supply is sufficient to power the DS1643 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at 25°C with the internal clock oscillator running in the absence of V_{CC} power. The DS1643 is shipped from Dallas Semiconductor with the clock oscillator turned off, so the expected life should be considered to start from the time the clock oscillator is first turned on. Actual life expectancy of the DS1643 will be much longer than 10 years since no internal lithium battery energy is consumed when V_{CC} is present. In fact, in most applications, the life expectancy of the DS1643 will be approximately equal to the shelf life (expected useful life of the lithium battery with no load attached) of the lithium battery which may prove to be as long as 20 years.

8085A

8-Bit Microprocessor

MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

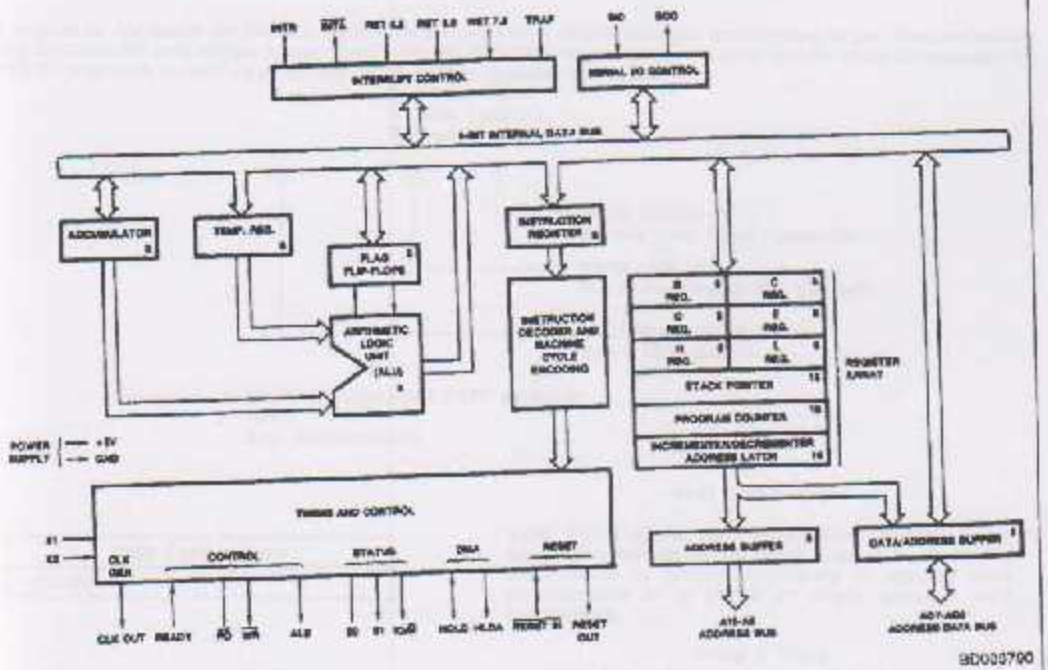
- SMD/DESC qualified
- 3- and 5-MHz selections available
- On-chip system controller; advanced cycle status information available for large system control
- Four vectored interrupts (one is non-maskable)
- On-chip clock generator (with external crystal, LC or R/C network)
- Serial in/serial-out port
- Decimal, binary, and double-precision arithmetic
- Direct addressing capability to 64K bytes of memory
- 1.3 µs instruction cycle (8085A)
- 0.8 µs instruction cycle (8085A-2)
- 100% software-compatible with 8080A
- Single +5 V power supply

GENERAL DESCRIPTION

The 8085A is a new generation, complete 8-bit parallel central processing unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor. Specifically, the 8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A. The 8085A-2 is a faster version of the 8085A. The 8085A is a 3-MHz CPU with 10% supply tolerances and lower power consumption.

The 8085A uses a multiplexed data bus. The address is split between the 8-bit address bus and the 8-bit data bus. The on-chip address latches of 8155H/56H memory products allow a direct interface with 8085A. The 8085A components, including various timing-compatible support chips, allow system speed optimization.

BLOCK DIAGRAM



9D003790

Publication # 09231 Rev. A Amendment /0
Issue Date: November 1987

CONNECTION DIAGRAM
Top View
DIPs

CD005564

Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

Standard Military Drawing (SMD)/DESC Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for SMD/DESC products is formed by a combination of: **a. Military Drawing Part Number**
b. Device Type
c. Case Outline
d. Lead Finish

79010 — 01 — Q — X

d. LEAD FINISH
X = Any Lead Finish Acceptable

c. CASE OUTLINE
Q = 40-Pin Ceramic DIP (CD 040)

b. MILITARY DEVICE TYPE
01 = 3 MHz (8085A)

a. MILITARY DRAWING PART NUMBER
79010
8-Bit Microprocessor

Valid Combinations	
7901001	QX

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released valid combinations.

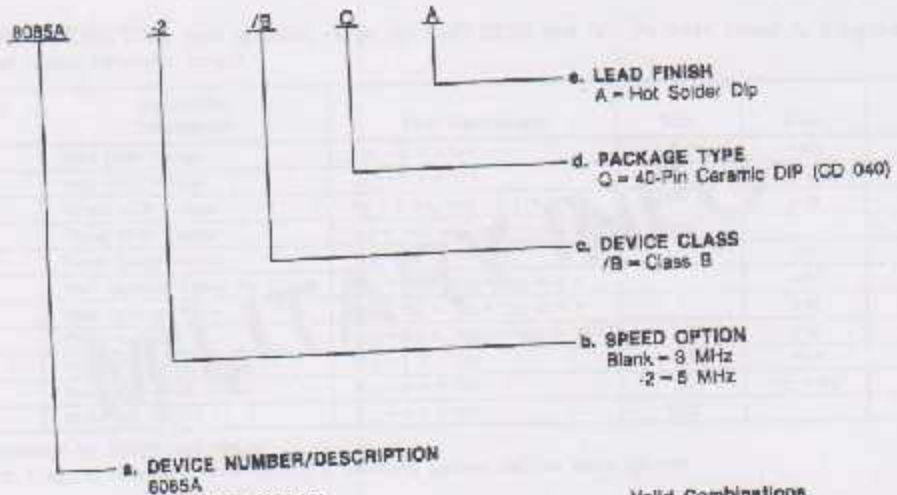
Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

MILITARY ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
8085A	/BQA
8085A-2	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage on Any Pin
With Respect to Ground ..... −0.5 to +7 V
Power Dissipation ..... 1.5 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... 5 V ±10%
Supply Current (I_{CC}) ..... 200 mA

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage	V_{CC} = 5 V ±10%	−0.5*	+0.8	V
V_{IH}	Input HIGH Voltage	V_{CC} = 5 V ±10%	2.2	V_{CC} +0.5*	V
V_{OL}	Output LOW Voltage	I_{OL} = 2 mA, V_{CC} = 5 V ±10%		0.45	V
V_{OH}	Output HIGH Voltage	I_{OH} = −400 µA, V_{CC} = 5 V ±10%	2.4		V
I_{CC}	Power Supply Current	V_{CC} = 5.5 V (NOTE 1)		200	mA
I_{IL1}	Input Leakage, Except Pin 1	V_{IN} = V_{CC} to 0 V		±10	µA
I_{IL2}	Input Leakage, Pin 1	V_{CC} = 5.5 V, V_{IN} = V_{CC} to 0 V		±70	µA
I_{LO}	Output Leakage	V_{CC} = 5.5 V, V_{OUT} = V_{CC} to .45 V		±10	µA
V_{ILR}	Input LOW Voltage, RESET	V_{CC} = 5 V ±10%	−0.5*	+0.8	V
V_{IHR}	Input HIGH Voltage, RESET	V_{CC} = 5 V ±10%	2.4	V_{CC} +0.5*	V
V_{HY}	Hysteresis, RESET	V_{CC} = 5 V ±10%	0.25		V

*Guaranteed by design; not tested.

Notes: 1. I_{CC} is measured while running a functional pattern with no loads applied.

See Section 6 of the MOS Microprocessors and Peripherals Data Book (Order #230843A) for Thermal Characteristics Information.

SWITCHING CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	8085A (Note 2)		8085A-2 (Note 2)		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	CLK Cycle Period	320	2000	200	2000	ns
t_1	CLK LOW Time (Standard CLK Loading)	80		40		ns
t_2	CLK HIGH Time (Standard CLK Loading)	120		70		ns
t_r, t_f	CLK Rise and Fall Time		30		30	ns
t_{2XR}	X_1 Rising to CLK Rising	20	120	20	100	ns
t_{2XF}	X_1 Rising to CLK Falling	20	150	20	110	ns
t_{AC}	A_{8-15} Valid to Leading Edge of Control (Note 1)	270		115		ns
t_{ACL}	A_{0-7} Valid to Leading Edge of Control	240		115		ns
t_{AD}	A_{0-15} Valid to Valid Data In		575		350	ns
t_{AFR}	Address Float After Leading Edge of READ (INTA)		0		0	ns
t_{AL}	A_{8-15} Valid Before Trailing Edge of ALE (Note 1)	90		50		ns
t_{ALL}	A_{0-7} Valid Before Trailing Edge of ALE	70		50		ns
t_{ARY}	READY Valid from Address Valid		220		100	ns
t_{CA}	Address (A_{8-15}) Valid After Control	120		60		ns
t_{CC}	Width of Control LOW (RD, WR, INTA) Edge of ALE	400		230		ns
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	50		25		ns
t_{DW}	Data Valid to Trailing Edge of WRITE	420		230		ns
t_{HABE}	HLDA to Bus Enable		210		150	ns
t_{HABF}	Bus Float After HLDA		210		150	ns
t_{HACK}	HLDA Valid to Trailing Edge of CLK	110		40		ns
t_{HDH}	HOLD Hold Time	0		0		ns
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		120		ns
t_{INH}	INTR Hold Time	0		0		ns
t_{INS}	INTR, RST, and TRAP Setup Time to Falling Edge of CLK	160		150		ns
t_{LA}	Address Hold Time After ALE	100		50		ns
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	130		60		ns
t_{LCK}	ALE LOW During CLK High	100		50		ns
t_{LDR}	ALE to Valid Data During Read		460		270	ns
t_{LDW}	ALE to Valid Data During Write		200		120	ns
t_{LL}	ALE Width	140		80		ns
t_{LRY}	ALE to READY Stable		110		90	ns
t_{RAE}	Trailing Edge of READ to Re-Enabling of Address	150		90		ns
t_{RD}	READ (or INTA) to Valid Data		300		160	ns
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	400		220		ns
t_{RDH}	Data Hold Time After READ INTA (Note 6)	0		0		ns
t_{RYH}	READY Hold Time	0		0		ns
t_{RYS}	READY Setup Time to Leading Edge of CLK	110		100		ns
t_{WD}	Data Valid After Trailing Edge of WRITE	100		60		ns
t_{WDL}	LEADING Edge of WRITE to Data Valid		40		20	ns

Notes: 1. $A_8 - A_{15}$ address Specs apply to IO/$\overline{M}$, S_0 and S_1, except $A_8 - A_{15}$ are undefined during $T_4 - T_6$ of OF cycle; whereas, IO/$\overline{M}$, S_0, and S_1 are stable.

2. Test conditions: t_{CYC} = 320 ns (8085A)/200 ns (8085A-2); C_L = 100 pF; V_{CC} = 5 V ±10%; V_{IL} = .45 V; V_{IH} = 2.4 V; V_{OL} = .8 V; V_{OH} = 2.0 V.

3. For all output timing where C_L = 150 pF use the following correction factors:
25 pF ≤ C_L < 150 pF: ±0.10 ns/pF
150 pF < C_L ≤ 300 pF: ±0.30 ns/pF

4. Output timings are measured with purely capacitive load.

5. To calculate timing specifications at other values of t_{CYC} use Table 3 on page 3-191 of the MOS Microprocessors and Peripherals Data Book (Order #09067A)

6. Data hold time is guaranteed under all loading conditions.