Palestine Polytechnic University
College of Applied Science

CONTROLLED ROOM

Graduation Project

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MAY- 2007

Palestine Polytechnic University

HEBRON-PALESTINE

CONTROLLED ROOM

Project Team

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In accordance with the recommendation of project supervisors and acceptance of all examining committee members, this project has been submitted to the Department of Applied Electronics in the College of Applied Sciences in partial fulfillment of requirements of the Department for Degree of Bachelor of applied electronics.

Signature of Project Supervisor

Name.....

Signature of Department Chairman

Name.....

MAY- 2007

ABSTRACT

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This project is to design and build a controlled room, to control door opening by IR-Sensor from 8 AM to 2 PM, Keypad from 2PM to 8AM through DALAS Timer, Lightning strength and window opening by LDR, person detector to detect if anybody in the house by Passive IR, all of these operations are done through motors such as door opening process, these inputs and outputs are connected through the 8085 microprocessor, which gives the ability to program and synchronize these operations.

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1

INTRODUCTION

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1.1 Overview

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1.3 Time Plan

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CHAPTER ONE

INTRODUCTION

1.1 Overview

Since humanity always looking for flexibility and comfortability, and with all technologies and since revolution man kinds have reaches, with all the humans have done some investment into their life's using those technologies that they reached.

Being one of the people who are learned in some of the sections of seine , make us to feel responsible for doing what makes the life for human more comfortable , if consider that we are studies electronic.

Depending on all the above we have choose our project subject which is called (control room), which is the main target for it is to make life easier and more comfortable.

Such a technologies are used in a different aspects of life , the most aspects are in hotels and companies and university door rooms, all of these combinations used this kind of technology to ensure that they save the electrical power consuming , and to have more security in their institutes.

In general, the room have a sensor inside the room (Movement sensor), which detect whither there is a person inside the room or not, if their is a person inside the room, the sensor will turn on the light, and gives the person the ability to control the room, but if there is not anyone in the room, the sensor will turn off the light, and close the windows of the room, and disable any control to the room.

The project is based on three main components which they are critical points in the room work:

1) door control
2) window control
3) lamp control

controlling the door depends on the time, which means that we programmed the door in two cases, first case is when the time is between 8:00AM to 2:00PM o'clock AM, in this time the door will open to all the users, by distributing the photo electric signal that is on the door, that means that any one is cut the signal between the transmitter and the receiver, the door will open.

The second case is between 2:00 PM to 8:00 AM o'clock PM, the users of the room inforce to enter a serial number "password" to enable them to enter the room, through a keypad.

The second basic component is the window, which have a sensor called LDR, this sensor detect the light of the sun, in order to open the window if there is a light, or to close it when it is night.

1.2 Literature Review

We were research in our university and its library about any literature review support our project, but we did not found any literature review.
In the internet, we are finding some of literature review as shown as below:

Loucetios self-configuring lighting control system solution for bedrooms, offices and perimeter areas. Under automatic operation, the system senses luminosity inside and outside a room, controls the angle of the blinds and dims the lamps to

maintain a prescribed level of illumination inside the room. The system also provides the user with 4 pre-programmed ambience settings that can set the tone of the room with just a button press. Loucetios is an environmentally friendly system that saves energy by keeping unoccupied rooms unlit and maximizing the use of available natural light. In the long-run, provides control solutions that reduce energy costs and extend lamp life.

Smart House Possible pieces may include a centrally controllable lighting system, microphone array design for voice recognition and speech synthesis to interact with the appliances, entertainment system which allows individual configurations in different rooms, Each sensor is wired back to the central computer using a separate cable. An interface at the computer allows a program to probe the values being returned by each of the sensors

Electronic combination lock with PIC -P16F628-This is electronic combination lock to use with an outdoor gate. The functionality is implemented in software. It turns on a relay (usually to open a door) for a few seconds if someone enters the valid code. This relay can operate a power-to-open type electric strike with a shorting contact or a power-to-hold type electromagnetic lock with a breaking contact (the relay is used because these locks usually work with AC, not DC). The code can be changed any time after entering the current code.

1.3 Time Plan

Table 1-1: Time Plan

Week / FUN	A	B	C	D	E	F	G	H	I	J
1										
2										
3										
4										
5										
6										
7										
8										
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32										

task	Description
A	Problem searching
B	Project selectivity
C	Searching project component
D	Circuit building
E	Design final circuit
F	Write instruction of microprocessor
G	Programming the microprocessor
H	Building and testing the circuit of the project
I	Building the body of the project
J	Connect all circuit with microprocessor

1.4 Brief Project Budget:

Table 1.2: Brief Project Budget:

Part name	Qut.	Total Cost($)
Optocouplers 4N25	4	5
Transistors BD442/1	8	8
Diodes N2007	4	1
Resistors	x	2
Transistor BC547	1	1
Cooper Board 50cm	X	15
IR LED	1	1
IC sockets	X	30
Wire	X	5
Wire wrapping	X	5
DVD BOX	2	10
Photo diode	1	4
LDR	1	1
Tin	X	10
MOC3023	1	2
DS1643	1	15
Triac Q4004	1	2
IC Schmitt trigger 7414	1	2
PIR	1	20
Regulator 7805	1	1
Packaging House	X	60
Total Budget in US Dollars ($)		**230.0**

1.5 block diagram

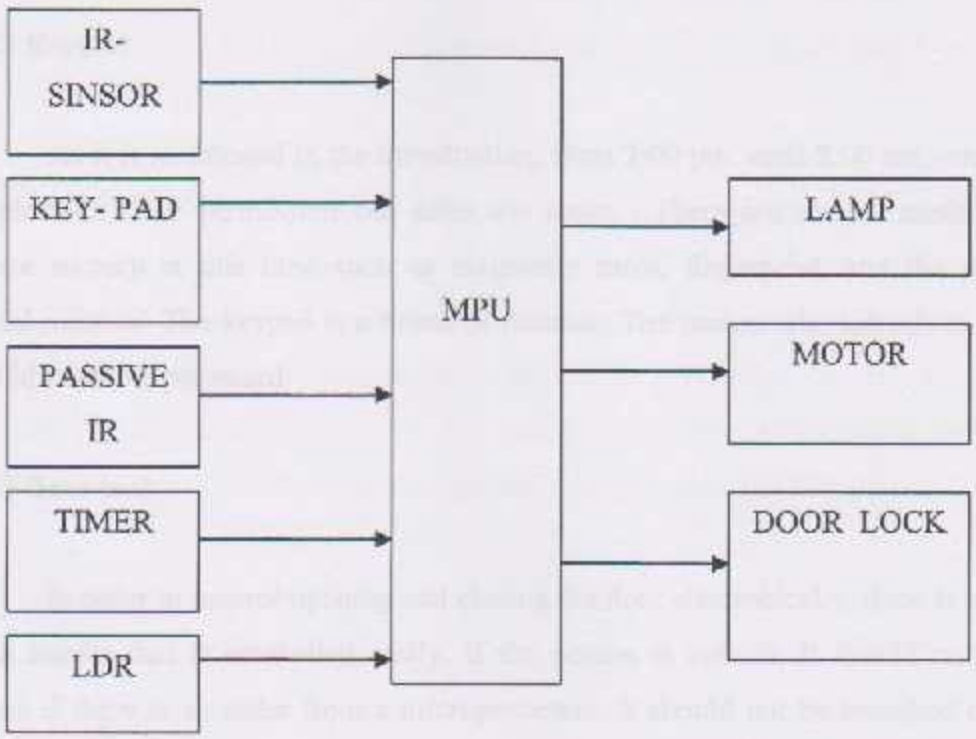


Figure 1.1: block diagram

1.6 project component

1.6.1 IR Sensor

We need to know in the case if someone approached the door and wants to enter. The easiest way is the presence of a light signal. If someone crossed this sign, this sign shows that a person is near the door.

In order to implement this idea, there is a need for a receiver and a sender as the sender transmits constantly a signal to the receiver. This signal doesn't break up unless a person passed between the receiver and the sender. The sign coming from

the sender should suit the features of the receiver. That is the receiver should be only affected by the signal that is transmitted by the sender.

1.6.2 Keypad

As it is mentioned in the introduction, from 2:00 pm. until 8:00 am., only the people who have permission can enter the room. There are several methods to ensure secrecy at this time such as magnetite cards, fingerprint, and the private digital number. The keypad is a board of number. The person who intends to go in should enter the password.

1.6.3 Door lock

In order to control opening and closing the door electronically, there is a need for a handle that is controlled easily. If the person is outside, it should not open unless if there is an order from a microprocessor. It should not be breached easily. Whereas, from inside it doesn't need the order from the microprocessor.

1.6.4 Motor

This project needs a motor that is capable to open and close the window. This motor should be fitting to the electricity volts that are used in houses and offices and the surrounding environment. It is neither inside the room nor outside it. Thus it should be fitting to the humidity and the temperature that is in the site. We should take into consideration the speed of this device, sound, and its energy.

1.6.5 Movement sensor

Movement sensor predicts if someone is inside the room and it should cover all the room. It shouldn't also give a signal that there is someone f he s sleeping. This aims to save electricity and security as the window doesn't open unless someone is inside the room. Several types of such sensors are available such as PIR DETE , AIR DE, Microwave, Ultrasonic and others.

1.6.6 Microprocessor

There is a need for a microprocessor to connect and control the operation of the devices that are used in the project. It is necessary also that the microprocessor functions in accordance to time that the project ids divided according to as stated previously. It is easy to do so through programming the microprocessor.

1.6.7 Timer

As it is mentioned above, the project is divided into two parts regarding the time. The main piece in the project that determines the operation of the devices in accordance to time and should know the definite time precisely is the microprocessor. Thus, there is a need for a device that gives the time precisely and to be suitable for the microprocessor. At the same time, it should provide the day and keep on working regardless of the outside effects such as interruption of electricity....

1.6.8 Light sensor

There is a need for a light sensor to enable the microprocessor to distinguish whether it is night or day and to implement that given order according to the time.

There is no need to know the exact amount of light inside the room. What is needed is only is to know whether there is day light or night light.

CHAPTER

2

Control

The following contents are going to be covered in this chapter:

2.1 Microprocessor 8085

2.2 Memory

2.3 DS1643 Nonvolatile Timekeeping RAM

CHAPTER TWO

Control

2.1 Microprocessor 8085

2.1.1 Why Microprocessor 8085

1. It is an 8-bit microprocessor, such processor is required for this simple system, it's not complex to interface and program this processor.
2. Speed is convenient.
3. The programmer is available.
4. And our project doesn't need to a large ability which presents from the microcontroller.

Microprocessor is an electronic circuit that functions as the central processing unit (CPU) of a computer, providing computational control.

2.1.2 Introduction to 8085 Architecture and Programming

1. Internal architecture of 8085 microprocessor
2. 8085 pin description.
3. Instruction format.

1. Internal Architecture of 8085 Microprocessor

Control Unit.

Generates signals to carry out the instruction, which has been decoded. In reality causes certain connections between blocks of the MPU to be opened or closed, so that data goes where it is required, and so that ALU operations occur.

Arithmetic Logic Unit

The ALU performs the actual numerical and logic operation such as 'add', 'subtract', 'AND', 'OR', etc. Uses data from memory and from Accumulator to perform arithmetic. Always stores result of operation in Accumulator.

Registers

The 8085 programming model includes six registers, one accumulator, and One flag register, as shown in Figure 2.1 , In addition, it has two 16-bit registers: the stack pointer and the program counter. They are described briefly as follows. The 8085 has six general-purpose registers to store 8-bit data; these are identified as B,C,D,E,H, and L as shown in the figure. They can be combined as register pairs - BC, DE, and HL - to perform some 16-bit operations. The programmer can use these registers to store or copy data into the registers by using data copy instructions.

Accumulator

The accumulator is an 8-bit register that is a part of arithmetic/logic unit (ALU). This register is used to store 8-bit data and to perform arithmetic and logical operations. The result of an operation is stored in the accumulator. The accumulator is also identified as register A.

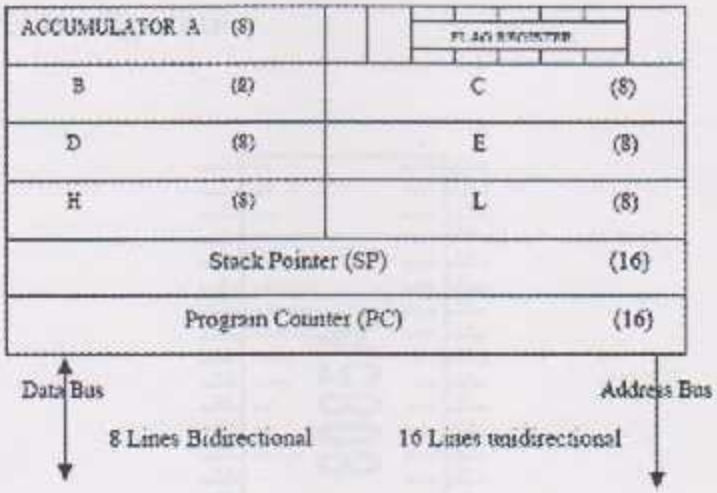


Figure 2-1: 8085 register

Flags

The ALU includes five flip-flops, which are set or reset after an operation according to data conditions of the result in the accumulator and other registers. They are called Zero (Z), Carry (CY), Sign (S), Parity (P), and Auxiliary Carry (AC) flags; they are listed in the Table and their bit positions in the flag register are shown in the Figure below. The most commonly used flags are Zero, Carry, and Sign. The microprocessor, the flag register shown in figure 2-2.

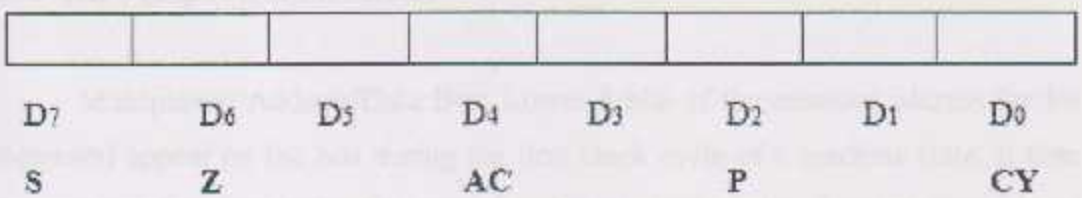


Figure 2-2: flags register

2.1.3 8085 Pin configuration.

Figure 2-3: 8085A

2.1.3.1 The following describes the function of each pin:

A6 - A1s (Output 3 State)

Address Bus; The most significant 8 bits of the memory address or the 8 bits of the I/0 addresses, 3 stated during Hold and Halt modes.

AD0 -AD 7 (Input/Output 3state)

Multiplexed Address/Data Bus; Lower 8 bits of the memory address (or I/0 addresses) appear on the bus during the first clock cycle of a machine state. It then becomes the data bus during the second and third clock cycles. 3 stated during Hold and Halt modes.

ALE (Output)

Address Latch Enable: It occurs during the first clock cycle of a machine state and enables the address to get latched into the on chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. ALE can also be used to strobe the status information. ALE is never 3stated.

SO, S1 (Output)

Data Bus Status. Encoded status of the bus cycle:

S1 S0

O O HALT

0 1 WRITE

1 0 READ

1 1 FETCH

S1 can be used as an advanced R/W status.

RD (Output 3state)

READ; indicates the selected memory or 1/0 device is to be read and that the Data Bus is available for the data transfer.

WR (Output 3state)

WRITE; indicates the data on the Data Bus is to be written into the selected memory or 1/0 location. Data is set up at the trailing edge of WR. 3stated during Hold and Halt modes.

READY (Input)

If Ready is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If Ready is low, the CPU will wait for Ready to go high before completing the read or write cycle.

RESET IN (Input)

Reset sets the Program Counter to zero and resets the Interrupt Enable and HLDA Flip-flops. None of the other flags or registers (except the instruction register) are affected The CPU is held in the reset condition as long as Reset is applied.

RESET OUT (Output)

Indicates CPU is being reset. Can be used as a system RESET. The signal is synchronized to the processor clock.

X1, X2 (Input)

Crystal or R/C network connections to set the internal clock generator X1 can also be an external clock input instead of a crystal. The input frequency is divided by 2 to give the internal operating frequency.

IO/M (Output)

IO/M indicates whether the Read/Write is to memory or I/O Tri stated during Hold and Halt modes.

Vcc: +5 volt supply.

Vss: Ground Reference.

2.1.4 8085 Instruction Format

An instruction is a command to the microprocessor to perform a given task on a Specified data. Each instruction has two parts: one is task to be performed, called the Operation code (opcode), and the second is the data to be operated on, called the Operand. The operand (or data) can be specified in various ways. It may include 8-bit (or 16-bit) data, an internal register, a memory location, or 8-bit (or 16-bit) address.

2.1.4.1 Instruction word size

The 8085 instruction set is classified into the following three groups according to Word size:

1. One-word or 1-byte instructions.
2. Two-word or 2-byte instructions.
3. Three-word or 3-byte instructions.

In the 8085, "byte" and "word" are synonymous because it is an 8-bit microprocessor.

2.2 Memory

Memory is the internal storage component of a Microprocessor, The amount is important in determining the software that can be used because each program requires a specific amount of memory to be functional.

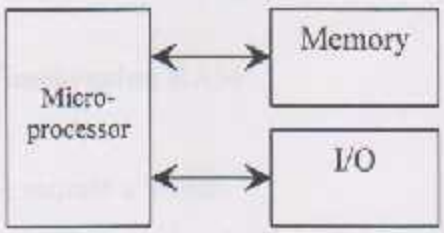


Figure 2-4: Memory

2.2.1 Random Access Memory (RAM)

All microprocessor systems need memory that can be both read from and written to. RAM memory is used to store dynamic data (that will change during the operation of the program).

2.2.2 Read Only Memory (ROM)

This is memory that can only be read, the data being stored in the memory device during its manufacture. And there are two types of ROM such as EPROM and EEPROM.

Erasable Programmable Read Only Memory (EPROM). This is similar to ROM type memory but the user can program it. The contents of the memory can be erased from the memory by exposing the memory chip to ultraviolet radiation for a short period of time. It can therefore be used many times over.

Electrically Erasable Programmable Read Only Memory (EEPROM). Similar to EPROM but has part or all of the memory contents erased by the microprocessor. So a typical microprocessor system will contain both ROM (could be EPROM, EEPROM, or ROM) to store the program code, and RAM to store dynamic data.

2.3 DS1643 Nonvolatile Timekeeping RAM

2.3.1 Why Nonvolatile Timekeeping RAM

1. Quartz accuracy ±1 minute a month.
2. BCD coded year, month, date, day, hours, minutes, and seconds.
3. Internal battery longevity.

The DS1643 is an 8K x 8 nonvolatile static RAM with afull function real time clock which are both accessible in a bytewide format. The device can also be easily substituted in ROM, EPROM and EEPROM sockets providing read/write nonvolatility and the addition of the real time clock function. The real time clock information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24 hour BCD format. Corrections for the day of the month and leap year are made automatically.

The RTC clock registers are double buffered to avoid access of incorrect data that can occur during clock update cycles. The double buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1643 also contains its own power-fail circuitry which deselects the device when the VCC supply is in an out of tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low VCC as errant access and update cycles are avoided.

2.3.2 Pin configuration

A0–A12 – Address Input

CE – Chip Enable

OE – Output Enable

WE – Write Enable

NC – No Connection

VCC – +5 Volts, GND – Ground

DQ0-DQ7 – Data Input/Output

Figure 2-5: IC 8255A

2.3.3 SETTING THE CLOCK

The 8–bit of the control register is the write bit. Setting the write bit to a one, like the read bit, halts updates to the DS1643 registers. The user can then load them with the correct day, date and time data in 24 hour BCD format. Resetting the write bit to a zero then transfers those values to the actual clock counters and allows normal operation to resume.

2.3.4 DS1643 REGISTER MAP – BANK

Table 2-1: ds1643 register map - bank

ADDRESS	DATA								FUNCTION	
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1FFF	–	–	–	–	–	–	–	–	YEAR	00–99
1FFE	X	X	X	–	–	–	–	–	MONTH	01–12
1FFD	X	X	–	–	–	–	–	–	DATE	01–31
1FFC	X	FT	X	X	X	–	–	–	DAY	01–07
1FFB	X	X	–	–	–	–	–	–	HOUR	00–23
1FFA	X	–	–	–	–	–	–	–	MINUTES	00–59
1FF9	$\overline{OSC}$	–	–	–	–	–	–	–	SECONDS	00–59
1FF8	W	R	X	X	X	X	X	X	CONTROL	A

$\overline{OSC}$ = STOP BIT R = READ BIT FT = FREQUENCY TEST
W = WRITE BIT X = UNUSED

CHAPTER

3

SENSOR AND DRIVERS

The following contents are going to be covered in this chapter:

CHAPTER THREE

SENSOR AND DRIVERS

3. 1 Infrared LED

3.1.1 Why Infrared LED

We use this chip as a sores of infrared signal , we chose infrared to avoid any effecting of another signal (other wavelength) on the receiver (photo transistor) .
We use LED because it gives continues wave and easy to build in a circuit, and it consume low power, cheep and available.

3.1.2 Construction of LED

The basic operation of the light-emitting (LED) is as follows. When the device is forward-biased, electrons cross the *pn* junction from the *n*-type material and recombine with holes in the *p*-type material. these free electrons are in the conduction band and at a higher energy level than the holes in the valence band. When recombination takes place, the recombining electrons release energy in the from of heat and light. As illustrated in Figure 3-1. Various impurities are added during the doping process to establish the wavelength determines the color of the light and if it is visible or invisible (infrared).

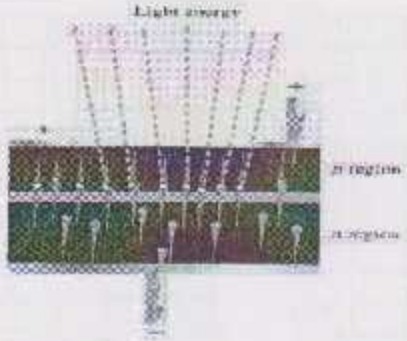


Figure 3-1: electroluminescence in a forward-biased LED

Semiconductive Materials: LEDs are made of gallium arsenide (GaAs), gallium arsenide phosphide (GaAsP), or gallium phosphide (GaP). Silicon and germanium are not used because they are essentially heat-producing materials and are very poor at producing light. GaAs LEDs emit infrared (IR) radiation, which is nonvisible, GaAsP produces either red or yellow visible light, and GaP emits red or green visible light. LEDs that emit blue light are also available. Red is most common.

3.1.3 Light Emission Diode

The wavelength of light determines whether it is visible or infrared. An LED emits light over a specified range of wavelengths as indicated by the spectral output curves in Figure 3-2. The curves in part (a) represent the light output versus wavelength for typical visible LEDs, and the curve in part (b) is for typical infrared LED. The wavelength (λ) is expressed in nanometers (nm). The normalized output of the visible red LED peaks at 660 nm, the yellow at 590 nm, green at 540 nm, and blue at 460 nm. The output for the infrared LED peaks at 940 nm.

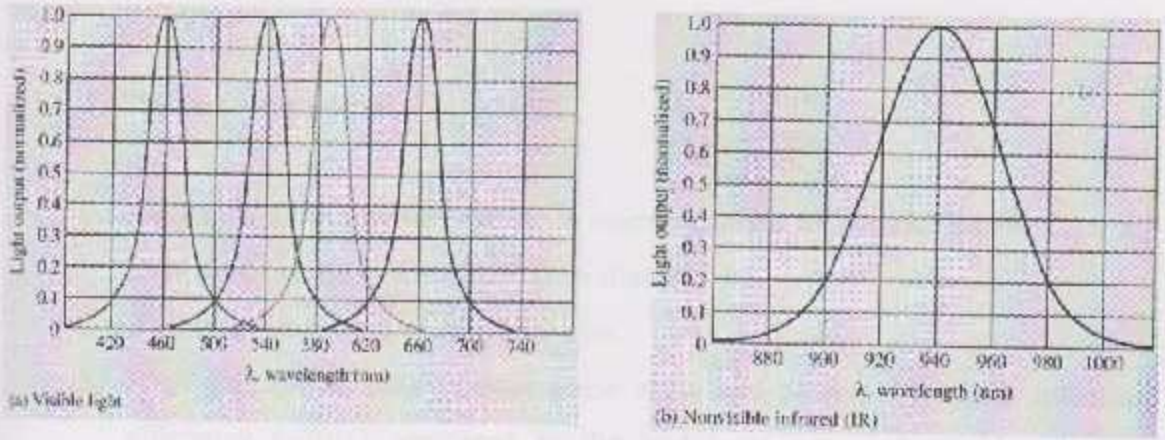


Figure 3-2: typical spectral output curves for LEDs

The graph in Figure 2-7 is radiation pattern for a typical LED. It shows how directional the emitted light is. The radiation pattern depends on the type of lens structure of the LED. The narrower the radiation pattern, the more the light is concentrated in a particular direction. Also, colored lenses are used to enhance the color.

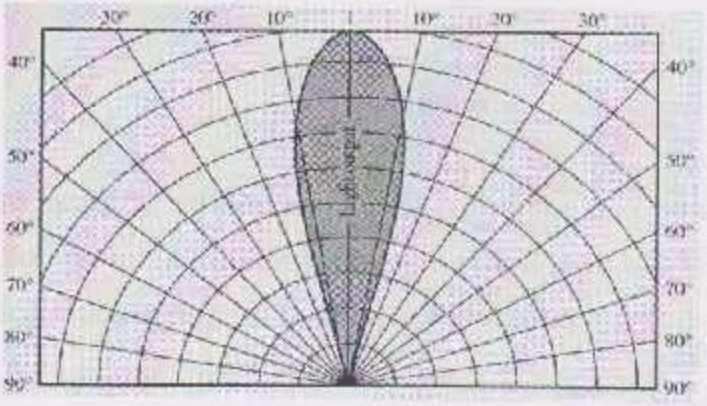


Figure 3-3: general radiation pattern of typical LED

3.2 Phototransistor

3.2.1 Why phototransistor

1. Easy to build in interface circuit to microprocessor as infrared receiver, and all component needs in this circuit is available.
2. Phototransistor work as amplifier also.
3. High gain (up to 3000), lower noise equivalent power, and higher quantum efficiency (~70%) compared to the traditional extended wavelength PIN photodiodes.
4. Doesn't effect expect the signal wavelength which out from the LED (infrared) phototransistor available and cheep.

3.2.2 Phototransistor basic operation

The relationship between the collector current and the light-generated base current in a phototransistor

$$Ic = \beta_{DC} I_b$$

The larger the physical area of this region, the more base current is generated. Thus, a typical phototransistor is designed to offer a large area to the incident light, as the simplified structure diagram in figure 3-4 illustrates.

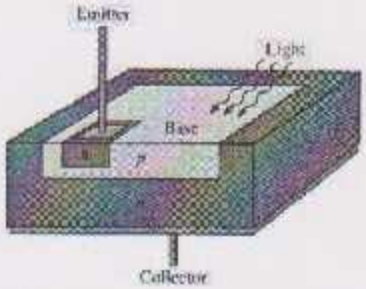


Figure 3-4: phototransistor chip structure

A phototransistor can be either a two-lead or three-lead device. The three-lead configuration, the base lead is brought out so that the device can be used as a conventional BJT or without the additional light-sensitivity feature. In two-lead configuration, the base is not electrically available, and the device can be used only with light as the input. In many applications, the phototransistor is used in the two-lead version. Figure 3-5 shows a phototransistor typical collector characteristic curve. Notice that each individual curve on the grave corresponds to certain value of light intensity (in this case, the units are Mw/cm2) and that the collector current increases with light intensity.

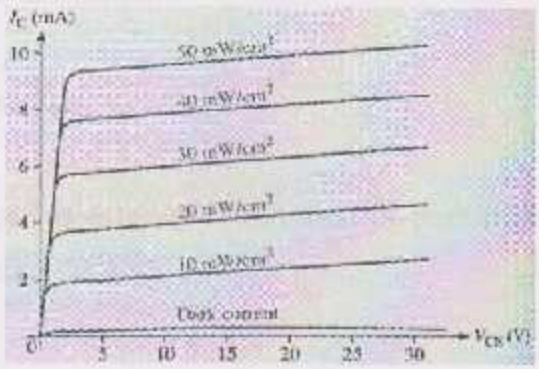


Figure 3-5: collector characteristic curve

Phototransistors are not sensitive to all light but only to light within a certain range of wavelength. They are most sensitive to particular wavelengths, as shown by the peak of the spectral response curve in figure 3-6.

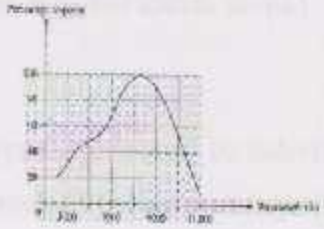


Figure 3-6: Phototransistors spectral response

3.3 Keypad

3.3.1 Why keypad

1. Simple to interface with a microprocessor.
2. Insure the security that we need in our project can't be masked easily.
3. Also there is available IC that converts the output of keypad to 4bit digit (hex decimal) that makes deal with keypad easily.
4. A keypad is a convenient way of entering data into the 8085 without tying up one I/O line for each switch.

3.2.2 Keypad configuration

But The keypad is actually a collection of push-buttons, organized into a matrix. It looks like this:

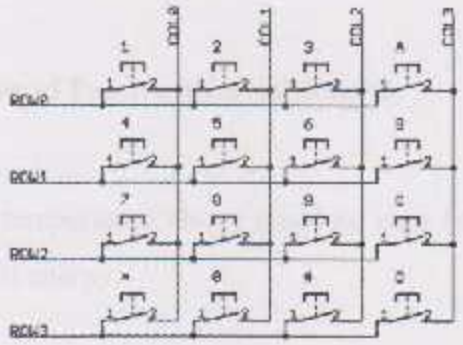


Figure 3-7: 4×4 matrix keypad

A 4 row by 4 column keypad consists of 16 individual push buttons, but only needs 8 I/O lines to determine which of the sixteen keys has been pressed Figure 3-7 Shows 4×4 matrix.

3.4 Passive infrared detector (PIR)

3.4.1 Why Passive infrared detector

1. Cover a wide area.
2. Good sensitivity to any movement in the room.
3. Finally it easy to interface with the microprocessor.

Figure 3-8: Passive infrared detectors

3.4.2 Theory and Operation of Passive infrared detector

Any object with a temperature above absolute zero (virtually every object, therefore), radiates infrared energy.

Passive infrared (PIR) detectors do not generate an energy, passive infrared detectors are designed to make use of infrared energy which virtually all objects generate. The detector ignores all gradual fluctuations of temperature caused by sunlight, heating systems, and air conditioners. A typical PIR detector can monitor an area of about 6 x 9 meters or a narrow hallway about 15 meters long. It doesn't penetrate walls (or anything else).

Using a lens or mirrors to determine coverage patterns, the detector focuses the radiated energy on the sensor face. The area of coverage of a PIR device may be adjusted using circuitry built into the detector. In addition, such detectors have an externally mounted LED which provides a visual indication that the device is functioning.

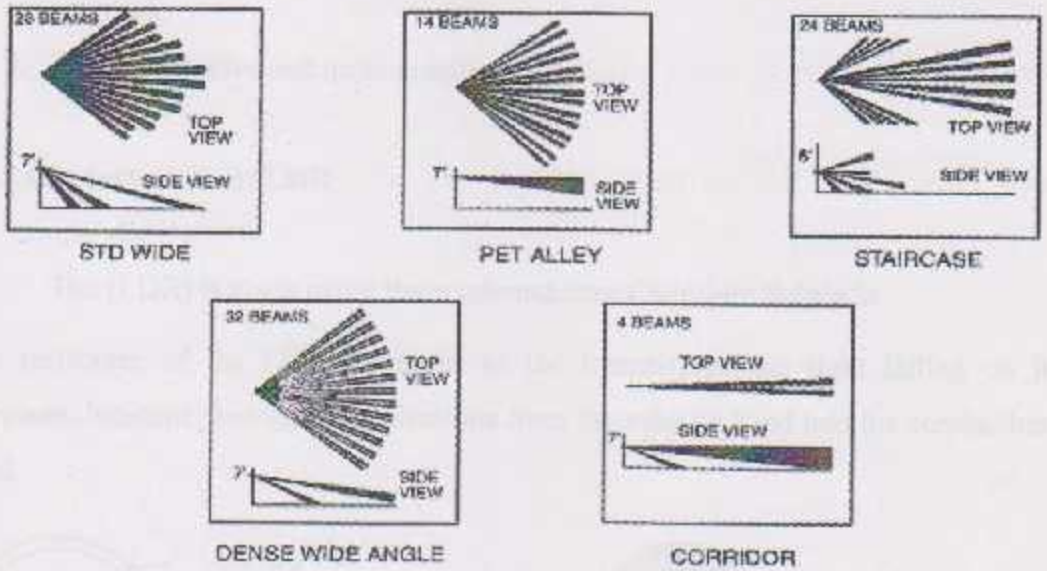


Figure 3-9: Passive infrared detector beams

3.5 Light Dependant Resistors (LDR)

3.5.1 Why LDR

1. Has the property that its resistance decreases when the light level increases.
2. The resistance can change by a factor of 100 or more when exposed to light and dark.
3. It is inexpensive and quite sensitive.

3.5.2 Characteristic of LDR

The (LDR) is made using the semiconductor Cadmium Sulphide.

The resistance of the LDR decreases as the intensity of the light falling on it increases. Incident photons drive electrons from the valency band into the conduction band.

Figure 3.10: (a) Structure of a Light Dependent Resistor (b) Cadmium Sulphide track and an atom to illustrate electrons in the valence and conduction bands.

This resistance can change by a factor of 100 or more when exposed to light a dark, typical use is on top of a lamppost to turn the street light on and off depending on the light level. Photo Diodes are used when a quick response is required, as LDR's are slow to respond.

3.6 Limit Switches

3.6.1Characteristic of Limit Switches

1. Mechanical limit switches often called "micro switches"
2. A variety of sensors are available that give ON/OFF (or yes/no) binary outputs.
3. activation causes electrical contacts to either "break" ("normally closed" or NC switch) or "make" ("normally open" or NO switch) -or both NC and NO.
4. More sophisticated binary sensors are collectively known as proximity switches.

3.6.2 Standard Basic Switches:

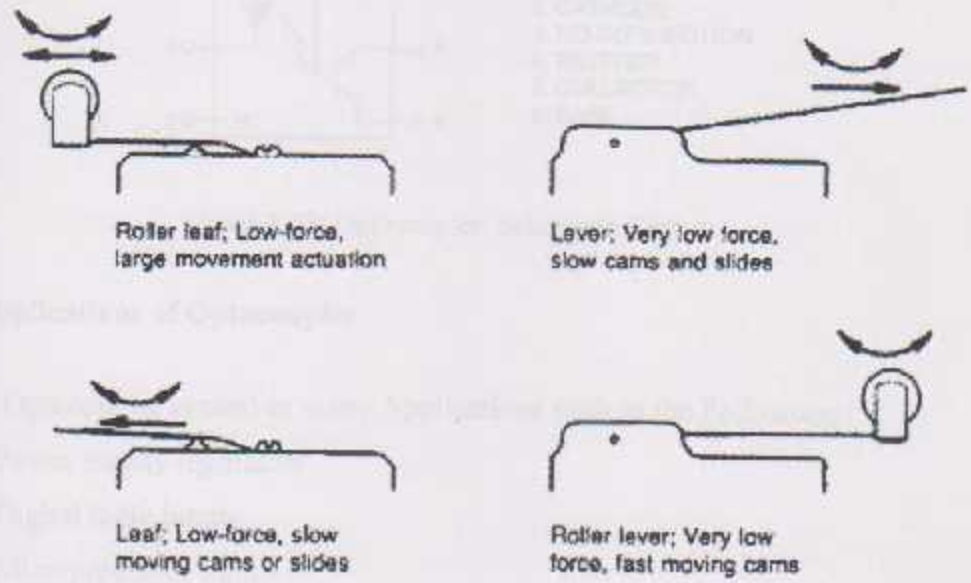


Figure 3-11: Standard Basic Switches

3.6.3 Switch Contact Configurations:

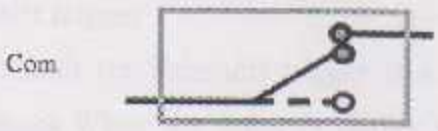


Figure 3-12: Switch Contact

3.7 Optocoupler 4N25

The general purpose optocouplers consist of a gallium arsenide infrared emitting diode driving a silicon phototransistor in a 6-pin dual in-line package, Figure 3-13 Show the schematic Circuit of 4N25 Optocoupler.

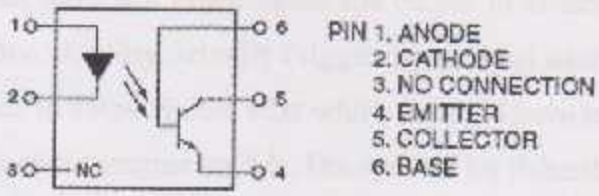


Figure 3-13: Optocoupler, Schematic Circuit.

3.7.1 Applications of Optocoupler

The Optocoupler is used in many Applications such as the Following:

1. Power supply regulators
2. Digital logic inputs
3. Microprocessor inputs

3.8 Schmitt trigger

A Schmitt (or Schmidt) trigger is a comparator circuit that incorporates positive feedback.When the input is higher than a certain chosen threshold, the output is high; when the input is below another (lower) chosen threshold, the output is low; when the input is between the two, the output retains its value. The trigger is so named because the output retains its value until the input changes sufficiently to trigger a change. This dual threshold action is called hysteresis, and implies that the Schmitt trigger has some memory.

The benefit of a Schmitt trigger over a circuit with only a single input threshold is greater stability (noise immunity). With only one input threshold, a noisy input signal near that threshold could cause the output to switch rapidly back and forth from noise alone. A noisy Schmitt Trigger input signal near one threshold can cause only one switch in output value, after which it would have to move to the other threshold in order to cause another switch .The symbol for Schmitt triggers in circuit diagrams is a triangle with a hysteresis symbol in figure 3-14.

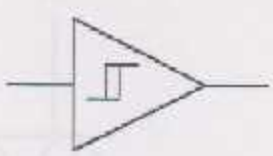


Figure 3-14: symbol of Schmitt trigger

We use Schmitt trigger inverter in many circuits to obtain digital pulse from sensor as will describe in other section.

3.9 TRIAC

A **TRIAC** or **Triode for Alternating Current** is an approximately equivalent to two silicon-controlled rectifiers (SCRs/thyristors) joined in inverse parallel (paralleled but with the polarity reversed) and with their gates connected together. These results in a bidirectional electronic switch which can conduct current in either direction when it is triggered (turned on). It can be triggered by either a positive or a negative voltage being applied to its gate electrode.

Once triggered, the device continues to conduct until the current through it drops below a certain threshold value, such as at the end of a half-cycle of alternating current (AC) mains power. This makes the TRIAC a very convenient switch for AC circuits, allowing the control of very large power flows with milliampere-scale control currents. In addition, applying a trigger pulse at a controllable point in an AC cycle allows one to control the percentage of current that flows through the TRIAC to the load

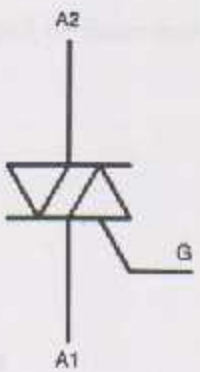


Figure 3-15: symbol of triac

3.10 Motors

3.10.1 Why single-phase motors are different

Most homes and rural areas are supplied with single-phase ac electrical power. Consequently, most electrical home appliances and electrically driven farm machines employ single-phase motors. They drive washing machines, refrigeration and air-conditioning compressors, grain dryers, fans, pumps, sewing machines, vacuum cleaners, clocks, phonographs, hand tools, and so on. Literally millions of single-phase motors are manufactured each year.

The difficulty with single-phase as a power source for motors is that it dose not lend itself to producing a rotating magnetic field. the magnetic filed set up by a single phase winding. It "breathes"; that is, it dose not move around the air gap but remains stationary as it oscillates in magnitude and polarity. This pulsating filed, acting alone, dose not produce starting torque.

Several schemes have been developed to circumvent this difficulty. Each results in a motor with specific characteristics suitable to a certain range of uses. This chapter discusses the most important of these motor types.

3.10.2 Why Induction Motors

- Low Initial Cost
- Simple & Efficient Operation
- Compact Size – cubic inches/Hp
- Long Life – 30,000 to 50,000 hours
- Low Noise
- Withstand high temporary overloads

3.10.3 Motor Parts

- Enclosure
- Stator
- Rotor
- Bearings
- Conduit Box
- Eye Bolt

Figure 3-16: Motor Parts

3.10.4 Capacitor motors

Capacitor motors are single-phase induction motors that employ a capacitor in the auxiliary-winding circuit to cause a greater phase split between the currents in the main and auxiliary winding.

3.10.5 Two -value capacitor motors

The impedances of both the main and auxiliary windings vary with motor speed .by the use of two capacitors, however, it is possible to achieve balanced, two-phase operation of the motor at starting and at one other speed, if the auxiliary winding remains connected. The speed chosen would be close to that at which rated horsepower is developed, say , at about 80 percent of rated horsepower. The auxiliary winding must be designed for continuous operation .

The circuit for a two-value capacitor motor is shown in figure 3-17 the two capacitor are connected in parallel at starting. The starting capacitor is almost always electrolytic. The running capacitor must handle alternating current continuously ,and is usually of oil-filled paper construction. Running capacitors contribute considerably to the cost of these motors.

Two-value capacitor motor motors are quiet and smooth running. They a higher efficiency than motors that run on the main winding alone. A still higher

efficiency is possible if the capacitor is connected in series with the main winding rather than the possible if the capacitor is connected in series with the main winding rather than the auxiliary winding, but the capacitor required is very large and prohibitively expensive.

3.10.6 Capacitor Start-Run Motor

Advantage of Capacitor Start-Run Motor

1- Larger single phase motors up to 10 Hp.

2- Good starting torque less than (cap start) with lower starting current.

3- Higher cost than cap start.

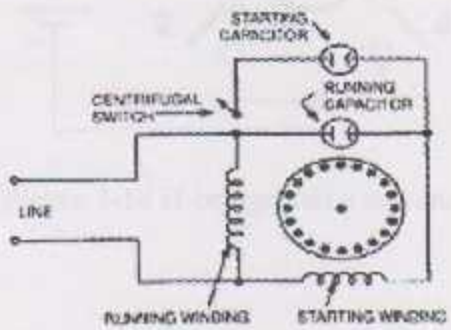


Figure 3-17: Capacitor Start-Run Motor

3.11 Driving circuit

When using a microprocessor as a controller, an interfacing circuit is needed to drive a motor, so that the motor power is supplied from power source different from the source of controller. This interfacing circuit can be implemented in a variety of technologies such as bipolar transistors, and if reversing of motor is needed this interfacing is known as H-bridge and is usually consists of four switches connected in the topology of an H as shown in figure 3-18.

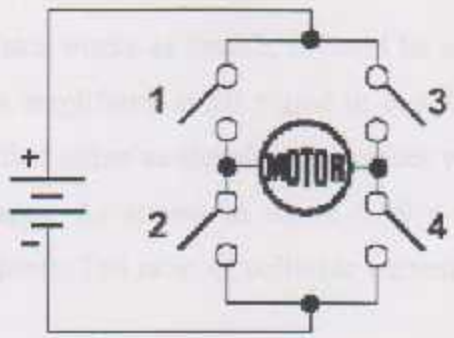


Figure 3-18 H-bridge using switches

3.11.1 H-bridge

In an H-bridge, all the switches are opened and closed so as to put a voltage of one polarity across the motor for current to flow through it in one direction, or a voltage of the opposite direction, causing current to flow through the motor in opposite direction for reverse rotation.

Transistor is dipolar junction; simply it two PN junction (two diodes). There are two possible combination of two PN junctions, NPN or PNP as shown in figure ()

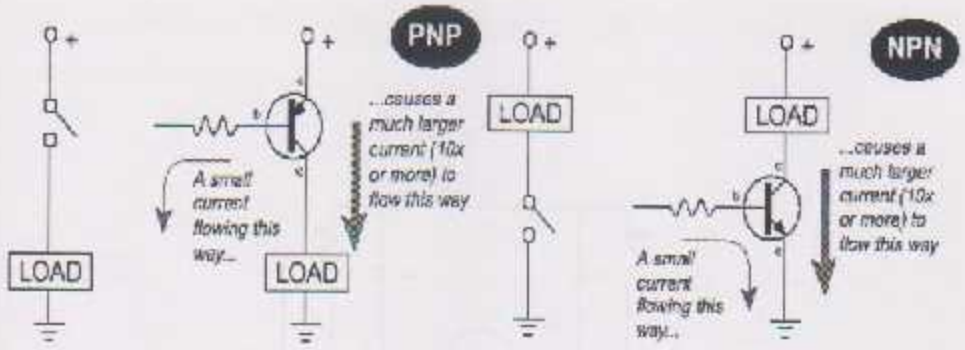


Figure 3-19 PNP and NPN transistors

Beside the transistor works as switch, it could be used as linear amplifier to add gain to a circuit for amplifying small signal to match it with a higher power. Transistors can be classified either as signal-level devices which capable of handling large currents and voltages. As shown in figure 3-19 a transistor has 3-terminal (collector, base, and emitter). The ratio of collector current to be base current is the current gain (β)

$$\beta = Ic/IB$$

Where:

IC is the current pass through the collector.

IB is the current applied to the base of the transistor.

Let's note that the voltage VCE is the voltage drop between the collector and the emitter. When VCE is small (approach zero) the transistor is work in saturation and then the transistor works as switch.

Now, to implement the H-bridge using NPN transistor the circuit will be as shown in figure 3-19. Sometimes instead of using single transistor we could use what is called Darlington transistor which is small transistor combined to large transistor, the result being equivalent to a large transistor with large amplification factor.

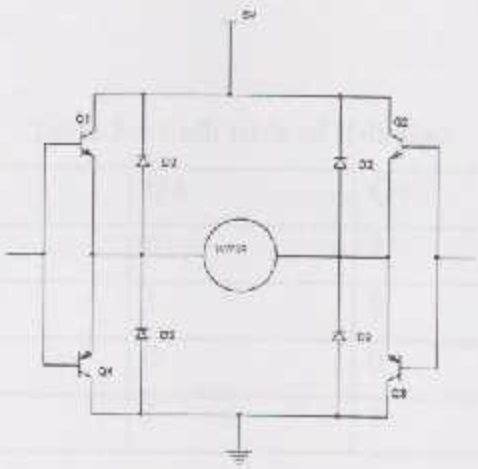


Figure 3-20 H-bridge using transistors.

Now, to turn the motor in a direction, a signal is applied to the base of Q1, and Q4 and so the tow transistor (switches) will pass Ic to the motor and then to the ground, and to turn the motor in the other direction the signal is applied to the base of Q2 and Q3.

Noting that Ic=Ia then the required β=Ic/IB, and according to Ia and β the transistor selected.

Generally, for inductive load such as a motor, when it switched off, the energy present in the magnetic field induces a current on the winding. These are in reverse polarity with respect to the supply current. When a motor is switched off, a diode in parallel shorts these reverse induced current, so the diode creates a return path for the current. It should add diodes to catch the back voltage that generated by the motor's coil when the power is switched on and off. If the diodes are not used, the transistors will burn out.

According for table3-1, the upper left and lower right transistors figure3-20 turn on, then the power flows through the motor forward, i.e:1 to Q1, 0 to Q2, 0 to Q3 and 1 to Q4.

Table 3-1 truth table of H-bridge.

Q1	Q2	Q3	Q4	Function
1	0	0	1	Forward
0	1	1	0	Reverse
1	1	0	0	Brake
0	0	1	1	Brake

Then for reverse, the upper right and lower left transistors figure turn on, then the power flows through the motor reverse, i.e.: 0 to Q1, 1 to Q2, 1 to Q3 and 0 to Q4.

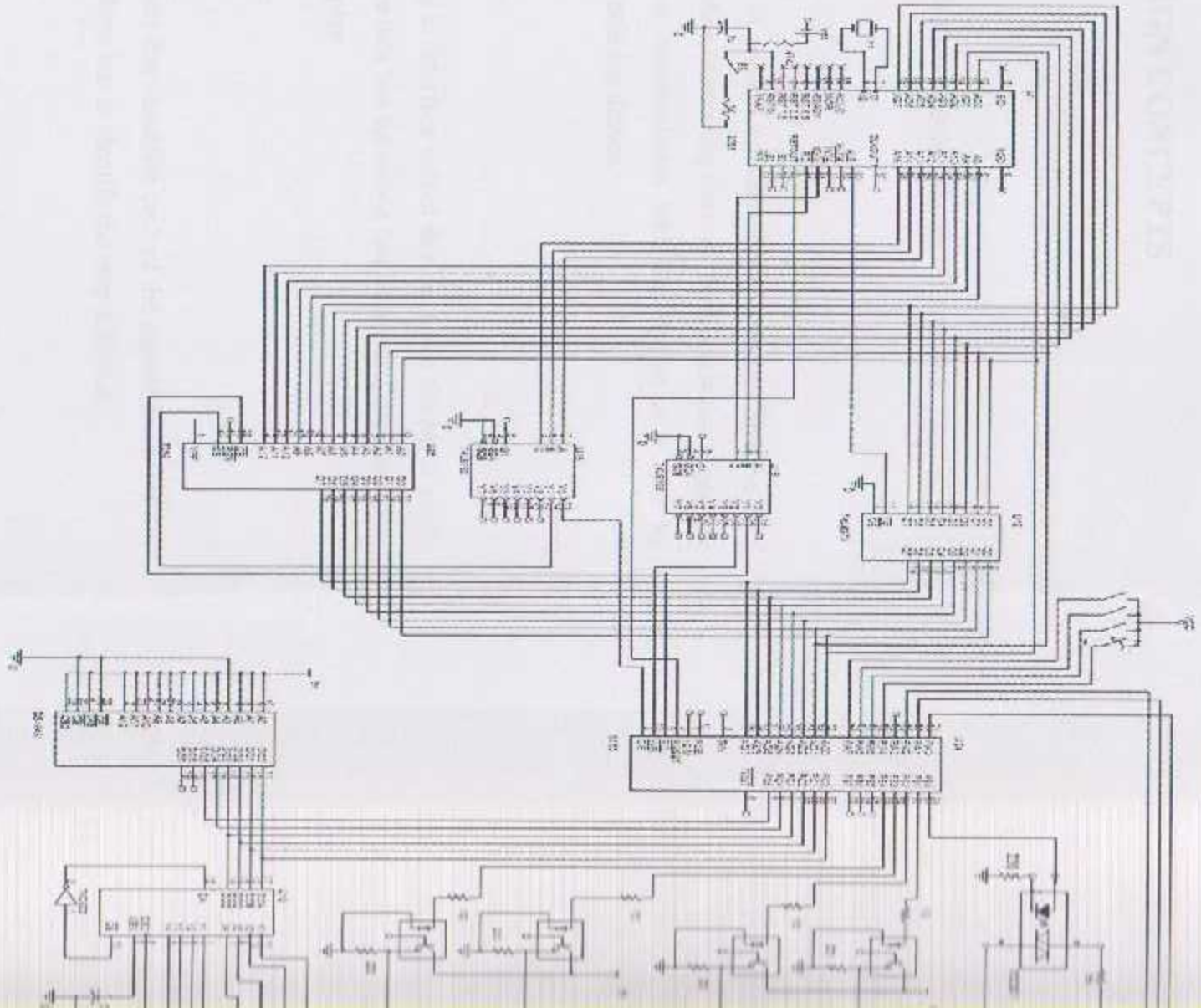
If the two upper transistors turn on, the motor resist turning, so we effectively have a braking mechanism. The same is true if both lower transistors turn on.

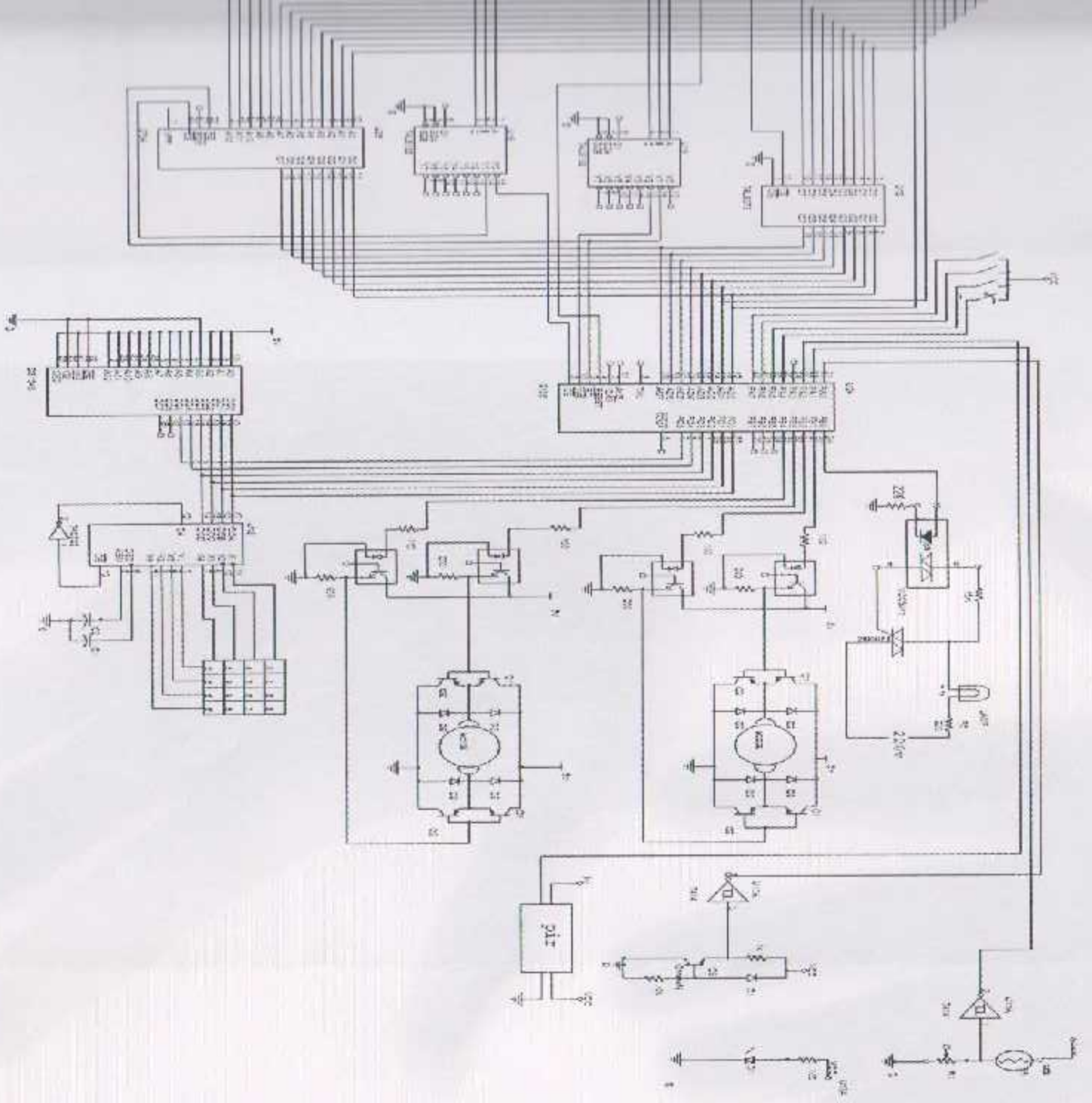
CHAPTER

4

DESIGN CONCEPTS

The following contents are going to be covered in this chapter:





CHAPTER FOUR

DESIGN CONCEPTS

4.1 Schematic design

The final design of controlled room project shown if figure: 4.1.

4.1.1 Tri-state buffer

Peripherals are connected in parallel between the address bus and the data bus. However, because of the tri-state interfacing devices. Peripherals don't load the system buses. The microprocessor communicates with one device at a time by enabling the tri-state line of the interfacing device.

4.1.2 Latch

A Latch is used commonly to interface output device, when the MPU sends an output , data are available on the data bus for only a few microseconds; therefore , a Latch is used to hold data for display.

4.1.3 Decoder

The decoder is a logic circuit that identifies each of the signals present at it's input, also it used to decode on address bus to identify the output device.

4.1.4 Control signal and address demultiplexing

To input "read" or output "write" data in or out of microprocessor, we need to give address of the ship and control signal.
The address consist of 16-bit , the low-order address bus in microprocessor multiplexed with data bus (AD0-AD7), the Latch 74LS373 and ALE signal use to demultiplexed address and data.

4.1.5 Generating control signal

Control signals are generating by combining the signal RD,WR and IO/M, because we use memory map only combine RD,WR and M using negative NAND gates, when both inputs signals go low, the output of the gates go low and generate MEMR (memory read) and MEMW (memory write) .

4.1.6 Memory address decoding

For the EPROM2732 and DS1643 , the process of addresses decoding should result identifying a register for a given address.
We should be able to generate unique pulse for a given address, as shown in figure:4-3 - 12 address line (A11-A0) are connected to the memory ship, and remaining four address lines (A15-A12) of the 8085 connect with decoder 74LS138.
A14, A13 and A12 are the input of the decoder, and A15 use as enable, the output of the decoder (Y0, Y1) in memory address connect directly with enable pin of EPROM2732 and DS1643 .

4.1.7 Interface peripheral address decoding

Peripheral address decoding differ than memory address decoding, (A11-A0) are don't care but (A15-A12) are the same (connect with decoder 74LS138) , the output of the decoder (Y2, Y3) combine with the control signal (MEMW, MEMR) to enable Latch 74LS373 and puffer 74244 , the two signal should be low to enable one chip a time.

4.2 Sensors circuit

When the buffer enabled the data transfer from sensors circuit to the data bus of the microprocessor , and the description of sensor circuit is :

1-LDR circuit

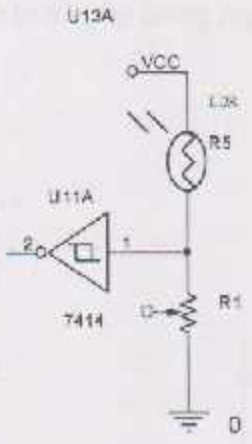


Figure 4-2: LDR

The output of the figure 4-1, is digital (pulse) because of using Schmitt trigger inverter, the input voltage of Schmitt trigger is proportional to the value of LDR resistance which dependent to the light incident to it.

The input voltage to Schmitt trigger inverter using divider rule is:

Vin = Vcc*Rpot/ (Rpot+Rldr).

Where:

Vin: the voltage input to Schmitt trigger.

Vcc: bias voltage.

Rpot: the resistance of potentiometer.

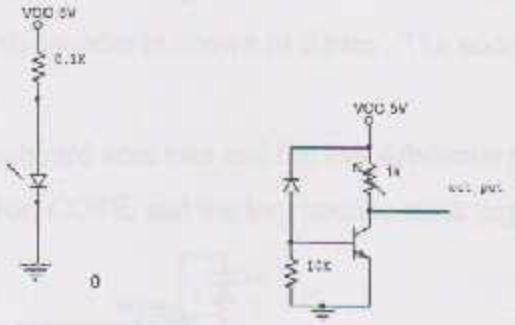
RLDR : the resistance of photo resistance.

When Vin grater or equal 1.7v the output voltage of Schmitt trigger is low (nearly 0v), if Vin equal 0.8v or less the output voltage of Schmitt trigger is high (3.4v).

2- PIR detector:

If the PIR detector doesn't sense any movement, the output is 0V, if it sense a movement the output is 12V, but Microprocessor deal with 5V, so we must reduce the voltage out from PIR detector to 5V, by using regulator 7805.

3- IR sensor



(a) (b)

Figure 4-3: IR sensor

a-) transmitter: the transmitter circuit consists of limit resistor and IR LED as shown in figure 4-5 which emits continuous signal to the receiver, which located in straight line together.

b-) receiver: the receiver circuit consist of photoled and transistor as shown in figure ,the receiver element is photoled ,as known the reverse current of photoled increase as infrared signal incident to it increase ,this current very small so its necessary to amplify the current ,this amplification maintains by using transistor .

We get the output from the collector of transistor, when the reverse current of photoled is large enough the transistor will be on so that the output voltage is 0v, and if the reverse current of photoled is very small the transistor will be of, so that the output voltage is 5v.

4-Keypad

The MM74C922 Keyboard Encoders implement all the logic necessary to interface a 16 key switch matrix to a microprocessor.

The connection of keypad with encoder is shown in figure . The encoder will convert a key switch closer to a 4 bit.

capacitors control both the keyboard scan rate and the key debounce period by altering, the oscillator capacitor, COSE, and the key bounce mask capacitor, CMSK.

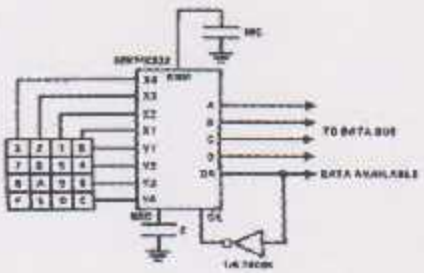


Figure 4.4: Keypad

CHAPTER

5

SOFTWARE SYSTEM AND ASSEMBLERS

The following contents are going to be covered in this chapter:

CHAPTER FIVE

SOFTWARE SYSTEM AND ASSEMBLERS

5.1 Introduction

Each machine has its own set of instruction based on the design of its Microprocessor , To communicate with the computer, one must give instructions in binary language (**machine language**), Because it is difficult for most people to write programs in sets of 0's and 1's, computer manufactures have devised English-like words to represent the binary instructions of a machine. Programmers can write programs, called **assembly language** programs, using these words. Because an assembly language is specific to a given machine.

8085 Machine Language, The 8085 is a microprocessor with 8-bit word length: its instruction set (or language) is designed by using various combinations of these eight bits. The 8085 is an improved version of the earlier processor 8085A, an instruction is a binary pattern entered through an input device in memory to command the microprocessor to perform that specific function.

8085 Assembly Language, Even though the instructions can be written in hexadecimal code, it is still difficult to understand a program written in hexadecimal numbers. Therefore, each manufacture of a microprocessor has devised a symbolic code for each instruction, called a mnemonic, (The word mnemonic is based on the Greek word meaning mindful; that is, a memory aid.) The mnemonic for a particular instruction consists of letters that suggest the operation to be performed by that instruction.

5.2 Flow Chart

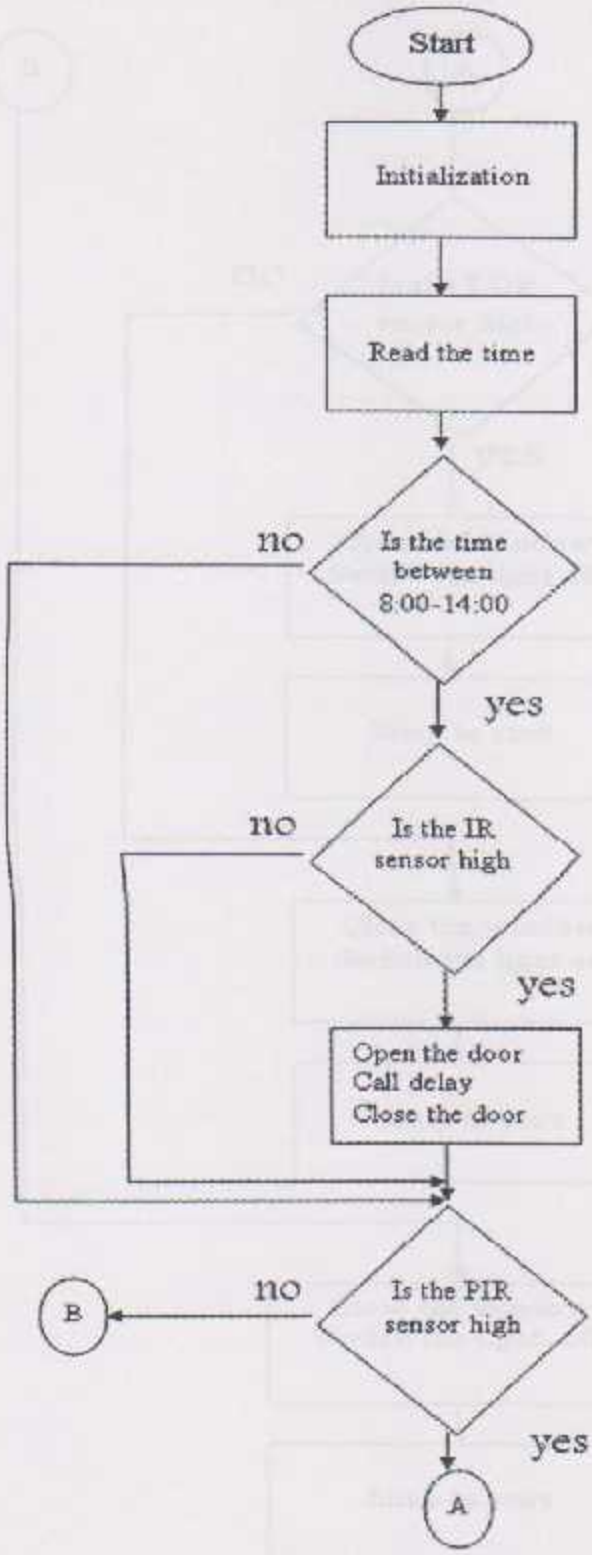
The program of the partial controlled room:

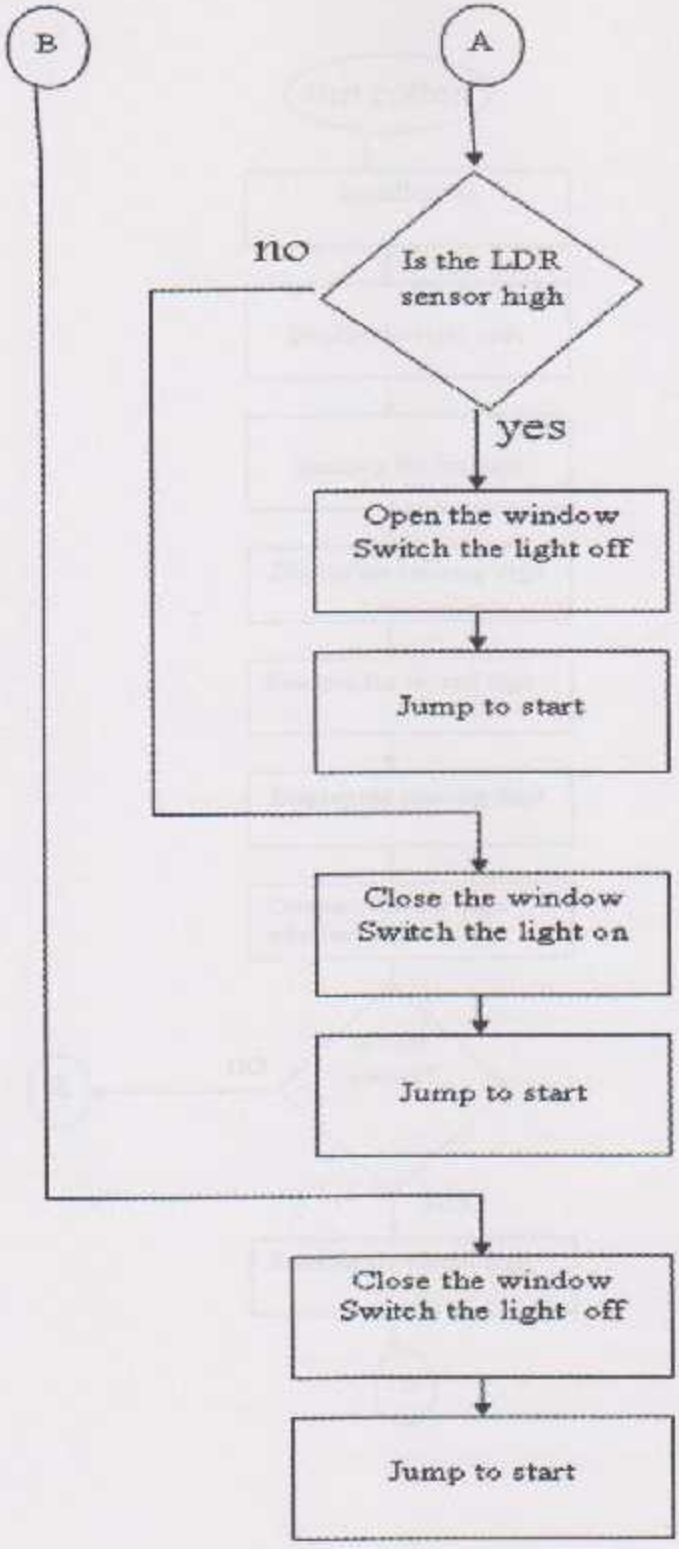
1- Initialize the critical hour we need and Code Number that contains 4-digits from the keypad, and showing the code on the display (address field of the MC-1).

2- Read the time , sensors and keypad and process it.

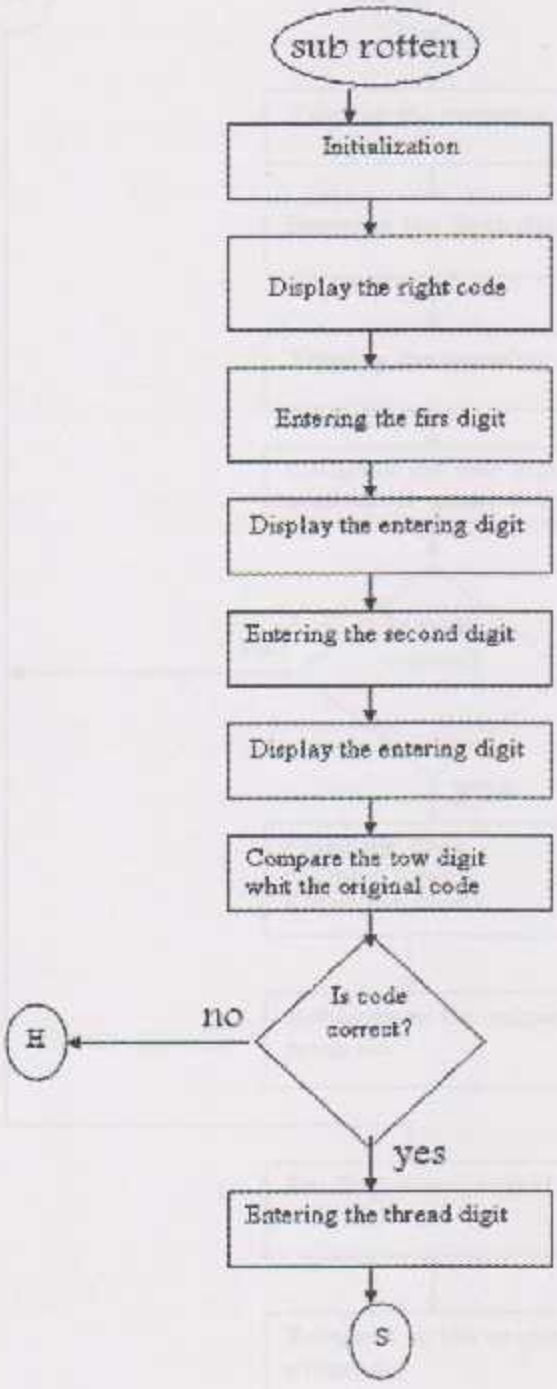
3- Output the result of processing.

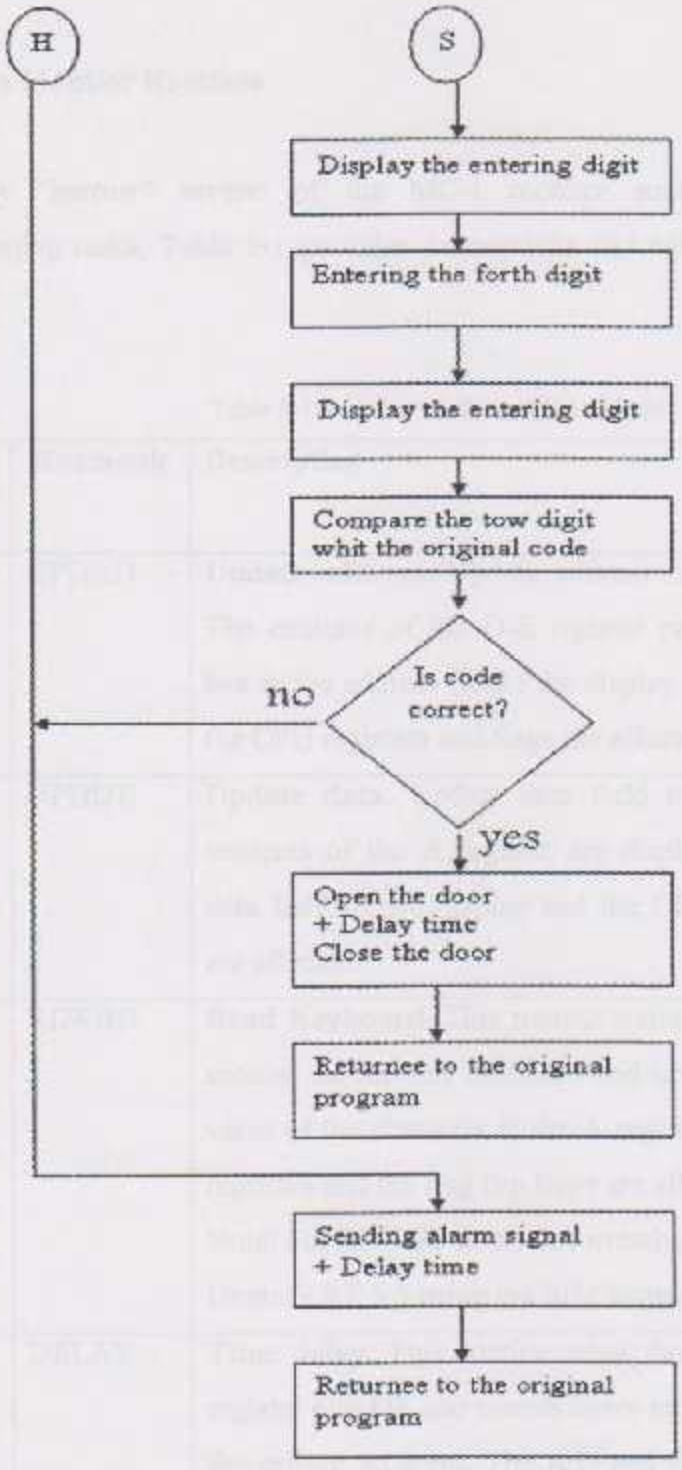
The flowchart of the Microprocessor programming that's illustrates in the above steps are shown in the Figure (5.1).


Start
Initialization
Read the time
Is the time between 8:00-14:00
no
yes
Is the IR sensor high
no
yes
Open the door
Call delay
Close the door
Is the PIR sensor high
no
yes
B
A


B
A
no
Is the LDR sensor high
yes
Open the window
Switch the light off
Jump to start
Close the window
Switch the light on
Jump to start
Close the window
Switch the light off
Jump to start

The flow chart of sub rotten is illustrated in figure 5-2 below.




H
S
Display the entering digit
Entering the forth digit
Display the entering digit
Compare the tow digit whit the original code
Is code correct?
no
yes
Open the door
+ Delay time
Close the door
Returnee to the original program
Sending alarm signal
+ Delay time
Returnee to the original program

5.3 Assembly Language Programming

Access to Monitor Routines

We may "borrow" several pf the MC-1 monitor routines to simplify our programming tasks, Table 5-1 provides descriptions and calling address for theses routines.

Table 5-1: Monitor routine calling address

Calling address	Mnemonic	Description
0363	UPDAD	**Update address.** Update address field of the display. The contents of the D-E register pair are displayed in hex in the address field f the display. The contents of all the CPU registers and flags are affected.
036E	UPDDT	**Update data.** Update data field of the display. The contents of the A register are displayed in hex in the data field of the display and the CPU condition codes are affected.
02E7	RDKBD	**Read Keyboard.** This routine waits until a character is entered on the hex keyboard and upon return place the value of the character in the A register. The A, H and L registers and the flag flip flops are affected. Note: For RDKBD to work correctly, you must first: Unmask RT 5.5 using the SIM instructions.
05F1	DELAY	**Time delay.** This routine takes the 16-bit contents of register pair DE and counts down to zero. The returns to the calling program. The A,D and E registers and flags are affected

Table 5.2: Assembly Language Programming.

address	Instructions Set	
2000	MVI B 08	Set the clock
2001		
2002	MVI C 14	
2003		
2004	MVI A 02	initialization
2005		
2006	OUT 20	
2007		
2008	IN 23	Read the time
2009		
200A	ANI 3F	
200B		
200C	MOV H A	
200D	SUB B	
200E	JC 2035	
200F		
2010		
2011	MOV A H	
2012	SUB C	
2013	JNZ 2035	
2014		
2015		
2016	IN 21	
2017		
2018	ANI 01	Read the IR
2019		

201A	JZ 2035	
201B		
201C		
201D	OUT 22	Open the door
201E		
201F	LXI D FFFF	Daly time
2020		
2021		
2022	CALL05F1	
2023		
2024		
2025	LXI D FFFF	
2026		
2027		
2028	CALL05F1	
2029		
202A		
202B	MVI A 02	
202C		
202D	OUT 22	
202E		
202F	LXI D FFFF	
2030		
2031		
2032	CALL05F1	
2033		
2034		
2035	IN 21	

2036		
2037	ANI 04	Read the PIR
2038		
2039	JZ 205D	
203A		
203B		
203C	IN 21	
203D		
203E	ANI 02	Read the LDR
203F		
2040	JZ 2050	
2041		
2042		
2043	MVI A 18	
2044		
2045	OUT 22	Close the window
2046		
2047	LXI D FFFF	
2048		
2049		
204A	CALL05F1	
204B		
204C		
204D	JMP 2000	
204E		
204F		
2050	MVI A 04	
2051		

2052	OUT 22	Light off
2053		
2054	LXI D FFFF	
2055		
2056		
2057	CALL05F1	
2058		
2059		
205A	JMP 2000	
205B		
205C		
205D	MVI A 08	
205E		
205F	OUT 22	Light on
2060		
2061	LXI D FFFF	
2062		
2063		
2064	CALL05F1	
2065		
2066		
2067	JMP 2000	
2068		
2069		

20CE	LXI SP20B0	initialization
20CF		
20D0		

20D1	MVI A 08	
20D2		
20D3	SIM	Set the interrupt
20D4	MVI D 12	Set the code
20D5		
20D6	MVI E 12	
20D7		
20D8	CALL0363	Display the code
20D9		
20DA		
20DB	LXI D FFFF	
20DC		
20DD		
20DE	CALL05F1	
20DF		
20E0		
20E1	MVI D 00	
20E2		
20E3	MOV E D	
20E4	CALL02E7	Enter the first digit
20E5		
20E6		
20E7	RLC	
20E8	RLC	
20E9	RLC	
20EA	RLC	
20EB	MOV D A	
20EC	PUSH D	

20ED	CALL0363	Display first digit
20EE		
20EF		
20F0	POP D	
20F1	CALL02E7	Enter second digit
20F2		
20F3		
20F4	ORA D	
20F5	PUSH D	
20F6	CALL0363	Display second digit
20F7		
20F8		
20F9	POP D	
20FA	MVI H 20	
20FB		
20FC	MVI L 90	
20FD		
20FE	MOV A D	
20FF	CMP M	Compare the first tow digit
2100	JNZ 2143	
2101		
2102		
2103	CALL02E7	Enter the third digit
2104		
2105		
2106	RLC	
2107	RLC	
2108	RLC	

2109	RLC	
210A	MOV E A	
210B	PUSH D	
210C	CALL0363	Display the third digit
210D		
210E		
210F	POP D	
2110	CALL02E7	Enter the fourth digit
2111		
2112		
2113	ORA E	
2114	PUSH D	
2115	CALL0363	Display the fourth digit
2116		
2117		
2118	POP D	
2119	MVI H 20	
211A		
211B	MVI L 90	
211C		
211D	MOV A E	
211E	CMP M	Compare the last tow digit
211F	JNZ 2143	
2120		
2121		
2122	MVI A 0D	
2123		
2124	OUT 20	

2125		
2126	MVI A 01	
2127		
2128	OUT 22	Open the door
2129		
212A	LXI D FFFF	
212B		
212C		
212D	CALL05F1	
212E		
212F		
2130	LXI D FFFF	
2131		
2132		
2133	CALL05F1	
2134		
2135		
2136	MVI A 02	
2137		
2138	OUT 22	Close the door
2139		
213A	LXI D FFFF	
213B		
213C		
213D	CALL05F1	
213E		
213F		
2140	JMP 2000	Return to the main program

```
2141
2142
2143    MVI A 80
2144
2145    OUT 22          Alarm on
2146
2147    LXI D FFFF
2148
2149
214A    CALL05F1
214B
214C
214D    LXI D FFFF
214E
214F
2150    CALL05F1
2151
2152
2153    JMP 2000        Return to the main program
2154
2155
```

CHAPTER

6

SYSTEM TESTING

The following contents are going to be covered in this chapter:

6.1 H-Bridge Testing

6.2 LDR Circuit Test

6.3 Test IR Sensor

6.4 test for operation lamp circuit

6.5 DS1643 testing

6.6 MC-1 microprocessor test

CHAPTER SIX

SYSTEM TESTING

6.1 H-Bridge Testing

First we connect the circuit as shown in figure 6-1, when we connect 5v to signal 1 and 0v to signal 2 motor operates in forward mode and when we connect 0v to signal 1 and 5v to signal 2motor operates in reverse mode.

Next step is adding Optocoupler 4n25 to both side of the circuit, adding Optocoupler causes a problem to circuit, by making the motor not operate.

The problem behind the motor problem is that when we send 0v to Optocoupler this voltage will not reach the base of transistor, so that PNP transistor will not operate. To solve this problem we connect 200ohm resistor at emitter of Optocoupler parallel with H-bridge so when we send 0v to Optocoupler the voltage in the base of H_bridge transistors will be 0v. the final circuit of h-bridge is shown in figure 6-1.

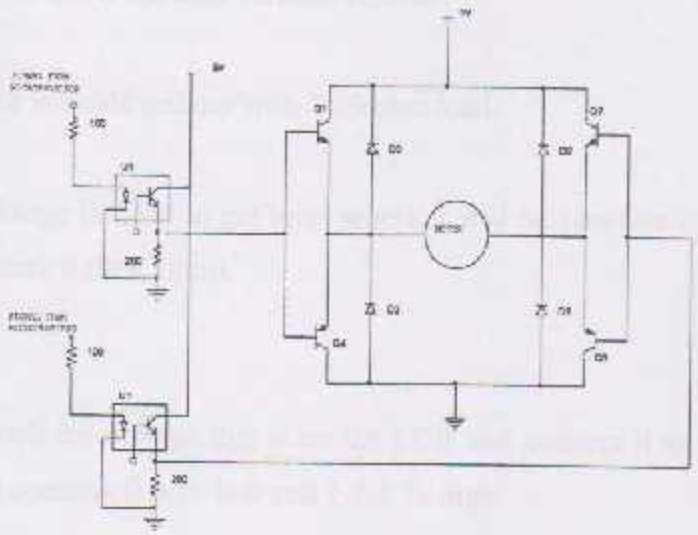


Figure 6.1: H-bridge circuit

6.2 LDR Circuit Test

This circuit is used to know the density of lighting that is outdoor the home.

6.2.1 Circuit building

1. we disconnect the LDR from the circuit after that we measure the resistor in darkness which will be 6M ohm ,which means open, and when we measure it with lighting it will be much less than that measured in darkness and as increase the density of light the resistor is going less, so that it work properly.

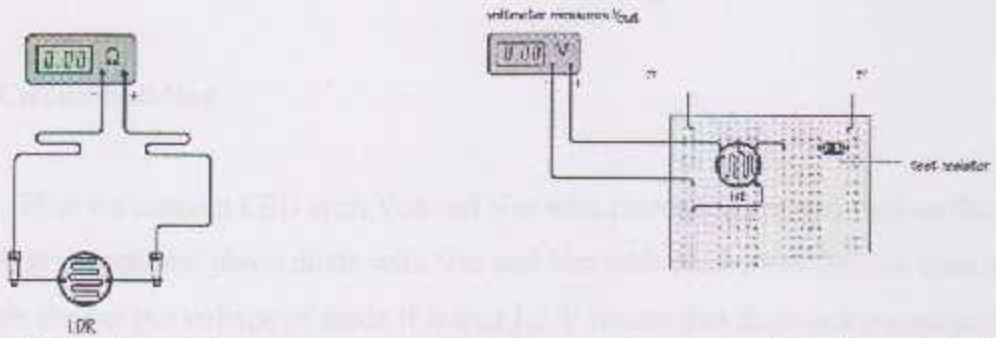


Figure 6-2 the left graph is the measurement of the resistance value operation. The right graph is the measurement of the out voltage for the potentiometer from LDR

2. How to know the load variable resistor:

A-we put variable resistor with 100kohm load.

B-we change its load to get level where it will be sensitive to lighting which we measure it (80K ohm).

3. We took the voltage that is on the LDR and connect it to Schmitt trigger, which it operates 0-0.7v low and 1.7-3.7v high.

6.3 Test IR Sensor

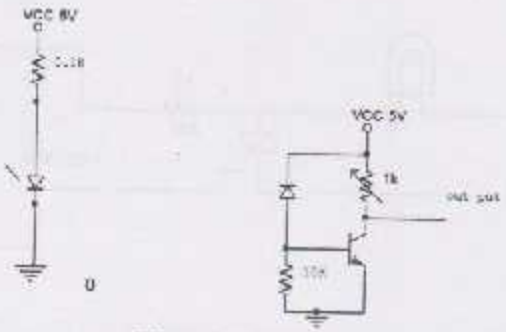


Figure 6-3 IR sensor

This circuit used to know whether as if there is a person near to the door.

6.3.1 Circuit building

First we connect LED with Vcc and Vss with protection resistor, and on the other side we connect photo diode with Vcc and Vss with protection resistor, then we measure the out put voltage of diode if it was 1.3 V means that there is a person and if it was 1.7 V mean there is no person, the distance between transmitter and receiver is 12 cm.

But the result is not enough to make it as input to Schmitt trigger, for that we do amplification to the current through making the voltage as input to amplifier, so that the out put of the amplifier going large, such that if there is a person the voltage is 5.03V and if there isn't it will be 0.03V.

6.4 TEST FOR OPERATION LAMB CIRCUIT

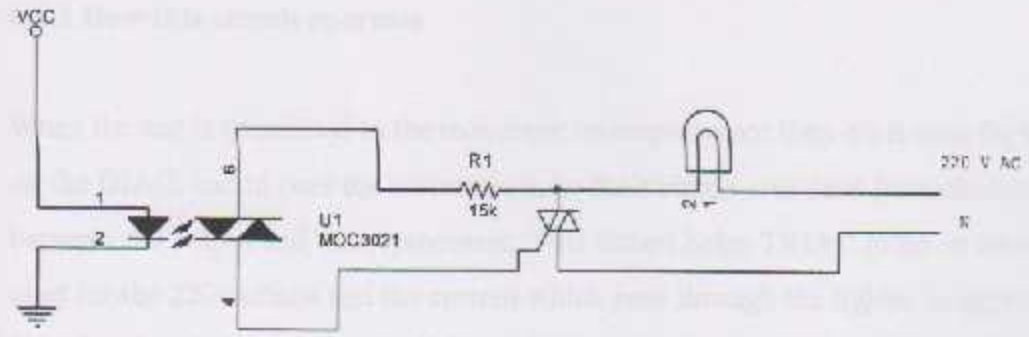


Figure 6-4 this circuit is used to control the lighting that works on 220v

6.4.1 Circuit building

1- We connect the moc that works on 5v through connect the 5v on the first pin and the ground on the second one

2- We put voltage multimiter on the output of the moc, and measure the voltage on it, the measured that we obtain (14mA), which is enough to operate trigger gate that is on triac

3- How to connect triac:

a- we connect emetar of triac that is on pin 4 into the moc with gate of triac

b- We connect the ANODE to N

c- We connect the lamp in series between Vcc (220v) and ANODE1

6.4.2 How this circuit operates

When the vcc is connected to the moc from microprocessor then it's it uses for turn on the DIAC, and to pass the current in it, so their circuit was used for isolation between the output and microprocessor, This circuit helps TRIAC to be on which used for the 220 voltage and the current which pass through the lighter to approach N. to be closed circuit, then the lighter will be turned on, and this voltage operate the TRIAC which allow the current to pass into it, as shown in the figure.

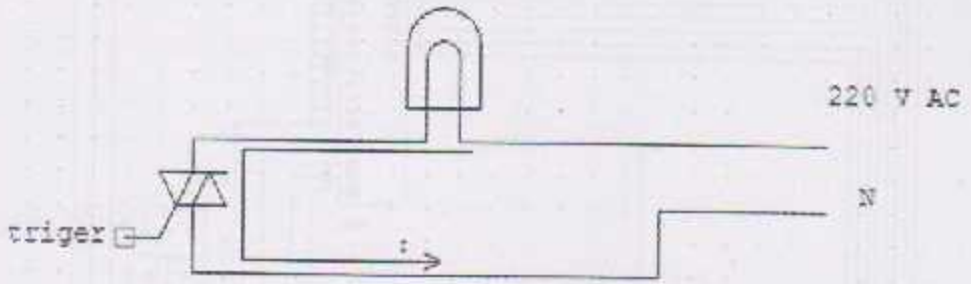


Figure 6-5 this circuit is explains current direction

We calculate R1 as follow

First we should know now the led need voltage and current operate, and also how much the maximum load.

$I = V\backslash R = 5V \setminus 220 = 2.27$ mA

MOC can hold 60 mA so that we choose 220 ohm which give us 2.27mA and we use it because it allow the starting current to run the lead which is found inside the moc.

6.5 DS1643 testing

As we mentioned before we use time keeping RAM to give us the time, we need to read from this chip hours only, so we set in it hour ,minutes and second.

We set this chip through connecting data and address lines, chip enable and control signals through switches as shown in figure 6-4.

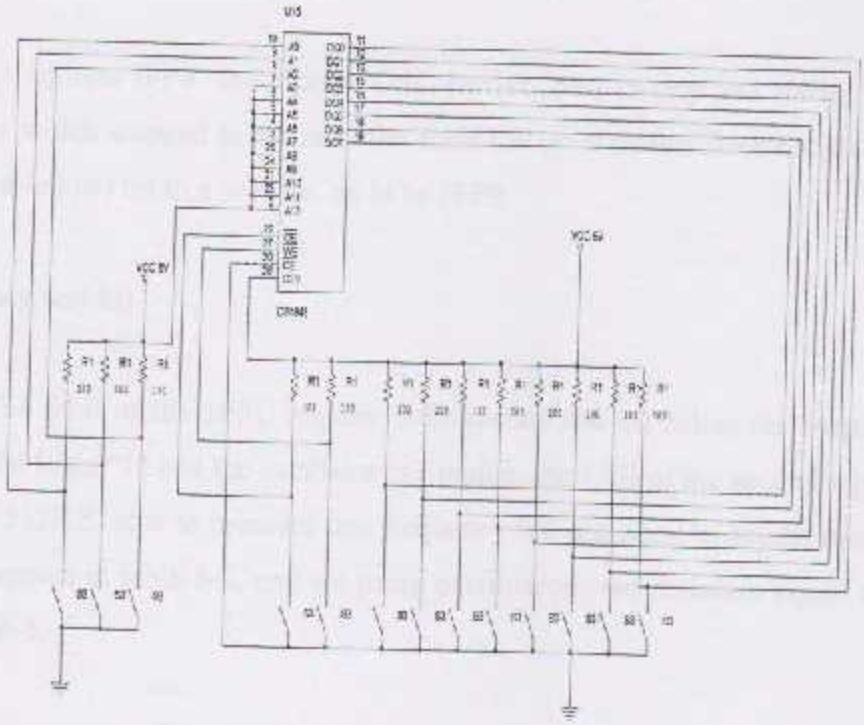


Figure 6-6 DS1643 setting circuit.

The first thing we did was setting the write bit to a one and the same for read bit which it 8-bit,7bit of address 1FF8 ,we enter this address through switches , now to input data to DS1643 we should put it in to read mode as shown in table 6-2.

Table 6-1 DS1643 truth table

V_{CC}	$\overline{CE}$	CE2	OE	$\overline{WE}$	MODE	DQ
5v	low	High	X	low	Write	Data in
5v	low	High	low	high	Read	Data out

Then by using switches we load (C0) into control register which enable us to enter new data to DS1643 register.

In address IFF9 the 6-bit is OSC (active low) to stop and staring the clock oscillator which stopped to increase the shelf life ,to start the clock oscillator we set OSC (active low) bit to a zero i.e. oo in to 1FF9.

Frequency test bit

The 6-bit of the 1FFC register is frequency test bit ,when the frequency test bit is set to logic "1" and the oscillator is running ,the LSB of the second register will toggle at 512HZ .now to measure this frequency the condition of access must remain valid as shown in table 6-2, and we using oscilloscope we maintain signal as shown in figure 6-5.

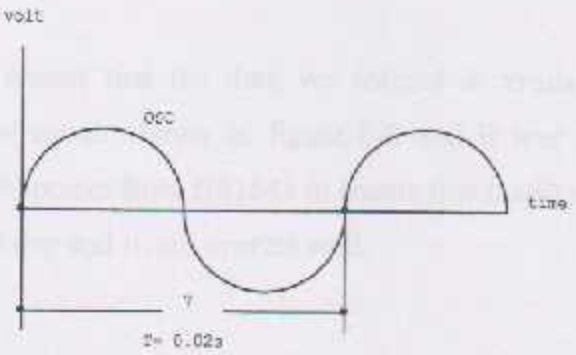


Figure 6-7 oscillator clock waves

F=1\T =1\0.002 =500HZ

Therefore the frequency we have is near the value it should be, so that DS1643 operate well, Then we set hour, minutes and seconds using the same method we used to setting control register and oscillator, At the end resetting the write bit to logic "0", it enables to transfers the previous value to actual clock counter and allows normal operation to resume, Table 6-3 show all the steps that we explain before.

Table 6-2 DS1643 setting description.

Address (A0-A12)	Data in (DQ0-DQ7)	$\overline{WE}$	$\overline{OE}$	NOTE
1FF8	C0	1	0	Sitting write bit
1FF9	00	1	0	Sitting clock oscillator
1FFC	40	1	0	Set frequency test bit
1FF9	-	0	1	Test frequency using oscilloscope
1FFB	14	1	0	Load hour by 14 (2PM)
1FFA	00	1	0	Setting minutes to 00
1FF9	00	1	0	Setting second to 00
1FF8	00	1	0	Start counting
1FFB	-	0	1	Read the hour

Finally ,we ensure that the data we entered is available on the register ,reading it using the circuit shown in figure 6-8 and it was right, after that we disconnect the electric power from DS1643 to ensure that it still operate, and we read the hour after several day and it still operate well.

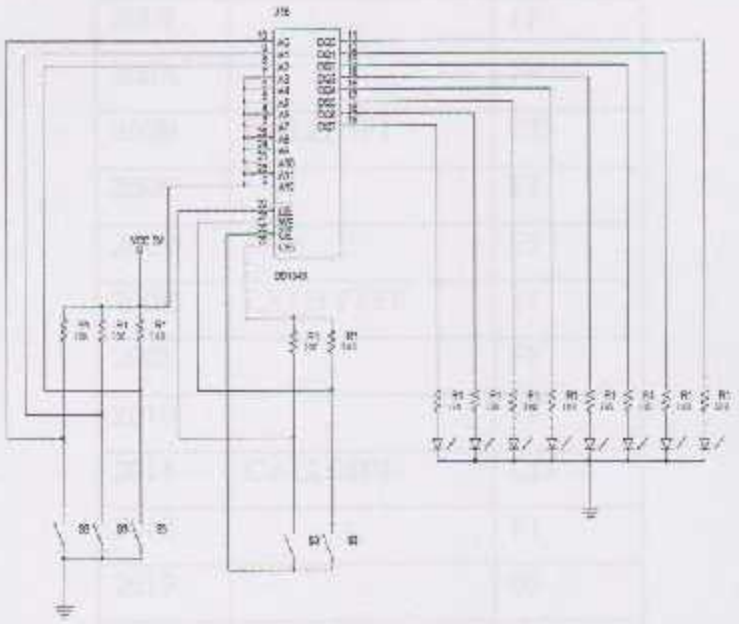


Figure 6-8 DS1643 reading data

6.6 MC-1 microprocessor test

MC-1 microprocessor is the most important component in our project ,so its important to ensure that it is in a good case, we write some programs and execute it.

6.6.1 to chick input and output ports we execute the following program.

2000	MVI A 02	3E
2001		02
2002	OUT 20	D3
2003		20
2004	IN 21	DB
2005		21
2006	OUT 22	D3
2007		22
2008	LXI D FFFF	11

2009		FF
200A		FF
200B	CALL05F1	CD
200C		F1
200D		05
200E	LXI D FFFF	11
200F		FF
2010		FF
2011	CALL05F1	CD
2012		F1
2013		05
2014	JMP 2004	C3
2015		04
2016		20

6.6.2 To chick display (seven segments) we execute the following program.

2000	MVI A 02	3E
2001		02
2002	OUT 20	D3
2003		20
2004	MVI A 00	3E
2005		00
2006	CALL036E	CD
2007		6E
2008		03
2009	LXI D FFFF	11
200A		FF
200B		FF

200C	CALL05F1	CD
200D		F1
200E		05
200F	INR A	3C
2010	JMP 2006	C3
2011		06
2012		20

6.6.3 To chick keypad we execute the following program.

2000	MVI A 02	3E
2001		02
2002	OUT 20	D3
2003		20
2004	MVI A 08	3E
2005		08
2006	SIM	30
2007	CALL02E7	CD
2008		E7
2009		02
200A	OUT 22	D3
200B		22
200C	LXI D FFFF	11
200D		FF
200E		FF
200F	CALL05F1	CD
2010		F1
2011		05
2012	JMP 2007	C3

2013		07
2014		20

6.6.4 To chick delay instruction we execute the following instruction.

2000	MVI A 02	3E
2001		20
2002	OUT 20	D3
2003		20
2004	MVI A 0F	3E
2005		0F
2006	OUT 22	D3
2007		22
2008	LXI D FFFF	11
2009		FF
200A		FF
200B	CALL05F1	CD
200C		F1
200D		5
200E	MVI A F0	3E
200F		F0
2010	OUT 22	D3
2011		22
2012	LXI D FFFF	11
2013		FF
2014		FF
2015	CALL05F1	CD
2016		F1

2017		5
2018	LXI D FFFF	11
2019		FF
201A		FF
201B	CALL05F1	CD
201C		F1
201D		5
201E	JMP 2004	C3
201F		4
2020		20

CHAPTER

7

Limitations and Recommendations

The following contents are going to be covered in this chapter:

CHAPTER SEVEN

Limitations and Recommendations

7.1 Limitations of Project

We are facing some of limitations in Our Projects that's including the limitations in partial controlled room and we will discuss these limitations and problems in sections as below.

7.1.1 General Limitations of the Partial Controlled Room

The most limitation of the partial controlled room is determined the as the following:

Load of the project

The time factor is the most important Limitations that's face us, load of the project is 1 credit hour and this not enough to such projects.

Design content

Our study plan in applied electronics is lacking to enough design content.

7.1.2 Limitations of the Partial Controlled Room

7.1.2.1 Design of the Circuit and Components

The second Limitations in the Controlled Room is the components of the microprocessor interfacing with inputs and outputs such as 8085A, 8255, and DS1643. And the designing of the circuit, if we want to construct the circuit of the partially controlled room we cant get and give the result that we want. In addition to the Cost of these components are expensive.

Programming Language

The Programming of the Microprocessor 8085A needs more efforts and time because we want to Programming 8085A by using Machine Language (Machine code) so we must convert from Assembly language to machine language.

7.1.2.2 Monitoring component (PIR)

The most limitation of the Monitoring System is determined as the following:

Area that PIR cover

PIR didn't cover all area of the room, but it cover a good area and it nearly enough to prove our idea.

Sensitivity of PIR

PIR depend on the variation of temperature to detect persons, so if a person stay several time without moving PIR will not detect him.

7.1.2.3 Interfacing time keeping ram with UNIT MC-1 MICROPROCESSOR

Because we use kit its impossible to connect this chip as RAM so that microprocessor cant send the address and control signals to read data from its registers.

7.2 Solutions of the problems

We Find and put the Solving of the limitations and problems that's explained in above sections , the solutions are described in sections 7.2.1 and 7.2.2 as below.

7.2.1 Solutions of the controlled room

The solutions of the controlled room are determined as the following:

We use kit unit MC-1 microprocessor 8085A, that's including all components of interfacing Microprocessor with input devices, that saves time, cost and efforts.

Unit MC-1 Microprocessor 8085A is programming directly from the keypad (input device) without Programmer by using the machine code.

7.2.2 Solutions of the Monitoring component (PIR)

The solutions of the limitations of the Monitoring System are determined as the following:

Use PIR that has high sensitivity and special lens to get good sensitivity and covered large area.

7.2.3 Solutions of interfacing time keeping ram DS1643 with unit MC-1 microprocessor.

We need to read data from DS1643 from only one address and there is no need to write data to DS1643 so we give stable address and enable to it, and it becomes ready to give data continuously to microprocessor.

7.3 The Conclusion

This project adds a new technique to control the basic things in any room, the door, lighting and window, and transfer the modern technology in our society. The controlled rooms have a lot of Features and this is some of this Feature as the following:

The controlled room is not expensive when comparing the cost with its benefits. The controlled room is not complex, on the contrary, it's simple to use in every where such as shops, homes and banks…etc.

When using the control room, the people will be feeling more safety and save electrical power and so save money.

7.4 Recommendations

Increase the credit hour of the project from 1 credit hour to 3 credit hour.

Adding courses for design the electronics circuits because it's very benefits for build the circuit and choosing the suitable components for such projects.

We hope in the future to add some techniques on our project to be more complementary, as the following:

- Develop our program of microprocessor or use different component than PIR to detect if there is any person in the room.

- Develop our project to fully controlled room, by control the temperature of room, use remote control, weekend consideration.....etc.

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SN5414, SN54LS14, SN7414, SN74LS14
HEX SCHMITT-TRIGGER INVERTERS

SDLS049B – DECEMBER 1983 – REVISED FEBRUARY 2002

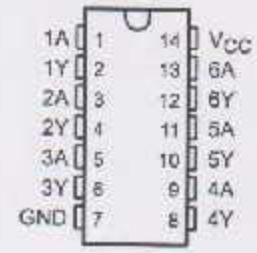
- **Operation From Very Slow Edges**
- **Improved Line-Receiving Characteristics**
- **High Noise Immunity**

description

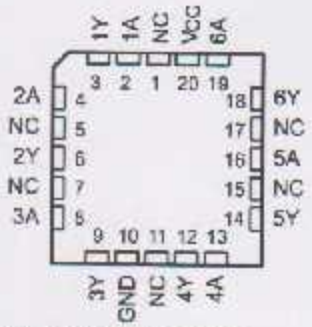
Each circuit functions as an inverter, but because of the Schmitt action, it has different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

SN5414, SN54LS14 . . . J OR W PACKAGE
SN7414 . . . D, N, OR NS PACKAGE
SN74LS14 . . . D, DB, OR N PACKAGE
(TOP VIEW)



SN54LS14 . . . FK PACKAGE
(TOP VIEW)



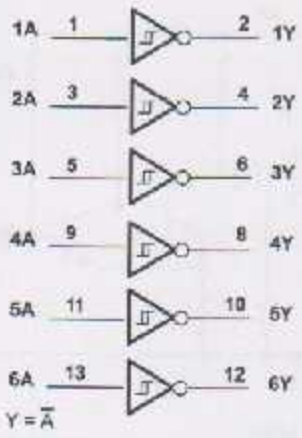
NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN7414N	SN7414N
		Tube	SN74LS14N	SN74LS14N
	SOIC – D	Tube	SN7414D	7414
		Tape and reel	SN7414DR	
		Tube	SN74LS14D	LS14
		Tape and reel	SN74LS14DR	
	SOP – NS	Tape and reel	SN7414NSR	SN7414
	SSOP – DB	Tape and reel	SN74LS14DBR	LS14
–55°C to 125°C	CDIP – J	Tube	SN5414J	SN5414J
		Tube	SNJ5414J	SNJ5414J
		Tube	SN54LS14J	SN54LS14J
		Tube	SNJ54LS14J	SNJ54LS14J
	CFP – W	Tube	SNJ5414W	SNJ5414W
		Tube	SNJ54LS14W	SNJ54LS14W
	LCCC – FK	Tube	SNJ54LS14FK	SNJ54LS14FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

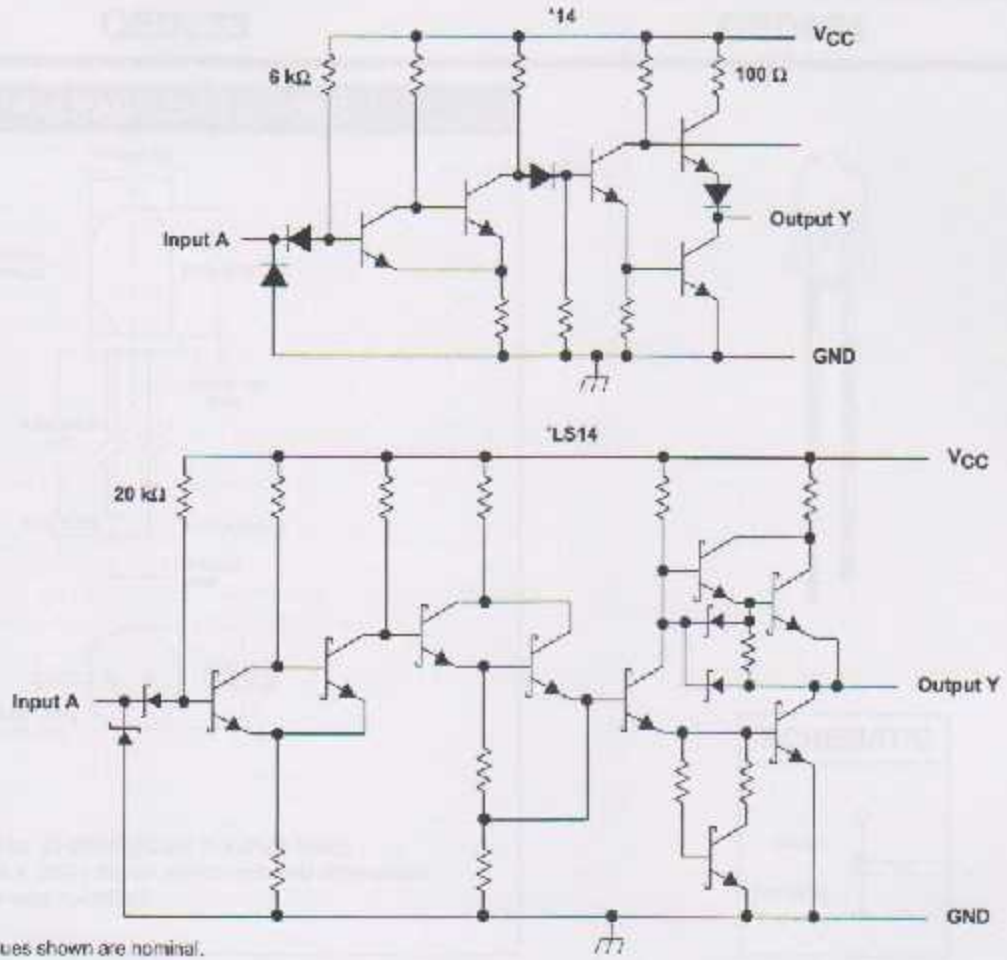
logic diagram (positive logic)



$Y = \overline{A}$

The numbers shown are for the D, DB, J, N, NS, and W packages.

schematic



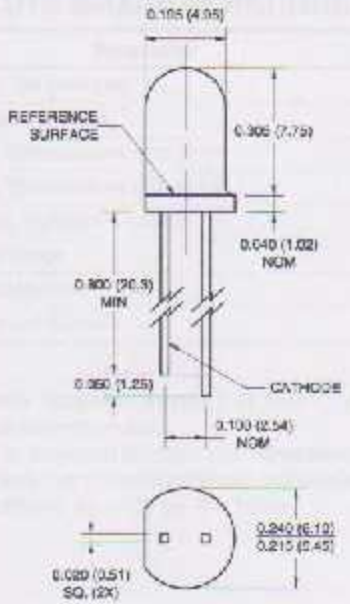
Resistor values shown are nominal.

FAIRCHILD
SEMICONDUCTOR®

PLASTIC INFRARED LIGHT EMITTING DIODE

QED233 QED234

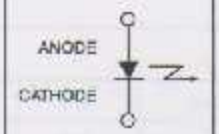
PACKAGE DIMENSIONS



NOTES:

1. Dimensions for all drawings are in inches (mm).
2. Tolerance of ± .010 (.25) on all non-nominal dimensions unless otherwise specified.

SCHEMATIC



DESCRIPTION

The QED233 / QED234 is a 940 nm GaAs / AlGaAs LED encapsulated in a clear untinted, plastic T-1 3/4 package.

FEATURES

- λp = 940 nm
- Chip material =GaAs with AlGaAs window
- Package type: T-1 3/4 (5mm lens diameter)
- Matched Photosensor: QSD122/123/124
- Medium Emission Angle, 40°
- High Output Power
- Package material and color: Clear, untinted, plastic
- Ideal for remote control applications

FAIRCHILD
SEMICONDUCTOR®

PLASTIC INFRARED LIGHT EMITTING DIODE

QED233 QED234

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Rating	Unit
Operating Temperature	T_{OPR}	-40 to +100	°C
Storage Temperature	T_{STG}	-40 to +100	°C
Soldering Temperature (Iron)[2,3,4]	T_{SOL-I}	240 for 5 sec	°C
Soldering Temperature (Flow)[2,3]	T_{SOL-F}	260 for 10 sec	°C
Continuous Forward Current	I_F	100	mA
Reverse Voltage	V_R	5	V
Power Dissipation[1]	P_D	200	mW
Peak Forward Current	I_{FP}	1.5	A

Derate power dissipation linearly 2.67 mW/°C above 25°C.
RMA flux is recommended.
Methanol or isopropyl alcohols are recommended as cleaning agents.
Soldering iron 1/16" (1.6mm) minimum from housing.
Pulse conditions: tp = 100 µs, T = 10 ms.

ELECTRICAL / OPTICAL CHARACTERISTICS (T_A =25°C)

PARAMETER	TEST CONDITIONS	DEVICE	SYMBOL	MIN	TYP	MAX	UNITS
Peak Emission Wavelength	I_F = 20 mA	ALL	λ_{PE}	—	940	—	nm
Spectral Bandwidth	I_F = 20 mA	ALL	—	50	—	nm	
Temp. Coefficient of λ_{PE}	I_F = 100 mA	ALL	TC_λ	—	0.2	—	nm/K
Emission Angle	I_F = 100 mA	ALL	$2\Theta_{1/2}$	—	40	—	Deg.
Forward Voltage	I_F = 100 mA, tp = 20 ms	ALL	V_F	—	—	1.6	V
Temp. Coefficient of V_F	I_F = 100 mA	ALL	TC_V	—	-1.5	—	mV/K
Reverse Current	V_R = 5 V	ALL	I_R	—	—	10	µA
Radiant Intensity	I_F = 100 mA, tp = 20 ms	QED233	I_E	10	—	50	mW/sr
		QED234		27	—	—	
Temp. Coefficient of I_E	I_F = 20 mA	ALL	TC_I	—	-0.6	—	%/K
Rise Time	I_F = 100 mA	ALL	t_r	—	1000	—	ns
Fall Time		ALL	t_f	—	1000	—	

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QED233 QED234

TYPICAL PERFORMANCE CURVES TBD

Fig. 1 Normalized Radiant Intensity vs. Forward Current

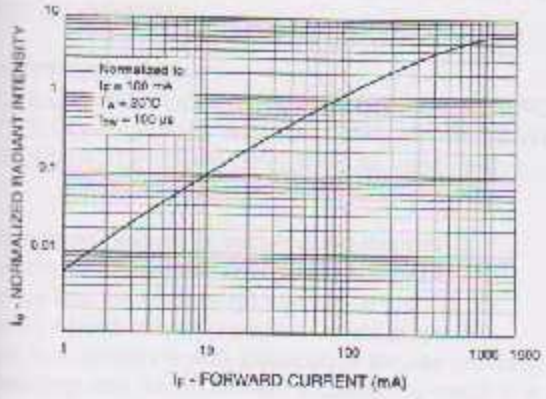


Fig. 2 Forward Voltage Vs. Ambient Temperature

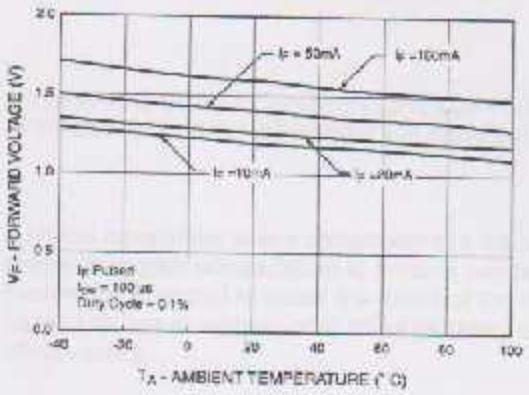


Fig. 3 Normalized Radiant Intensity vs. Wavelength

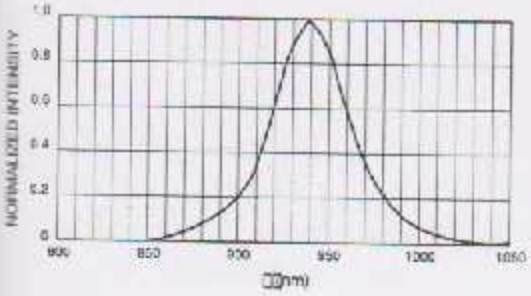


Fig. 4 Radiation Diagram

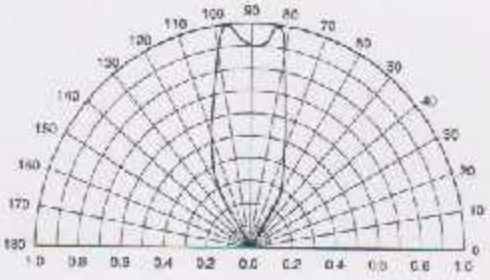
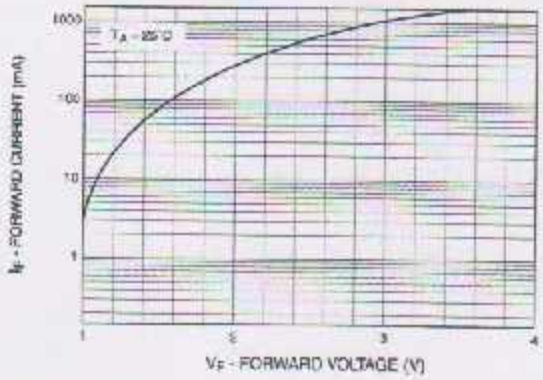


Fig. 5 Forward Current vs. Forward Voltage



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QED233 QED234

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body,or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

SGS-THOMSON MICROELECTRONICS

BD439/BD440 BD441/BD442

COMPLEMENTARY SILICON POWER TRANSISTORS

- SGS-THOMSON PREFERRED SALESTYPES
- COMPLEMENTARY PNP - NPN DEVICES

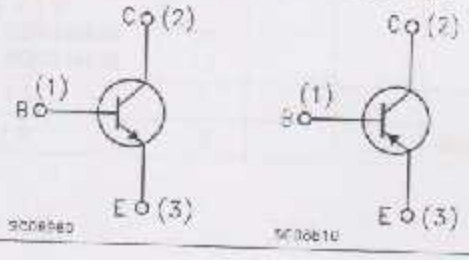
DESCRIPTION

The BD439 and BD441 are silicon epitaxial-base NPN power transistors in Jedec SOT-32 plastic package, intented for use in power linear and switching applications.

The complementary PNP types are BD440, and BD442 respectively.

SOT-32

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value		Unit
		NPN	BD439	BD441	
		PNP	BD440	BD442	
V_{CBO}	Collector-Base Voltage (I_E = 0)		60	80	V
V_{CES}	Collector-Emitter Voltage (V_{BE} = 0)		60	80	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)		60	80	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)		5		V
I_C	Collector Current		4		A
I_{CM}	Collector Peak Current (t ≤ 10 ms)		7		A
I_B	Base Current		1		A
P_{tot}	Total Dissipation at T_c ≤ 25 °C		36		W
T_{stg}	Storage Temperature		-65 to 150		°C
T_j	Max. Operating Junction Temperature		150		°C

For PNP types voltage and current values are negative.

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	3.5	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

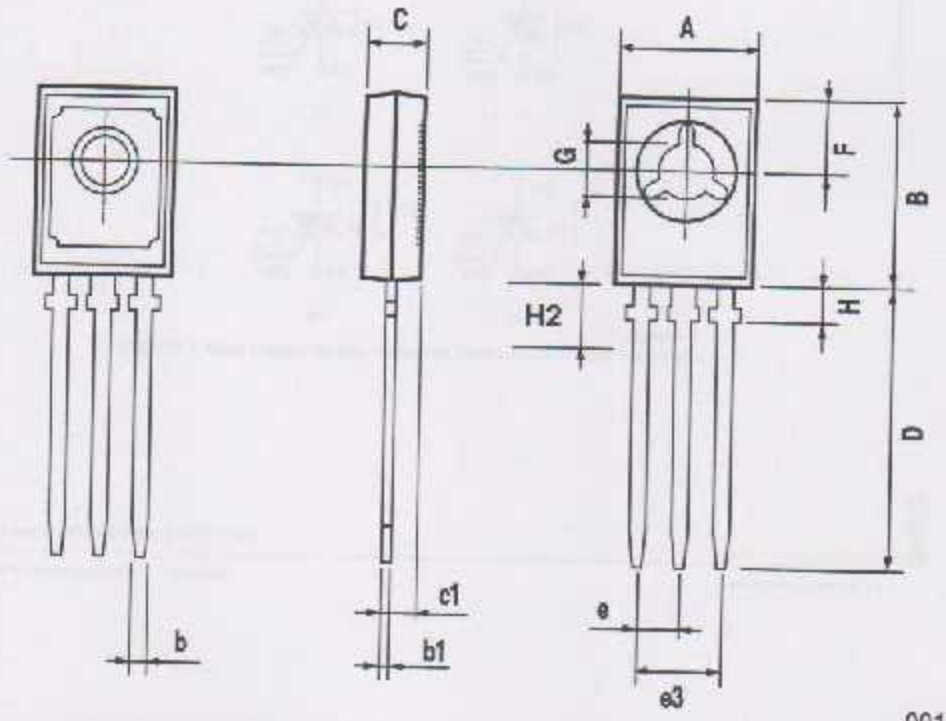
ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{CBO}	Collector Cut-off Current (I_E = 0)	for **BD439/440** V_{CB} = 60 V for **BD441/442** V_{CB} = 80 V				100 100	µA µA
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	for **BD439/440** V_{CB} = 60 V for **BD441/442** V_{CB} = 80 V				100 100	µA µA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V				1	mA
$V_{CEO(sus)}$*	Collector-Emitter Sustaining Voltage (I_B = 0)	I_C = 100 mA	for **DB439/440** for **BD441/442**	60 80			V V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	I_C = 2 A	I_B = 0.2 A			0.8	V
V_{BE}*	Base-Emitter Voltage	I_C = 10 mA I_C = 2 A	V_{CE} = 5 V V_{CE} = 1 V		0.58	 1.5	V V
h_{FE}*	DC Current Gain	I_C = 10 mA	V_{CE} = 5 V				
			for **BD439/440**	20	130		
			for **BD441/442**	15	130		
		I_C = 500 mA	V_{CE} = 1 V				
			for **BD439/440**	40	140		
			for **BD441/442**	40	140		
		I_C = 2 A	V_{CE} = 1 V				
			for **BD439/440**	25			
			for **BD441/442**	15			
h_{FE1}/h_{FE2}*	Matched Pair	IC = 500 mA	V_{CE} = 1 V			1.4	
f_T	Transition frequency	I_C = 250 mA	V_{CE} = 1 V	3			MHz

* Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

SOT-32 (TO-126) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	7.4		7.8	0.291		0.307
B	10.5		10.8	0.413		0.445
b	0.7		0.9	0.028		0.035
b1	0.49		0.75	0.019		0.030
C	2.4		2.7	0.040		0.106
c1	1.0		1.3	0.039		0.050
D	15.4		16.0	0.606		0.629
e		2.2			0.087	
e3	4.15		4.65	0.163		0.183
F		3.8			0.150	
G	3		3.2	0.118		0.126
H			2.54			0.100
H2		2.15			0.084	



0016114

Triac Control Using the COP400 Microcontroller Family

National Semiconductor
COP Note 6
February 1981

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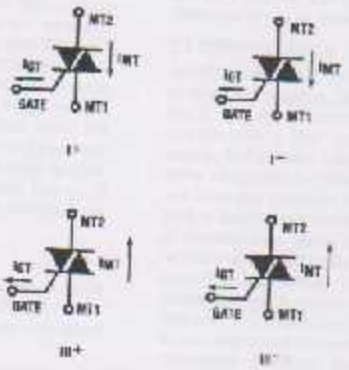
1.0 Triac Control

The COP400 single-chip controller family members provide computational ability and speed which is more than adequate to intelligently manage power control. These controllers provide digital control while low cost and short turn-around enhance COPS™ desirability. The COPS controllers are capable of 4 μs cycle times which can provide more than adequate computational ability when controlling 60 Hz line voltage. Input and output options available on the COPS devices can contour the device to apply in many electrical situations. A more detailed description of COPS qualifications is available in the COP400 data sheets.

The COPS controller family may be utilized to manage power in many ways. This paper is devoted to the investigation of low cost triac interfaces with the COP400 family microcontroller and software techniques for power control applications.

1.1 BASIC TRIAC OPERATION

A triac is basically a bidirectional switch which can be used to control AC power. In the high-impedance state, the triac blocks the principal voltage across the main terminals. By pulsing the gate or applying a steady state gate signal, the triac may be triggered into a low impedance state where conduction across the main terminals will occur. The gate signal polarity need not follow the main terminal polarity; however, this does affect the gate current requirements. Gate current requirements vary depending on the direction of the main terminal current and the gate current. The four trigger modes are illustrated in *Figure 1*.

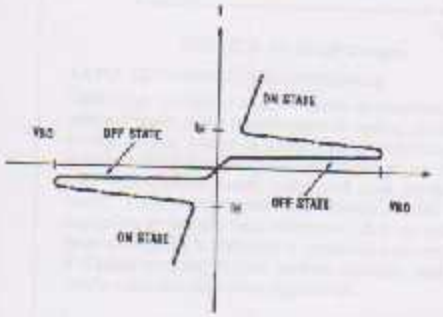


TL/DD/9688–1

FIGURE 1. Gate Trigger Modes. Polarities Referenced to Main Terminal 1.

The breakover voltage (V_{BO}) is specified with the gate current (I_{GT}) equal to zero. By increasing the gate current supplied to the triac, V_{BO} can be reduced to cause the triac to go into the conduction or on state. Once the triac has entered the on state the gate signal need not be present to sustain conduction. The triac will turn itself off when the main terminal current falls below the minimum holding current required to sustain conduction (I_H).

A typical current and voltage characteristic curve is given in *Figure 2*. As can be seen, when the gate voltage and the main terminal 2 (MT2) voltages are positive with respect to MT1 the triac will operate in quandrant 1. In this case the trigger circuit sources current to the triac (I+ MODE).



TL/DD/7889–2

FIGURE 2. Voltage-Current Characteristics

After conduction occurs the main terminal current is independent of the gate current; however, due to the structure of the triac the gate trigger current is dependent on the direction of the main terminal current. The gate current requirements vary from mode to mode. In general, a triac is more easily triggered when the gate current is in the same direction as the main terminal current. This can be illustrated in the situation where there is not sufficient gate drive to cause conduction when MT2 is both positive and negative. In this case the triac may act as a single direction SCR and conduction occurs in only one direction. The trigger circuit must be designed to provide trigger currents for the worst case trigger situation. Another reason ample trigger current must be supplied is to prevent localized heating within the pellet and speed up turn-on time. If the triac is barely triggered only a small portion of the junction will begin to conduct, thus causing localized heating and slower turn on. If an insufficient gate pulse is applied damage to the triac may result.

1.2 TRIGGERING

Gate triggering signals should exceed the minimum rated trigger requirements as specified by the manufacturer. This is essential to guarantee rapid turn-on time and consistent operation from device to device.

Triac turn-on time is primarily dependent on the magnitude of the applied gate signal. To obtain decreased turn-on times a sufficiently large gate signal should be applied. Faster turn-on time eliminates localized heat spots within the pellet structure and increases triac dependability.

Digital logic circuits, without large buffers, may not have the drive capabilities to efficiently turn on a triac. To insure proper operation in all firing situations, external trigger circuitry might become necessary. Also, to prevent noise from disturbing the logic levels, AC/DC solation or coupling techniques must be utilized. Sensitive gate triacs which require minimal gate input signal and provide a limited amount of main terminal current may be driven directly. This paper will focus on $190V_{AC}$ applications of power control.

1.3 ZERO VOLTAGE DETECTION

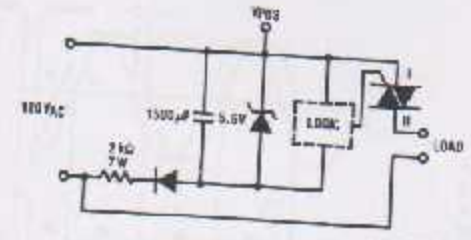
In many applications it is advantageous to switch power at the AC line zero voltage crossing. In doing this, the device being controlled is not subjected to inherent AC transients. By utilizing this technique, greater dependability can be obtained from the switching device and the device being switched. It is also sometimes desirable to reference an event on a cyclic basis corresponding to the AC line frequency. Depending on the load characteristics, switching times need to be chosen carefully to insure optimal performance. Triac controlled AC switching referenced to the AC 60 Hz line frequency enables precise control over the conduction angle at which the triac is fired. This enables the COPS device to control the power output by increasing or decreasing the conduction angle in each half cycle.

A wide variety of zero voltage detection circuits are available in various levels of sophistication. COPS devices, in most cases, can compensate for noisy or semi-accurate ZVD circuits. This compensation is utilized in the form of debounce and delay routines. If a noisy transition occurs near zero volts the COPS device can wait for a valid transition period specified by the maximum amount of noise present. Some software considerations are presented in the software section and are commented upon. The minimal detection circuit is shown in *Figure 3*.

1.4 DIRECT COUPLE

Isolation associated problems can be overcome by means of direct AC coupling. One such method is illustrated in *Figure 3*. This circuit incorporates a half-wave rectifier in conjunction with a filter capacitor to provide the logic power supply. The positive half-cycle is allowed to drop across the zener diode and be filtered by the capacitor. This creates a low cost line interface; however, only a limited supply current is available. In order to control the current capabilities of this circuit the series resistor must be modified. However, as more current is required, the power that must be dissipated in the series resistor increases. This increases the power dissipation requirements of the series resistor and the system cost. For applications which require large current sources an alternative method is advisable. In order to assure consistent operation, power supply ripple must be mini-

mized. COPS devices can be operated over a relatively wide power supply range. However, excessive ripple may cause an inadvertent reset operation of the device.

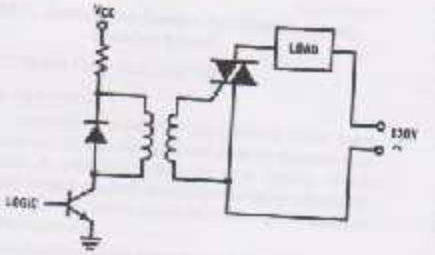


TL/DD/8909–3

FIGURE 3. AC Direct Couple

1.5 PULSE TRANSFORMER INTERFACE

Digital logic control of triacs is easily accomplished by triggering through pulse transformers or optical coupling. The energy step-up gained by using a pulse transformer should provide a more than adequate gate trigger signal. This complies with manufacturers' suggested gate signal requirements. Pulse transformers also provide AC/DC isolation necessary in control logic interfaces. Minimal circuit interface to the pulse transformer is required as shown in *Figure 4*. Optical coupling circuits provide isolation, and in some cases adequate gate drive capabilities.



TL/DD/8909–4

FIGURE 4. Pulse Transformer Interface

A logic controlled pulse is applied to the base of the transistor to switch current through the primary of the pulse transformer. The transformer then transfers the signal to the secondary and causes the triac to fire. The energy transfer that is now available on the secondary is more than adequate to turn on the triac in any of its operating modes. When the pulse transformer is switched off a reverse EMF is generates in the primary coil which may cause damage to the transistor. The diode across the primary serves to protect the collector junction of the switching transistor. Another major advantage is AC isolation; the gate of the triac is now completely isolated from the logic portion of the circuit.

1.6 FALSE TURN-ON

When switching an inductive load, voltage spikes may be generated across the main terminals of the triac which have the potential of a non-gated turn-on of the triac. This creates the undesirable situation of limited control of the system. In a system with an inductive load the voltage leads the current by a phase shift corresponding to the amount of inductance in the motor. As the current passes near zero, the voltage is at a non-zero value, offset due to the phase shift. When the principal current through the triac pellet decreases to a value not capable of sustaining conduction the triac will turn off. At this point in time the voltage across the terminals will instantaneously attain a value corresponding to the phase shift caused by the inductive load. The rapid decay of current in the inductor causes an L dI/dT voltage applied across the terminals of the triac. Should this voltage exceed the blocking voltage specified for the triac, a false turn on will occur.

In order to avoid false turn-on, a snubber network must be added across the terminals to absorb the excess energy generated by this situation. A common form of this network is a simple RC in series across the terminals. In order to select the values of the network it is necessary to determine the peak voltage allowable in the system and the maximum dV/dT stress the triac can withstand. One approach to obtaining the optimal values for R_S and C_S is to model the effective circuit and solve for the triac voltage. The snubber in conjunction with the load can now be modeled as an RLC network. Due to the two storage elements (L motor, C snubber) a second order differential equation is generated. Rather than approach this problem from a computer standpoint it becomes much easier to obtain design curves generated for rapid solution of this problem. These design curves are available in many triac publications. (For instance, see RCA application note AN 4745.)

2.0 Software Techniques

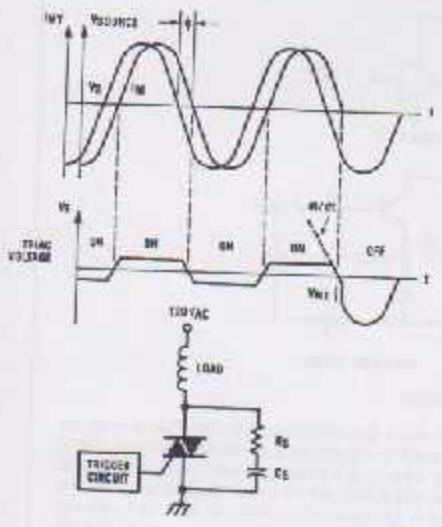
2.1 ZERO VOLTAGE DETECTION

In order to intelligently control triacs on a cyclic basis, an accurate time base must be defined. This may be in the form of an AC, 60 Hz sync pulse generated by a zero voltage detection circuit or a simple real time clock. The COP420 series microcontrollers are suited to accommodate either of these time base schemes while accomplishing auxiliary tasks.

Zero voltage detection is the most useful scheme in AC power control because it affords a real time clock base as well as a reference point in the AC waveform. With this information it is possible to minimize RFI by initiating power-on operations near the AC line voltage zero crossing. It is also possible to fire the triac for only a portion of the cycle, thus utilizing conduction angle manipulation. This is useful in both motor control and light intensity control.

Sophisticated zero voltage detection circuits which are capable of discriminating against noise and switch precisely at zero crossing are not necessary when used in conjunction with a COPS device. COPS software is capable of compensating for noisy or semi-accurate zero voltage detection circuits. This can be accomplished by introducing delays and debounce techniques in the software routines. With a given reference point in the AC waveform it now becomes easy

to divide the waveform to efficiently allocate processing time. These techniques are illustrated in the code listing at the end of this paper.



TL/DD/6939-5

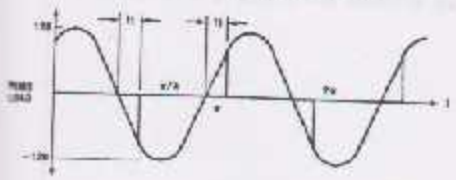
FIGURE 5. Current Lag Caused by Inductive Load, Snubber Circuit

2.2 PROCESSING TIME ALLOCATIONS

Half Cycle Approach

In order to accomplish more than triac firing, dead delay time must be turned into computation time. It appears that the controller is occupied totally by time delays, which leaves a very limited amount of additional control capability. There are, however, many ways to accomplish auxiliary tasks simultaneously.

On each half cycle an initial delay is incorporated to space into the cycle. This dead time may be put to use and very little voltage to the load is sacrificed. For example, if the load is switched on at $\pi/4$ RAD, the maximum applied RMS voltage to the load is $114V_{RMS}$ (assuming $V_{SUPPLY} = 120V_{RMS}$). This is illustrated in the figure below.



TL/DD/6939-6

FIGURE 6. Full Cycle Approach

If a delay of $\pi/4$ RAD (45 degrees) is inserted after each zero crossing detection the RMS voltage to the load can be determined in the following manner.

$$V_{LOAD} = \sqrt{\frac{(120\sqrt{2})^2}{(2)\pi}(2)\int_{\pi/4}^{\pi} \sin^2(\omega t)\, dt}$$

$$V_{LOAD} = \sqrt{\frac{(120\sqrt{2})^2}{(2)\pi}(2)(1.420)}$$

$$V_{LOAD} = 114.4\ V_{RMS}$$

$\pi/4$ RAD = 45 degrees @ 60 Hz $t = 2.08$ ms

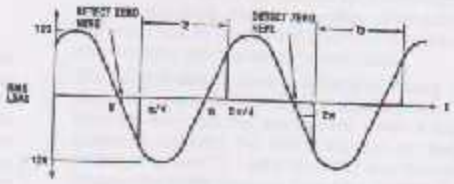
As can be seen the dead time on each half cycle can be 2.08 ms and the load will still see 114.4 V_{RMS} of a V_{SUPPLY} of 120 V_{RMS}. If this approach is implemented the initial delay of 2.08 ms can be used as computation time. The number of instructions which can be executed when operating at 4 µs instruction cycle time is:

2.08 ms/4 µs = 520 instructions

(120 instructions at 15 µs cycle time)

Full Cycle Approach

The methods of half cycle and full cycle triggering are very similar in procedure. The main difference is that all timing is referenced from only one (of the two) zero voltage detection transition in each full AC cycle. For most all applications, when varying the conduction angle it is desirable to fire at the same conduction angle each half cycle to maintain a symmetric applied voltage. In order to accomplish this the triac may be fired twice from one reference point. When applying this technique an 8.33 ms delay must be executed to maintain the symmetric applied voltage. This approach provides the most auxiliary computation time in that the 8.33 ms delay may be turned into computational time. The basic flow for this technique is illustrated below.



TL/DD/6939-7

FIGURE 7. Full Cycle Approach

In the above example the zero crossing pulse is debounced on the one-to-zero transition, thus marking the beginning of a full cycle. Once this transition has been detected, an ini-

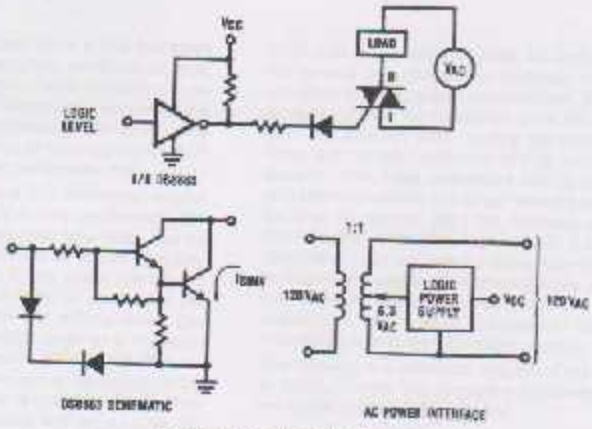


FIGURE 8. Steady State Triggering

TL/DD/9378-8

lial delay of w/z RAD is incorporated and the triac is fired. At this time exactly 8.33 ms is available until the triac need be triggered again. This will provide a symmetric voltage to the load only if the delay is 8.33 ms. During this period the number of instructions which can be executed when operating at 4 µs is:

$$8.33\ \text{ms}/4\ \mu\text{s} = 2082$$

(520 instructions at 16 µs)

An alternative approach may be to take the burden from the COPS device by using peripheral devices such as static display controllers, external latches, etc.

2.3 STEADY STATE TRIGGERING

It is possible to trigger a triac with a steady state logic level. This is accomplished by allowing the triac gate to sink or source current during the desired on-time. When utilizing this method it becomes easier to trigger the triac and leave it on for many cycles without having to execute code to retrigger. This approach is advantageous when the triac must be fired is for relatively long periods and conduction angle firing is not desired, thus more time is available to accomplish auxiliary tasks. A steady state on or off signal and external circuitry can accomplish triac firing and free the processor for other tasks. If it is desired to use a pulse transformer, an external oscillator must be gated to the triac to provide the trigger signal. A pulse train of 10 to 15 kHz is adequate to fire the triac each half cycle. This calls for external components and is relatively costly. If isolation associated problems can be tolerated or overcome (due power supply transformers, direct AC coupling, etc.), a simple buffer may be utilized in triggering the triac. This method is illustrated in *Figure 8*. The National Semiconductor DS8663 display driver is capable of steady state firing of the triac. National offers many buffers capable of driving several hundred milliamps, which are suitable for driving triacs. On the market today there are many suppliers of sensitive gate triacs which may be triggered directly from a COPS device or in conjunction with a smaller external buffer.

The DS8863 display driver is capable of sinking up to 500 mA, which is adequate to drive a standard triac. In the off state the driver will not sink current. When a logic "1" is applied to the input the device will turn on. Keeping the device off (output "1") will prevent the triac from turning on because the buffer does not have the capability of sourcing current. A series resistor limits the current from the triac gate and the diode isolates the negative spikes from the gate. Since the drive circuit will only sink current in this configuration, the triac will be operating in the I- and III- modes.

3.0 Triac Light Intensity Control Code

The following code is not intended to be a final functional program. In order to utilize this program, modifications must be made to specialize the routines. This is intended to illustrate the method and is void of control code to command a response such as intensify or deintensify. The control is up to the user and full understanding of the program must be attained before modifications can be implemented.

This program is a general purpose light intensifying routine which may be modified to suit light dimmer applications. The delay routines require a 4.469 μs cycle time which can be attained with a 3.576 MHz crystal (CKI/16 option). This program divides the half cycle of a 60 Hz power line into 16 levels. Intensity is varied by increasing or decreasing the conduction angle by firing the triac at various levels. The program will increase the conduction angle to a maximum specified intensity in a fixed amount of time. The time required to intensify to the maximum level is dependent on the number of fire-times per level that is specified (FINO). This code illustrates a half cycle approach and relies on the parameters specified by the programmer in the control selection.

Zero crossings of the 60 Hz line are detected and software debounced to initiate each half cycle; thus the triac is serviced on every half cycle of the power line. A level/sublevel approach is utilized to vary the conduction angle and provide a prolonged intensifying period. The maximum intensity is specified by the "LEVEL" RAM location and time required to get to that level is specified by the "FINO" RAM location.

Once a level has been specified, the remaining time in the half cycle is then divided into sublevels. The sublevels are increased in steps to the maximum level. The "FINO" RAM location contains the number of times that the triac will be fired per sublevel, thus creating the intensity time base. There are 15 valid sublevels and up to 15 fire-times per sublevel. Both these parameters may be increased to provide better resolution and longer intensify periods. To make the triac de-intensify (dim) the sublevels need only to be decremented rather than incremented. If this is done, the conduction angle will start out at the maximum level and dim by means of stepping down the sublevels. When modifying this routine to incorporate more resolution or increased versatility, care must be taken to account for transfer of control instructions to and from the delay routines.

The following is a schematic diagram of the COPS interface to 120V_{AC} lamps. The program will intensify or de-intensify the lamps under program control.

3.1 TRIAC LIGHT INTENSIFY ROUTINE

This program intensifies a light source by varying the conduction angle applied to the load. The maximum level of intensity is stored in "LEVEL," and the time to get to that level is specified by "FIND." Both these parameters may be altered to suit specific applications. To cause the program to de-intensify the light source, the sublevels must be decremented rather than incremented.

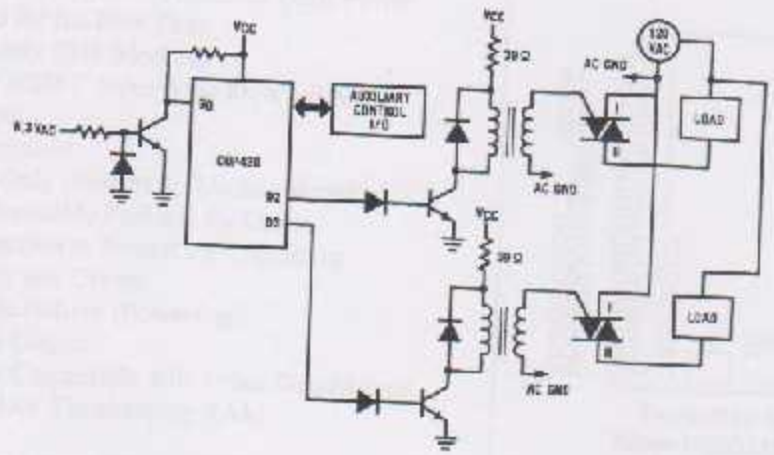


FIGURE 9. Triac Interface for COPS Program

DALLAS SEMICONDUCTOR MAXIM

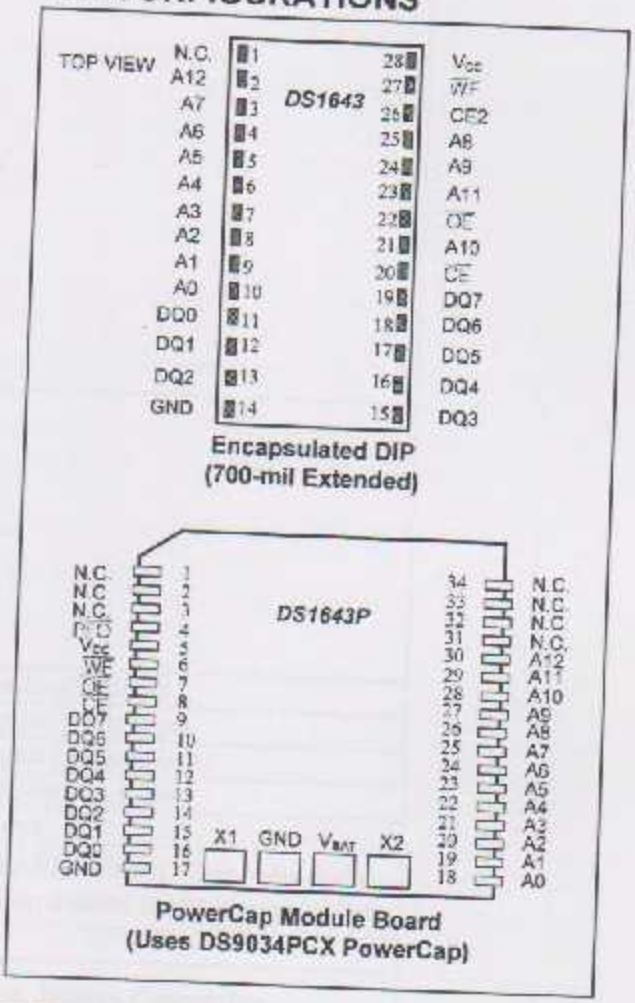
DS1643/DS1643P
Nonvolatile Timekeeping RAMs

www.maxim-ic.com

FEATURES

- Integrated NV SRAM, Real-Time Clock, Crystal, Power-Fail Control Circuit and Lithium Energy Source
- Clock Registers are Accessed Identically to the Static RAM. These Registers Reside in the Eight Top RAM Locations.
- Totally Nonvolatile with Over 10 Years of Operation in the Absence of Power
- Access Times of 70ns and 100ns
- BCD-Coded Year, Month, Date, Day, Hours, Minutes, and Seconds with Leap Year Compensation Valid Up to 2100
- Power-Fail Write Protection Allows for ±10% V_{CC} Power Supply Tolerance
- Lithium Energy Source is Electrically Disconnected to Retain Freshness Until Power is Applied for the First Time
- DS1643 Only (DIP Module)
  - Standard JEDEC Byte-Wide 8K x 8 RAM Pinout
  - UL Recognized
- DS1643P Only (PowerCap Module Board)
  - Surface Mountable Package for Direct Connection to PowerCap Containing Battery and Crystal
  - Replaceable Battery (PowerCap)
  - Power-Fail Output
  - Pin-for-Pin Compatible with Other Densities of DS164XP Timekeeping RAM

PIN CONFIGURATIONS



ORDERING INFORMATION

PART	VOLTAGE RANGE (V)	TEMP RANGE	PIN-PACKAGE	TOP MARK
DS1643-70+	5.0	0°C to +70°C	28 EDIP (0.740a)	DS1643+70
DS1643-70	5.0	0°C to +70°C	28 EDIP (0.740a)	DS1643-70
DS1643+100	5.0	0°C to +70°C	28 EDIP (0.740a)	DS1643+100
DS1643-100	5.0	0°C to +70°C	28 EDIP (0.740a)	DS1643-100
DS1643P-70+	5.0	0°C to +70°C	34-PowerCap*	DS1643P+70
DS1643P-70	5.0	0°C to +70°C	34-PowerCap*	DS1643P-70
DS1643P+100	5.0	0°C to +70°C	34-PowerCap*	DS1643P+100
DS1643P-100	5.0	0°C to +70°C	34-PowerCap*	DS1643P-100

*DS9034-PCX, DS9034I-PCX, DS9034-PCX+ required (must be ordered separately).
"+" indicates a lead-free product. The top mark will include a "+" symbol on lead-free devices.

REV: 042705

PIN DESCRIPTION

PIN		NAME	FUNCTION
PDIP	PowerCap		
1	1, 2, 3, 31–34	N.C.	No Connection
2	30	A12	Address Inputs
3	25	A7	
4	24	A6	
5	23	A5	
6	22	A4	
7	21	A3	
8	20	A2	
9	19	A1	
10	18	A0	
21	28	A10	
23	29	A11	
24	27	A9	
25	26	A8	
11	16	DQ0	Data Input/Output
12	15	DQ1	
13	14	DQ2	
15	13	DQ3	
16	12	DQ4	
17	11	DQ5	
18	10	DQ6	
19	9	DQ7	
20	8	$\overline{CE}$	Active-Low Chip-Enable Input
22	7	$\overline{OE}$	Active-Low Output-Enable Input
26	—	CE2	Chip-Enable 2 Input (Active High)
27	6	$\overline{WE}$	Active-Low Write-Enable Input
28	5	V_{CC}	Power-Supply Input
—	4	$\overline{PFO}$	Active-Low Power-Fail Output. This open-drain pin requires a pullup resistor for proper operation.
14	17	GND	Ground
—		X1, X2, V_{BAT}	Crystal Connection, Battery Connection

DESCRIPTION

The DS1643 is an 8K x 8 nonvolatile static RAM with a full function Real Time Clock (RTC) that are both accessible in a byte-wide format. The nonvolatile timekeeping RAM is functionally equivalent to any JEDEC standard 8K x 8 SRAM. The device can also be easily substituted in ROM, EPROM and EEPROM sockets providing read/write nonvolatility and the addition of the real time clock function. The real time clock information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24-hour BCD format. Corrections for the day of the month and leap year are made automatically. The RTC clock registers are double-buffered to avoid access of incorrect data that can occur during clock update cycles. The double-buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1643 also contains its own power-fail circuitry, which deselects the device when the V_{CC} supply is in an out of tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low V_{CC} as errant access and update cycles are avoided.

PACKAGES

The DS1643 is available in two packages: 28-pin DIP module and 34-pin PowerCap® module. The 28-pin DIP style module integrates the crystal, lithium energy source, and silicon all in one package. The 34-pin PowerCap Module Board is designed with contacts for connection to a separate PowerCap (DS9034PCX) that contains the crystal and battery. This design allows the PowerCap to be mounted on top of the DS1643P after the completion of the surface mount process. Mounting the PowerCap after the surface mount process prevents damage to the crystal and battery due to high temperatures required for solder reflow. The PowerCap is keyed to prevent reverse insertion. The PowerCap Module Board and PowerCap are ordered separately and shipped in separate containers. The part number for the PowerCap is DS9034PCX.

CLOCK OPERATIONS—READING THE CLOCK

While the double-buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1643 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a one is written into the read bit, the seventh most significant bit in the control register. As long as a 1 remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double-buffered system continue to update so that the clock accuracy is not affected by the access of data. All of the DS1643 registers are updated simultaneously after the clock status is reset. Updating is within a second after the read bit is written to 0.

PowerCap is a registered trademark of Dallas Semiconductor.

Figure 1. Block Diagram

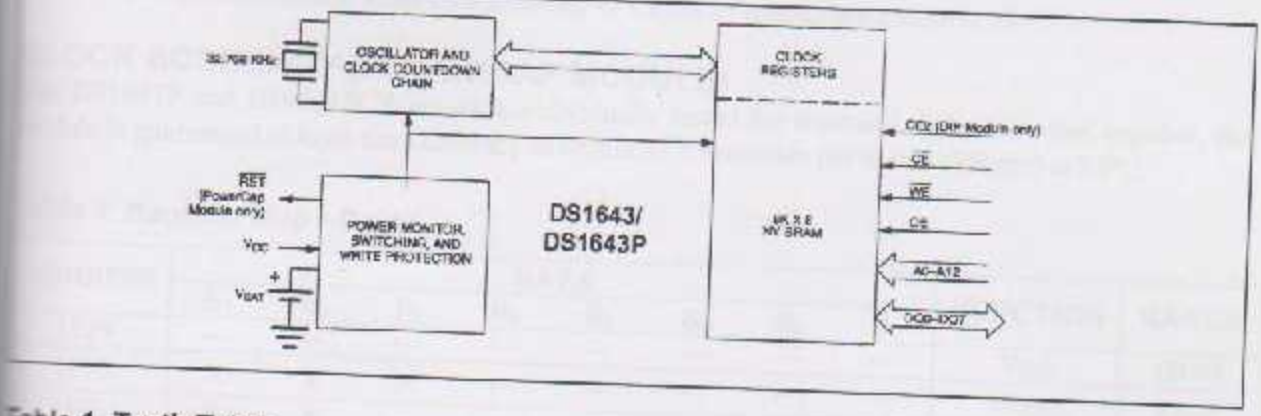


Table 1. Truth Table

V_{CC}	$\overline{CE}$	CE2	$\overline{OE}$	$\overline{WE}$	MODE	DQ	POWER
5V ±10%	V_{IH}	X	X	X	Deselect	High Z	Standby
	X	V_{IL}	X	X	Deselect	High Z	Standby
	V_{IL}	V_{IH}	X	V_{IL}	Write	Data In	Active
	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Read	Data Out	Active
	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Read	High-Z	Active
<4.5V > V_{BAT}	X	X	X	X	Deselect	High-Z	CMOS Standby
<V_{BAT}	X	X	X	X	Deselect	High-Z	Data Retention Mode

SETTING THE CLOCK

The 8-bit of the control register is the write bit. Setting the write bit to a 1, like the read bit, halts updates to the DS1643 registers. The user can then load them with the correct day, date and time data in 24 hour BCD format. Resetting the write bit to a 0 then transfers those values to the actual clock counters and allows normal operation to resume.

STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB for the seconds registers. Setting it to 1 stops the oscillator.

FREQUENCY TEST BIT

Bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic 1 and the oscillator is running, the LSB of the seconds register will toggle at 512Hz. When the seconds register is being read, the DQ0 line will toggle at the 512Hz frequency as long as conditions for access remain valid (i.e., $\overline{CE}$ low, $\overline{OE}$ low, CE2 high, and address for seconds register remain valid and stable).

CLOCK ACCURACY (DIP MODULE)

The DS1643 is guaranteed to keep time accuracy to within ±1 minute per month at 25°C.

CLOCK ACCURACY (POWERCAP MODULE)

The DS1643P and DS9034PCX are each individually tested for accuracy. Once mounted together, the module is guaranteed to keep time accuracy to within ±1.53 minutes per month (35ppm) at 25°C.

Table 2. Register Map—Bank1

ADDRESS	DATA								FUNCTION	RANGE
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1FFF	—	—	—	—	—	—	—	—		
1FFE	X	X	X	—	—	—	—	—	Year	00-99
1FFD	X	X	—	—	—	—	—	—	Month	01-12
1FFC	X	Ft	X	X	X	—	—	—	Date	01-31
1FFB	X	X	—	—	—	—	—	—	Day	01-07
1FFA	X	—	—	—	—	—	—	—	Hour	00-23
1FF9	$\overline{OSC}$	—	—	—	—	—	—	—	Minutes	00-59
1FF8	W	R	X	X	X	X	X	X	Seconds	00-59
									Control	A

OSC = STOP BIT
W = WRITE BIT
R = READ BIT
X = UNUSED
FT = FREQUENCY TEST

Note: All indicated "X" bits are not used but must be set to "0" for proper clock operation.

RETRIEVING DATA FROM RAM OR CLOCK

The DS1643 is in the read mode whenever $\overline{WE}$ (write enable) is high and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within t_{AA} after the last address input is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times and states are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, valid data will be available at the latter of chip enable access (t_{CEA}) or at output enable access time (t_{OEA}). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$ and $\overline{OE}$. If the outputs are activated before t_{AA}, the data lines are driven to an intermediate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain valid, output data will remain valid for output data hold time (t_{OH}) but will then go indeterminate until the next address access.

WRITING DATA TO RAM OR CLOCK

The DS1643 is in the write mode whenever $\overline{WE}$ and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring transition of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return inactive for a minimum of t_{WR} prior to the initiation of another read or write cycle. Data in must be valid t_{DS} prior to the end of write and remain valid for t_{DH} afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the outputs t_{WEZ} after $\overline{WE}$ goes active.

DATA RETENTION MODE

When V_{CC} is within nominal limits (V_{CC} > 4.5V) the DS1643 can be accessed as described above with read or write cycles. However, when V_{CC} is below the power-fail point V_{PF} (point at which write protection occurs) the internal clock registers and RAM are blocked from access. This is accomplished internally by inhibiting access via the $\overline{CE}$ signal. At this time the power-on reset output signal ($\overline{RST}$) will be driven active low and will remain active until V_{CC} returns to nominal levels. When V_{CC} falls below the level of the internal battery supply, power input is switched from the V_{CC} pin to the internal battery and clock activity, RAM, and clock data are maintained from the battery until V_{CC} is returned to nominal level. The $\overline{RST}$ signal is an open drain output and requires a pull up. Except for the $\overline{RST}$, all control, data, and address signals must be powered down when V_{CC} is powered down.

BATTERY LONGEVITY

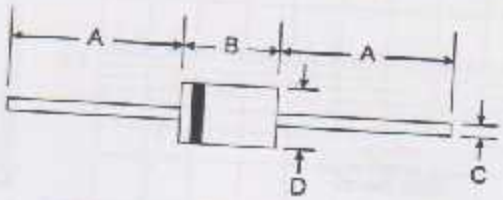
The DS1643 has a lithium power source that is designed to provide energy for clock activity, and clock and RAM data retention when the V_{CC} supply is not present. The capability of this internal power supply is sufficient to power the DS1643 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at 25°C with the internal clock oscillator running in the absence of V_{CC} power. Each DS1643 is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than V_{PF}, the lithium energy source is enabled for battery backup operation. Actual life expectancy of the DS1643 will be much longer than 10 years since no lithium battery energy is consumed when V_{CC} is present.

1N4001/L - 1N4007/L

1.0A RECTIFIER

Features

- Diffused Junction
- High Current Capability and Low Forward Voltage Drop
- Surge Overload Rating to 30A Peak
- Low Reverse Leakage Current
- Plastic Material: UL Flammability Classification Rating 94V-0



	DO-41 Plastic		A-405	
Dim	Min	Max	Min	Max
A	25.40	—	25.40	—
B	4.06	5.21	4.10	5.20
C	0.71	0.864	0.53	0.64
D	2.00	2.72	2.00	2.70
All Dimensions in mm				

"L" Suffix Designates A-405 Package
No Suffix Designates DO-41 Package

Mechanical Data

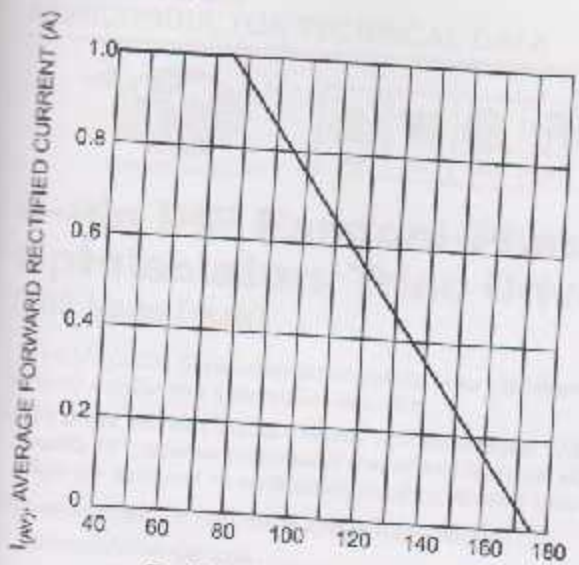
- Case: Molded Plastic
- Terminals: Plated Leads Solderable per MIL-STD-202, Method 208
- Polarity: Cathode Band
- Weight: DO-41 0.30 grams (approx)
  A-405 0.20 grams (approx)
- Mounting Position: Any
- Marking: Type Number

Maximum Ratings and Electrical Characteristics @ T_A = 25°C unless otherwise specified

Single phase, half wave, 60Hz, resistive or inductive load.
For capacitive load, derate current by 20%.

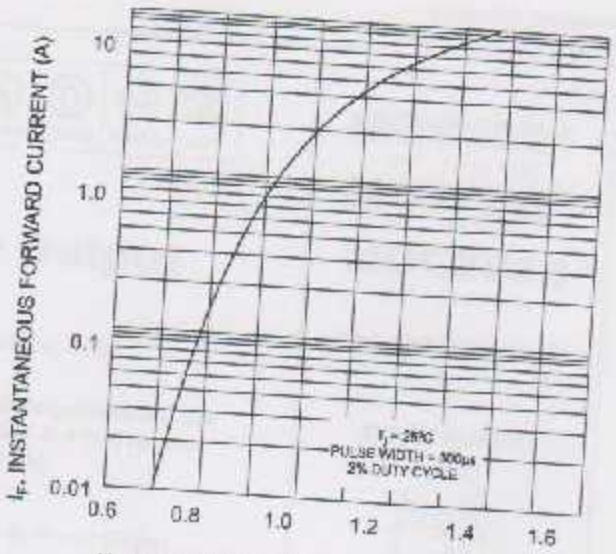
Characteristic	Symbol	1N 4001/L	1N 4002/L	1N 4003/L	1N 4004/L	1N 4005/L	1N 4006/L	1N 4007/L	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	800	1000	V
RMS Reverse Voltage	$V_{R(RMS)}$	35	70	140	280	420	560	700	V
Average Rectified Output Current (Note 1) @ T_A = 75°C	I_O	1.0							A
Non-Repetitive Peak Forward Surge Current 8.3ms single half sine-wave superimposed on rated load (JEDEC Method)	I_{FSM}	30							A
Forward Voltage @ I_F = 1.0A	V_{FM}	1.0							V
Peak Reverse Current @ T_A = 25°C at Rated DC Blocking Voltage @ T_A = 100°C	I_{RM}	5.0 50							µA
Typical Junction Capacitance (Note 2)	C_j	15				8			pF
Typical Thermal Resistance Junction to Ambient	$R_{\theta JA}$	100							K/W
Maximum DC Blocking Voltage Temperature	T_A	+150							°C
Operating and Storage Temperature Range (Note 3)	T_j, T_{STG}	-65 to +175							°C

Notes: 1. Leads maintained at ambient temperature at a distance of 9.5mm from the case.
2. Measured at 1. MHz and applied reverse voltage of 4.0V DC.
3. JEDEC Value



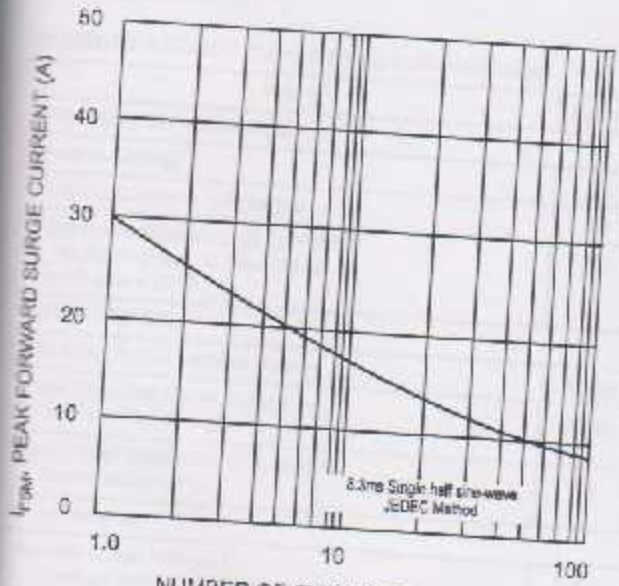
T_A, AMBIENT TEMPERATURE (°C)

Fig. 1 Forward Current Derating Curve



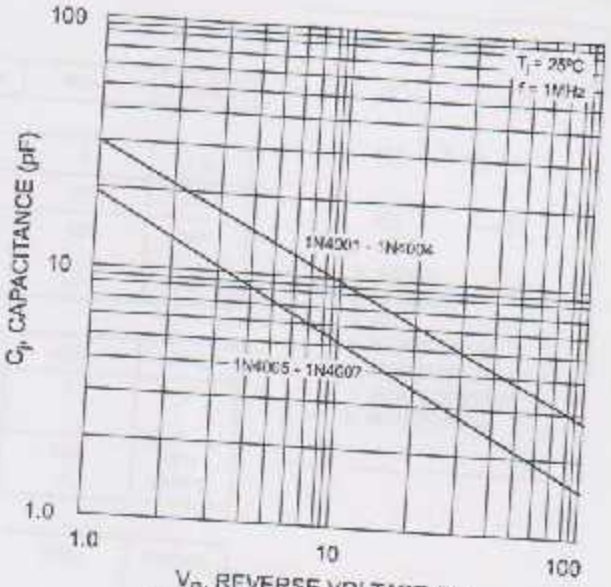
V_F, INSTANTANEOUS FORWARD VOLTAGE (V)

Fig. 2 Typical Forward Characteristics



NUMBER OF CYCLES AT 60 Hz

Fig. 3 Max Non-Repetitive Peak Fwd Surge Current



V_R, REVERSE VOLTAGE (V)

Fig. 4 Typical Junction Capacitance

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by MOC3020/D

GlobalOptoisolator™

VDE | UL | CSA | SETI | SEMKO | DEMKO | NEMKO | SABT

6-Pin DIP Random-Phase Optoisolators Triac Driver Output
(400 Volts Peak)

MOC3021
(IFT = 15 mA Max)
MOC3022
(IFT = 10 mA Max)
MOC3023*
(IFT = 5 mA Max)

*Motorola Preferred Device

The MOC3020 Series consists of gallium arsenide infrared emitting diodes, optically coupled to a silicon bilateral switch.

- ***To order devices that are tested and marked per VDE 0884 requirements, the suffix "V" must be included at end of part number. VDE 0884 is a test option.***

They are designed for applications requiring isolated triac triggering.

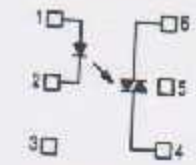
Recommended for 115/240 Vac(rms) Applications:

- Solenoid/Valve Controls
- Lamp Ballasts
- Interfacing Microprocessors to 115 Vac Peripherals
- Motor Controls
- Static ac Power Switch
- Solid State Relays
- Incandescent Lamp Dimmers

STYLE 6 PLASTIC

STANDARD THRU HOLE
CASE 730A–04

SCHEMATIC



1. ANODE
2. CATHODE
3. NC
4. MAIN TERMINAL
5. SUBSTRATE
   DO NOT CONNECT
6. MAIN TERMINAL

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INFRARED EMITTING DIODE			
Reverse Voltage	V_R	3	Volts
Forward Current — Continuous	I_F	60	mA
Total Power Dissipation @ T_A = 25°C Negligible Power in Triac Driver Derate above 25°C	P_D	100 1.33	mW mW/°C
OUTPUT DRIVER			
Off-State Output Terminal Voltage	V_{DRM}	400	Volts
Peak Repetitive Surge Current (PW = 1 ms, 120 pps)	I_{TSM}	1	A
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 4	mW mW/°C
TOTAL DEVICE			
Isolation Surge Voltage(1) (Peak ac Voltage, 60 Hz, 1 Second Duration)	V_{ISO}	7500	Vac(pk)
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	330 4.4	mW mW/°C
Junction Temperature Range	T_J	−40 to +100	°C
Ambient Operating Temperature Range(2)	T_A	−40 to +85	°C
Storage Temperature Range(2)	T_{stg}	−40 to +150	°C
Soldering Temperature (10 s)	T_L	260	°C

1. Isolation surge voltage, V_{ISO}, is an internal device dielectric breakdown rating.
   For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.
2. Refer to Quality and Reliability Section in Opto Data Book for information on test conditions.

Preferred devices are Motorola recommended choices for future use and best overall value.
GlobalOptoisolator is a trademark of Motorola, Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
INPUT LED						
Reverse Leakage Current (V_R = 3 V)		I_R	—	0.05	100	μA
Forward Voltage (I_F = 10 mA)		V_F	—	1.15	1.5	Volts
OUTPUT DETECTOR (I_F = 0 unless otherwise noted)						
Peak Blocking Current, Either Direction (Rated V_{DRM}(1))		I_{DRM}	—	10	100	nA
Peak On-State Voltage, Either Direction (I_{TM} = 100 mA Peak)		V_{TM}	—	1.8	3	Volts
Critical Rate of Rise of Off-State Voltage (Figure 7, Note 2)		dv/dt	—	10	—	V/μs
COUPLED						
LED Trigger Current, Current Required to Latch Output (Main Terminal Voltage = 3 V(3))	MOC3021 MOC3022 MOC3023	I_{FT}	— — —	5 — —	15 10 5	mA
Holding Current, Either Direction		I_H	—	100	—	μA

1. Test voltage must be applied within dv/dt rating.
2. This is static dv/dt. See Figure 7 for test circuit. Commutating dv/dt is a function of the load-driving thyristor(s) only.
3. All devices are guaranteed to trigger at an I_F value less than or equal to max I_{FT}. Therefore, recommended operating I_F lies between max I_{FT} (15 mA for MOC3021, 10 mA for MOC3022, 5 mA for MOC3023) and absolute max I_F (60 mA).

TYPICAL ELECTRICAL CHARACTERISTICS

T_A = 25°C

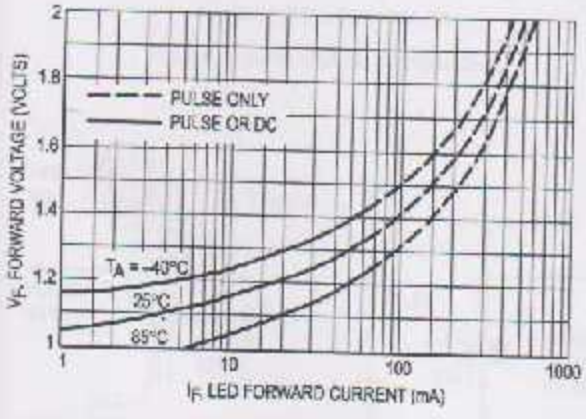


Figure 1. LED Forward Voltage versus Forward Current

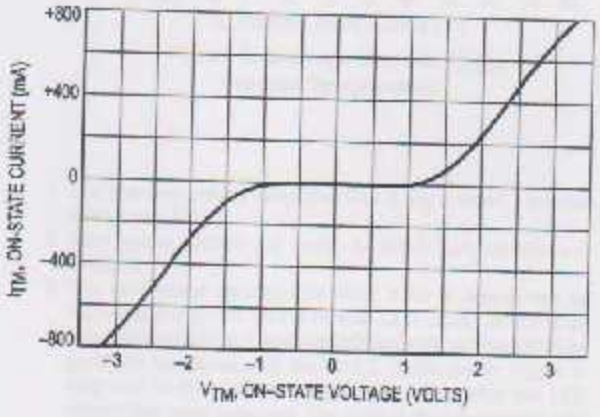


Figure 2. On-State Characteristics

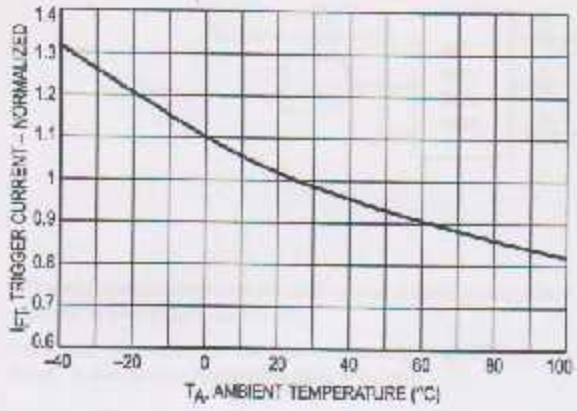


Figure 3. Trigger Current versus Temperature

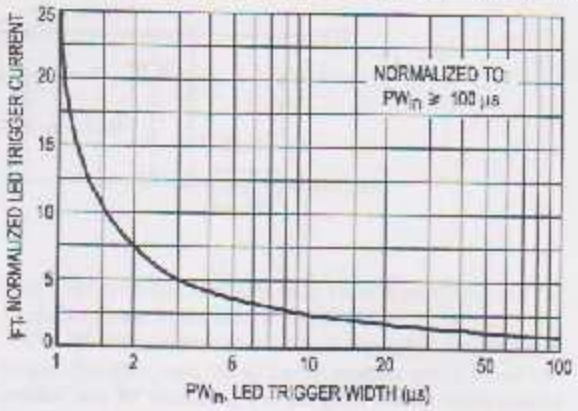


Figure 4. LED Current Required to Trigger versus LED Pulse Width

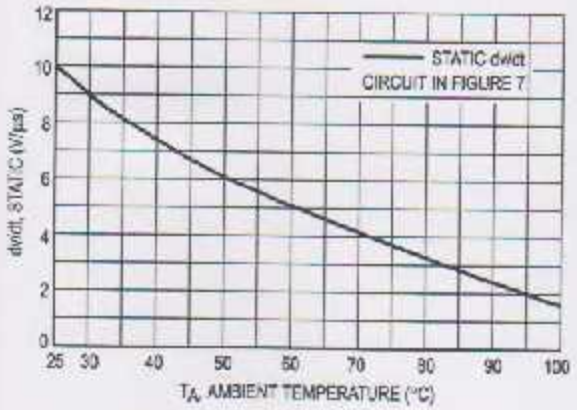


Figure 5. dv/dt versus Temperature

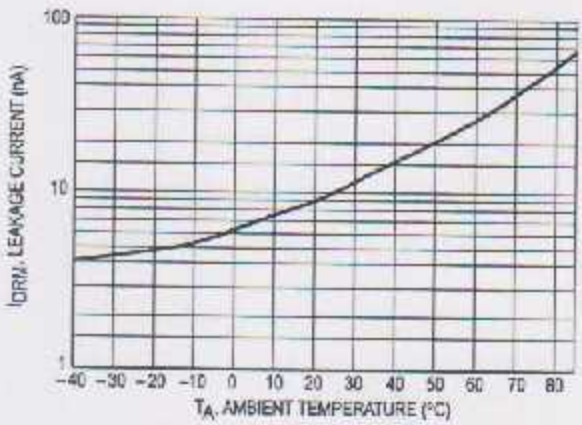
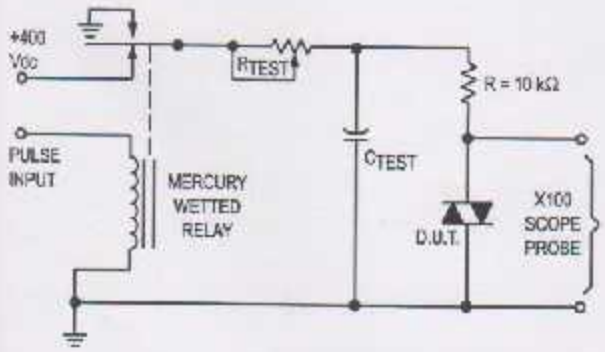


Figure 6. Leakage Current, I_{DRM} versus Temperature



1. The mercury wetted relay provides a high speed repeated pulse to the D.U.T.
2. 100x scope probes are used, to allow high speeds and voltages.
3. The worst–case condition for static dv/dt is established by triggering the D.U.T. with a normal LED input current, then removing the current. The variable R_{TEST} allows the dv/dt to be gradually increased until the D.U.T. continues to trigger in response to the applied voltage pulse, even after the LED current has been removed. The dv/dt is then decreased until the D.U.T. stops triggering. τ_{RC} is measured at this point and recorded.

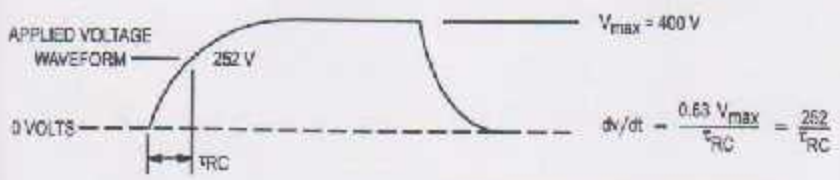
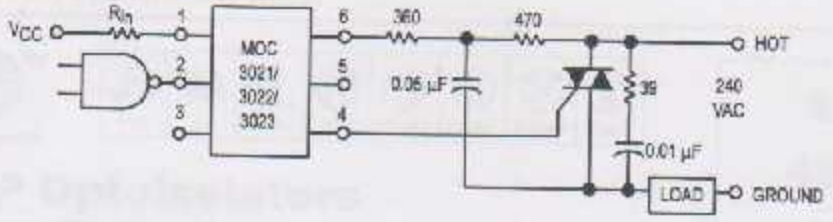


Figure 7. Static dv/dt Test Circuit



* This optoisolator should not be used to drive a load directly. It is intended to be a trigger device only.

Additional information on the use of optically coupled triac drivers is available in Application Note AN-780A.

In this circuit the "hot" side of the line is switched and the load connected to the cold or ground side.

The 39 ohm resistor and 0.01 µF capacitor are for snubbing of the triac, and the 470 ohm resistor and 0.05 µF capacitor are for snubbing the coupler. These components may or may not be necessary depending upon the particular triac and load used.

Figure 8. Typical Application Circuit

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Order this document
by 4N25/D

GlobalOptoisolator™

VDE | UL | CSA | FIMKO | SEMKO | DEMKO | NEMKO | BAST

6-Pin DIP Optoisolators Transistor Output

4N25*
4N25A*
4N26*
[CTR = 20% Min]
4N27
4N28
[CTR = 10% Min]
*Motorola Preferred Devices

The 4N25/A, 4N26, 4N27 and 4N28 devices consist of a gallium arsenide infrared emitting diode optically coupled to a monolithic silicon phototransistor detector.

- Most Economical Optoisolator Choice for Medium Speed, Switching Applications
- Meets or Exceeds All JEDEC Registered Specifications
- ***To order devices that are tested and marked per VDE 0884 requirements, the suffix "V" must be included at end of part number. VDE 0884 is a test option.***

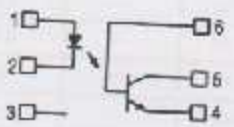
Applications

- General Purpose Switching Circuits
- Interfacing and coupling systems of different potentials and impedances
- I/O Interfacing
- Solid State Relays

STYLE 1 PLASTIC

STANDARD THRU HOLE
CASE 730A–04

SCHEMATIC



PIN 1. LED ANODE
2. LED CATHODE
3. N.C.
4. EMITTER
5. COLLECTOR
6. BASE

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT LED			
Reverse Voltage	V_R	3	Volts
Forward Current — Continuous	I_F	60	mA
LED Power Dissipation @ T_A = 25°C with Negligible Power in Output Detector Derate above 25°C	P_D	120 1.41	mW mW/°C
OUTPUT TRANSISTOR			
Collector–Emitter Voltage	V_{CEO}	30	Volts
Emitter–Collector Voltage	V_{ECO}	7	Volts
Collector–Base Voltage	V_{CBO}	70	Volts
Collector Current — Continuous	I_C	150	mA
Detector Power Dissipation @ T_A = 25°C with Negligible Power in Input LED Derate above 25°C	P_D	150 1.76	mW mW/°C
TOTAL DEVICE			
Isolation Surge Voltage(1) (Peak ac Voltage, 60 Hz, 1 sec Duration)	V_{ISO}	7500	Vac(pk)
Total Device Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	250 2.94	mW mW/°C
Ambient Operating Temperature Range(2)	T_A	−55 to +100	°C
Storage Temperature Range(2)	T_{stg}	−55 to +150	°C
Soldering Temperature (10 sec, 1/16" from case)	T_L	260	°C

1. Isolation surge voltage is an internal device dielectric breakdown rating. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.
2. Refer to Quality and Reliability Section in Opto Data Book for information on test conditions.

Preferred devices are Motorola recommended choices for future use and best overall value.
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REV 5

MOTOROLA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Min	Typ(1)	Max	Unit
INPUT LED						
Forward Voltage (I_F = 10 mA)	T_A = 25°C T_A = −55°C T_A = 100°C	V_F	— — —	1.15 1.3 1.05	1.5 — —	Volts
Reverse Leakage Current (V_R = 3 V)		I_R	—	—	100	μA
Capacitance (V = 0 V, f = 1 MHz)		C_J	—	18	—	pF
OUTPUT TRANSISTOR						
Collector–Emitter Dark Current (V_{CE} = 10 V, T_A = 25°C (V_{CE} = 10 V, T_A = 100°C)	4N25,25A,26,27 4N28 All Devices	I_{CEO}	— —	1 1	50 100	nA
Collector–Base Dark Current (V_{CB} = 10 V)		I_{CEO}	—	1	—	μA
Collector–Emitter Breakdown Voltage (I_C = 1 mA)		I_{CBO}	—	0.2	—	nA
Collector–Base Breakdown Voltage (I_C = 100 μA)		$V_{(BR)CEO}$	30	45	—	Volts
Emitter–Collector Breakdown Voltage (I_E = 100 μA)		$V_{(BR)CBO}$	70	100	—	Volts
DC Current Gain (I_C = 2 mA, V_{CE} = 5 V)		$V_{(BR)ECO}$	7	7.8	—	Volts
Collector–Emitter Capacitance (f = 1 MHz, V_{CE} = 0)		h_{FE}	—	500	—	—
Collector–Base Capacitance (f = 1 MHz, V_{CB} = 0)		C_{CE}	—	7	—	pF
Emitter–Base Capacitance (f = 1 MHz, V_{EB} = 0)		C_{CB}	—	19	—	pF
		C_{EB}	—	8	—	pF
COUPLED						
Output Collector Current (I_F = 10 mA, V_{CE} = 10 V)	4N25,25A,26 4N27,28	I_C (CTR)(2)	2 (20) 1 (10)	7 (70) 5 (50)	— —	mA (%)
Collector–Emitter Saturation Voltage (I_C = 2 mA, I_F = 50 mA)		$V_{CE(sat)}$	—	0.15	0.5	Volts
Turn–On Time (I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)(3)		t_{on}	—	2.8	—	μs
Turn–Off Time (I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)(3)		t_{off}	—	4.5	—	μs
Rise Time (I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)(3)		t_r	—	1.2	—	μs
Fall Time (I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)(3)		t_f	—	1.3	—	μs
Isolation Voltage (f = 60 Hz, t = 1 sec)(4)		V_{ISO}	7500	—	—	Vac(pk)
Isolation Resistance (V = 500 V)(4)		R_{ISO}	10^{11}	—	—	Ω
Isolation Capacitance (V = 0 V, f = 1 MHz)(4)		C_{ISO}	—	0.2	—	pF

1. Always design to the specified minimum/maximum electrical limits (where applicable).
2. Current Transfer Ratio (CTR) = I_C/I_F x 100%.
3. For test circuit setup and waveforms, refer to Figure 11.
4. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.

TYPICAL CHARACTERISTICS

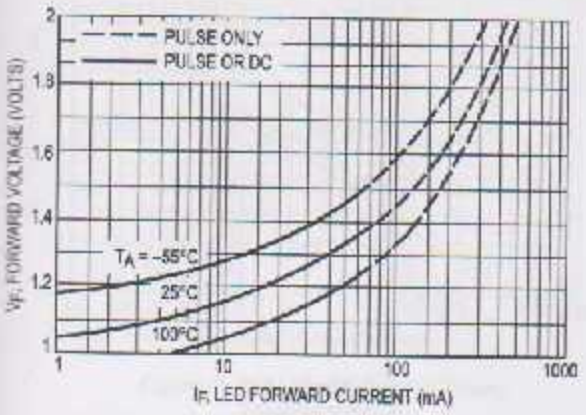

Figure 1. LED Forward Voltage versus Forward Current

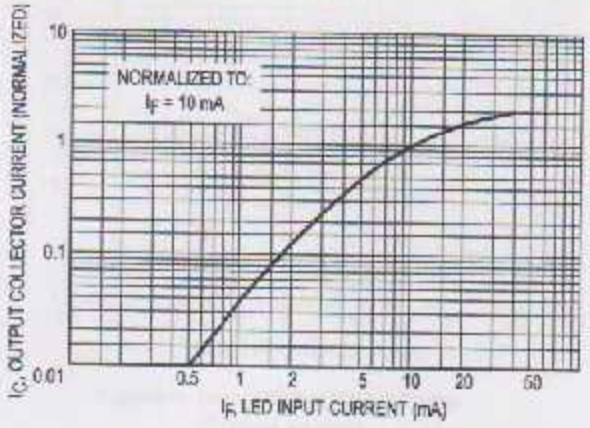

Figure 2. Output Current versus Input Current

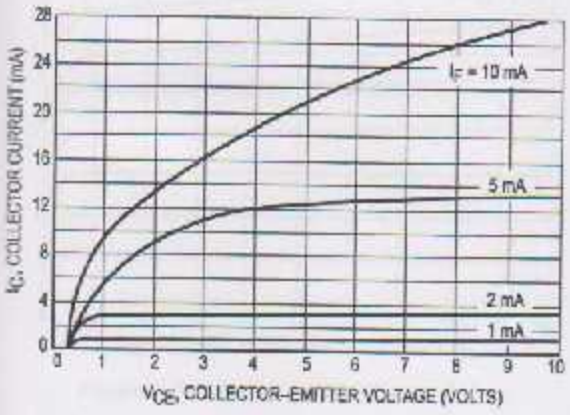

Figure 3. Collector Current versus Collector–Emitter Voltage

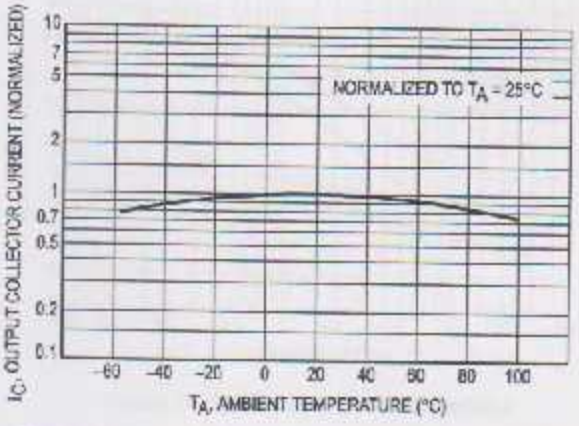

Figure 4. Output Current versus Ambient Temperature

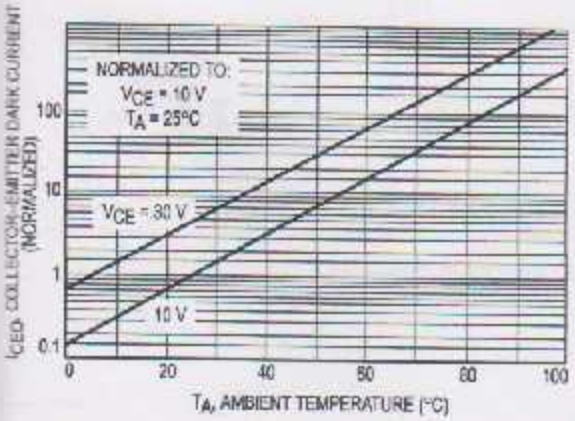

Figure 5. Dark Current versus Ambient Temperature

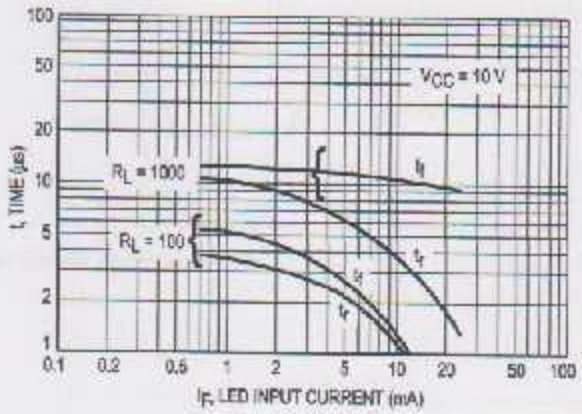

Figure 6. Rise and Fall Times (Typical Values)

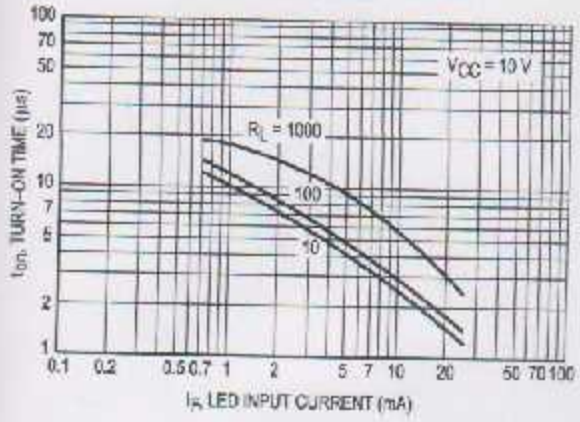

Figure 7. Turn–On Switching Times (Typical Values)

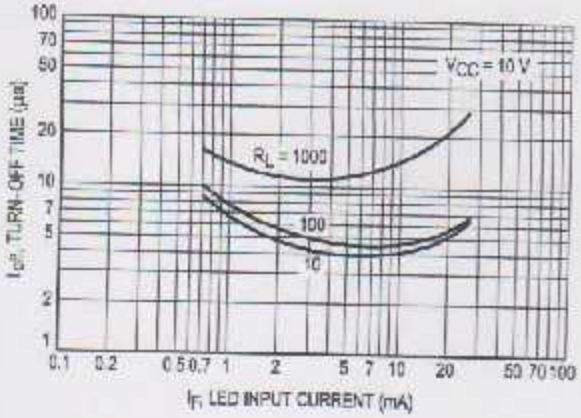

Figure 8. Turn–Off Switching Times (Typical Values)

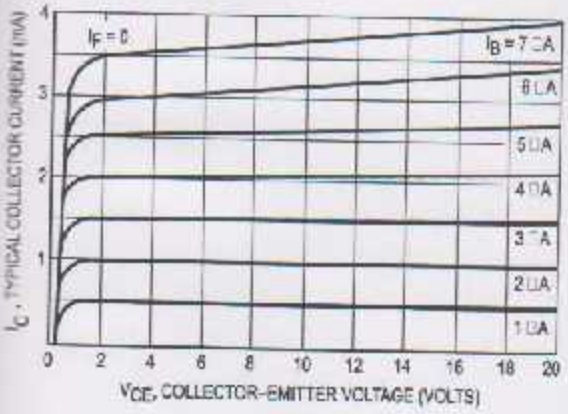

Figure 9. DC Current Gain (Detector Only)

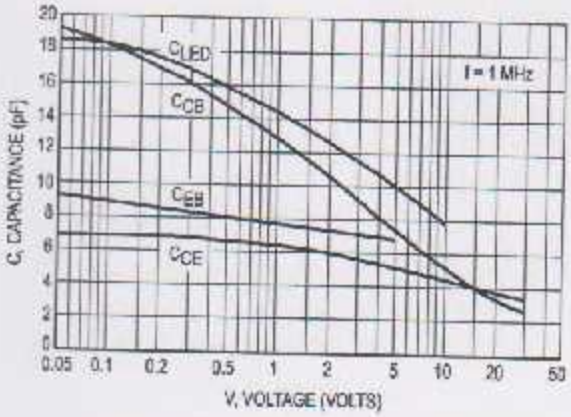

Figure 10. Capacitances versus Voltage

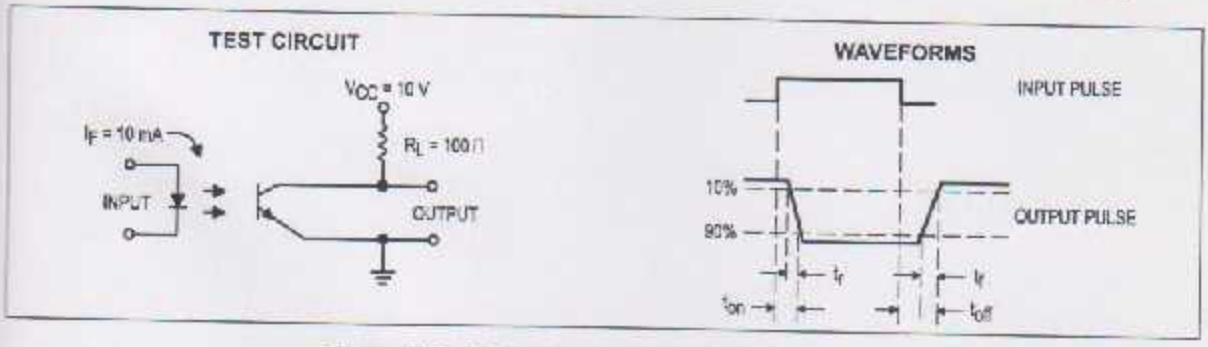

Figure 11. Switching Time Test Circuit and Waveforms