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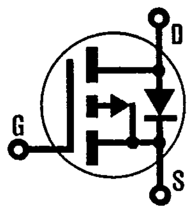
INTERNATIONAL RECTIFIER

Data Sheet No. PD-9.320F
T-39-21

INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRF9530 IRF9531 IRF9532 IRF9533



P-Channel

TO-220

-100 Volt, 0.3 Ohm HEXFET TO-220AB Plastic Package

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-Channel HEXFETs are designed for applications which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel HEXFETs such as voltage control, very fast switching, ease of paralleling, and excellent temperature stability. The P-Channel IRF9530 device is an approximate electrical complement to the N-Channel IRF520 HEXFET.

P-Channel HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuit and pulse amplifiers.

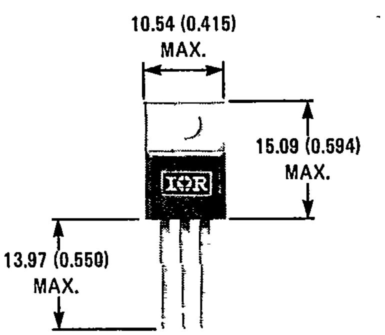
Features:

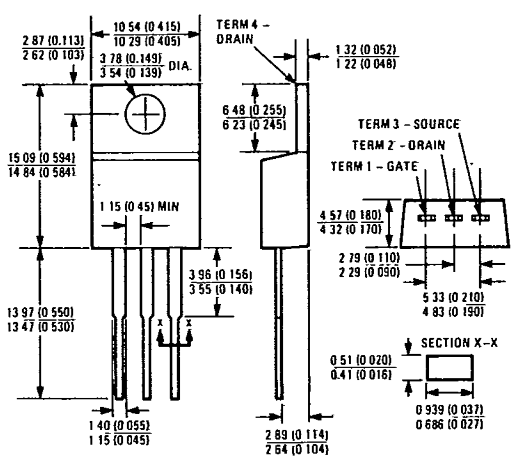
- P-Channel Versatility
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- Excellent Temperature Stability

Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF9530	-100V	0.30Ω	-12A
IRF9531	-60V	0.30Ω	-12A
IRF9532	-100V	0.40Ω	-10A
IRF9533	-60V	0.40Ω	-10A

CASE STYLE AND DIMENSIONS





Case Style TO-220AB
Dimensions in Millimeters and (Inches)

IRF9530, IRF9531, IRF9532, IRF9533 Devices

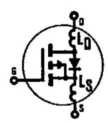
Absolute Maximum Ratings

	Parameter	IRF9530	IRF9531	IRF9532	IRF9533	Units
V_{DS}	Drain - Source Voltage ①	-100	-60	-100	-60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	-100	-60	-100	-60	V
I_D @ T_C = 25°C	Continuous Drain Current	-12	-12	-10	-10	A
I_D @ T_C = 100°C	Continuous Drain Current	-7.5	-7.5	-6.5	-6.5	A
I_{DM}	Pulsed Drain Current ③	-48	-48	-40	-40	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/K④
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH -48	-48	-40	-40	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF9530 IRF9532	-100	—	—	V	V_{GS} = 0V
		IRF9531 IRF9533	-60	—	—	V	I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	-500	nA	V_{GS} = -20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	500	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF9530 IRF9531	-12	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = -10V
		IRF9532 IRF9533	-10	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF9530 IRF9531	—	0.25	0.30	Ω	V_{GS} = -10V, I_D = -6.5A
		IRF9532 IRF9533	—	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.0	3.8	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = -6.5A
C_{iss}	Input Capacitance	ALL	—	500	700	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	300	450	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	100	200	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	30	60	ns	V_{DD} = 0.5 BV_{DSS}, I_D = -6.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	70	140	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	70	140	ns	
t_f	Fall Time	ALL	—	70	140	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	25	45	nC	V_{GS} = -15V, I_D = -15A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	13	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	12	—	nC	
L_D	Internal Drain Inductance	ALL	—	3.5	—	nH	Measured from the contact screw on tab to center of die.
			—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	1.67	K/W④	
R_{thCS}	Case-to-Sink	ALL	—	1.0	—	K/W④	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	80	K/W④	Typical socket mount

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF9530 IRF9531	—	—	-12	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRF9532 IRF9533	—	—	-10	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF9530 IRF9531	—	—	-48	A	
		IRF9532 IRF9533	—	—	-40	A	
V_{SD}	Diode Forward Voltage ②	IRF9530 IRF9531	—	—	-6.3	V	T_C = 25°C, I_S = −12A, V_{GS} = 0V.
		IRF9532 IRF9533	—	—	-6.0	V	T_C = 25°C, I_S = −10A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	—	300	—	ns	T_J = 150°C, I_F = −12A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	—	1.8	—	μC	T_J = 150°C, I_F = −12A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

④ K/W = °C/W
W/K = W/°C

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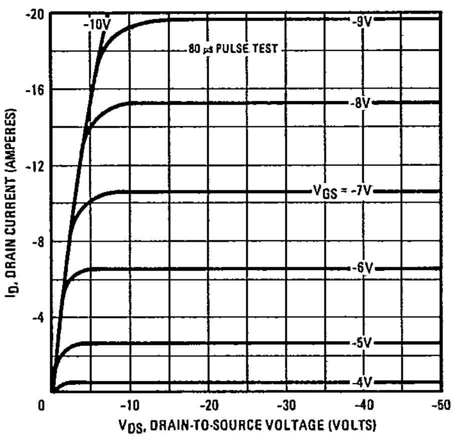


Fig. 1 — Typical Output Characteristics

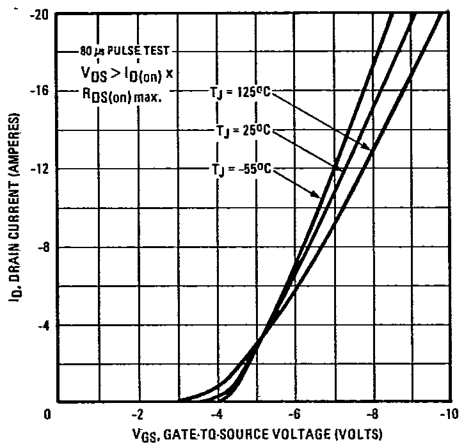


Fig. 2 — Typical Transfer Characteristics

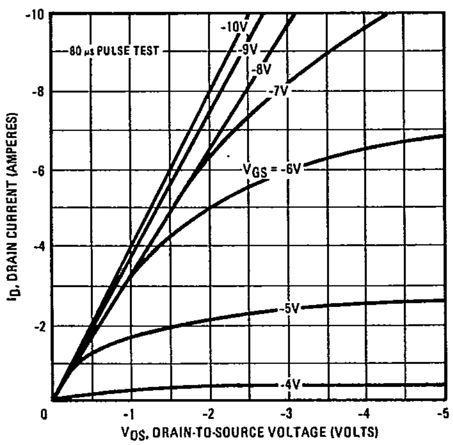


Fig. 3 — Typical Saturation Characteristics

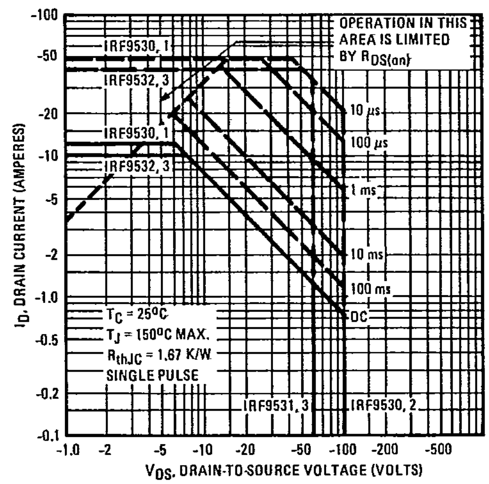


Fig. 4 — Maximum Safe Operating Area

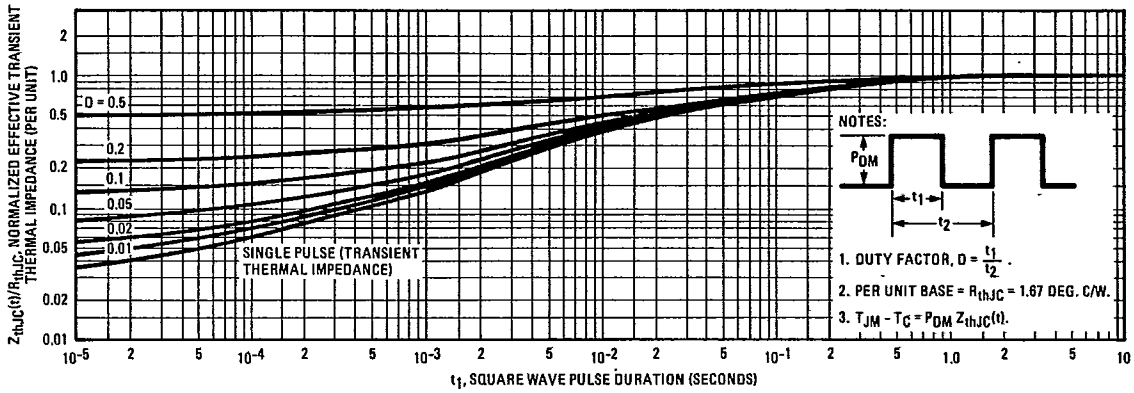


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

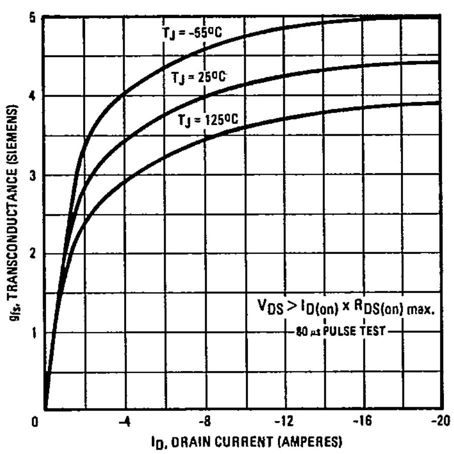


Fig. 6 — Typical Transconductance Vs. Drain Current

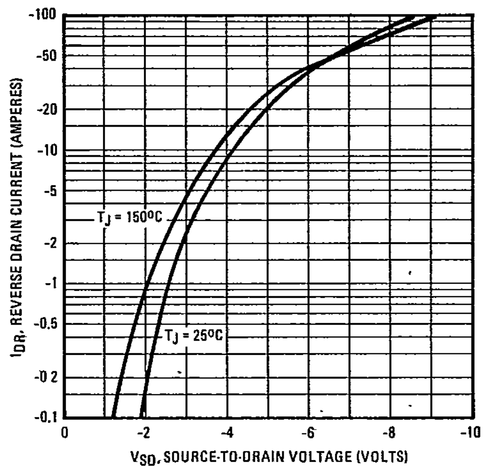


Fig. 7 — Typical Source-Drain Diode Forward Voltage

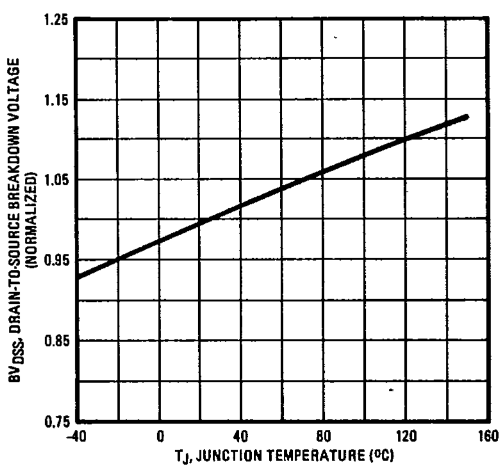


Fig. 8 — Breakdown Voltage Vs. Temperature

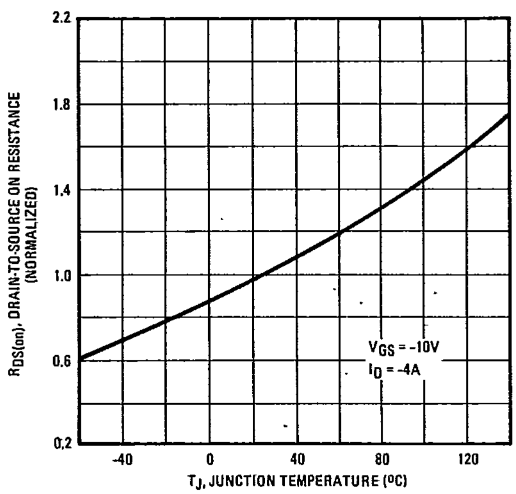


Fig. 9 — Normalized On-Resistance Vs. Temperature

IRF9530, IRF9531, IRF9532, IRF9533 Devices

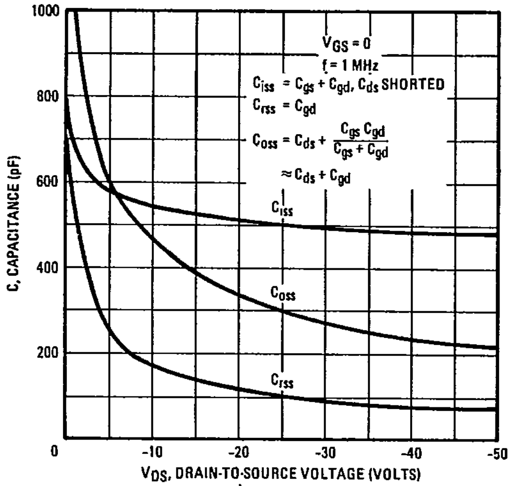


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

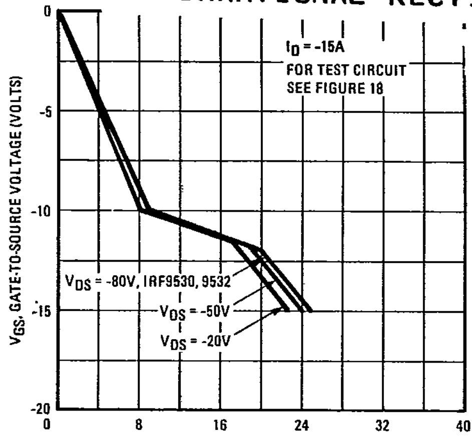


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

TO-220

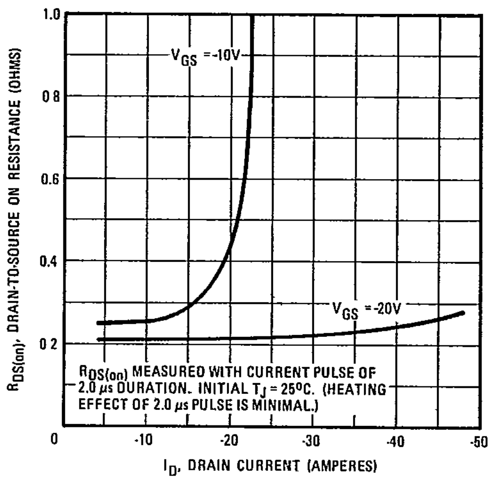


Fig. 12 – Typical On-Resistance Vs. Drain Current

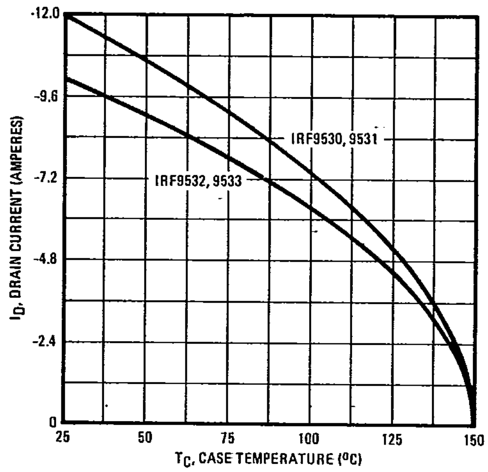


Fig. 13 – Maximum Drain Current Vs. Case Temperature

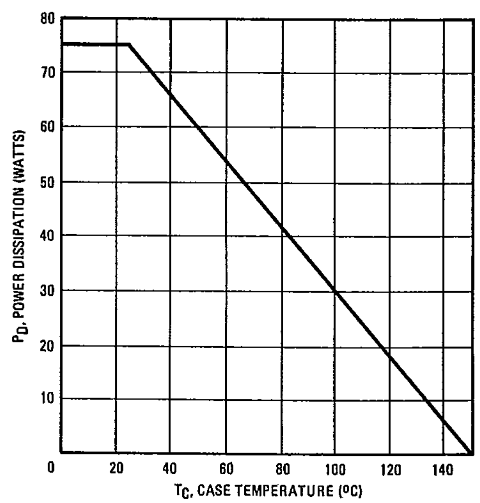


Fig. 14 – Power Vs. Temperature Derating Curve

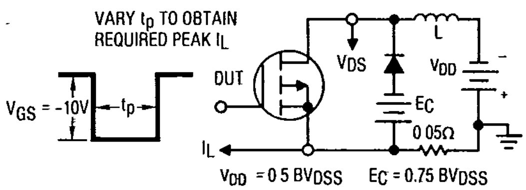


Fig. 15 — Clamped Inductive Test Circuit

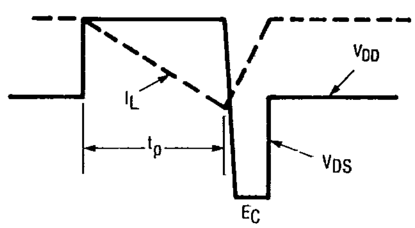


Fig. 16 — Clamped Inductive Waveforms

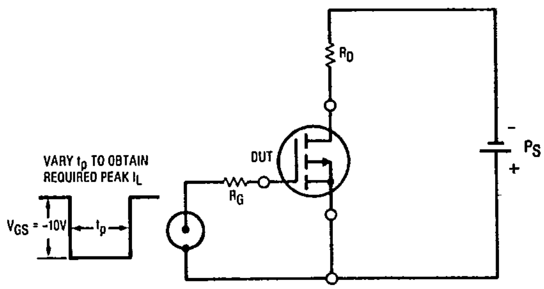


Fig. 17 – Switching Time Test Circuit

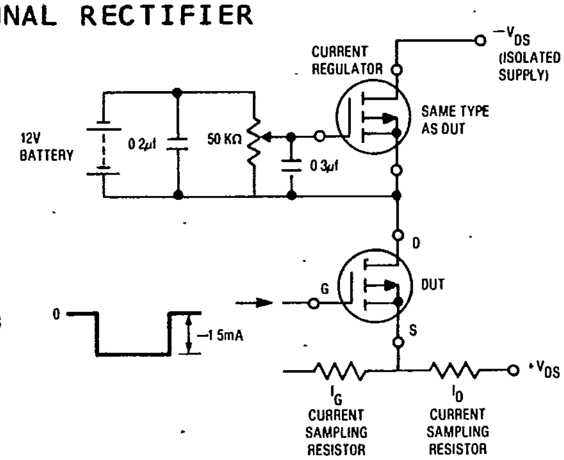


Fig. 18 – Gate Charge Test Circuit

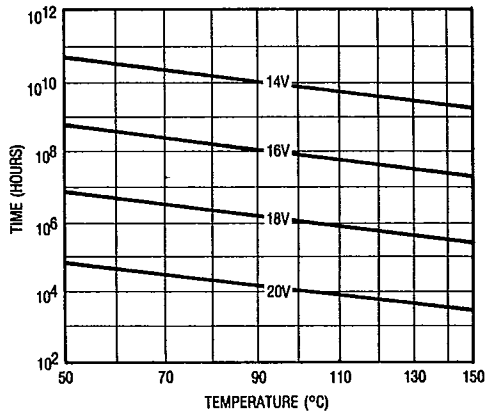


*Fig. 19 – Typical Time to Accumulated 1% Failure

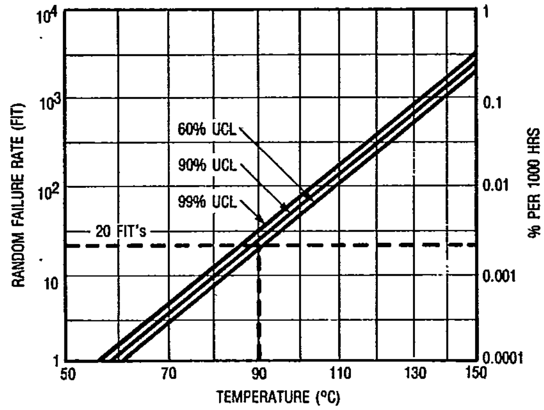


*Fig. 20 – Typical High Temperature Reverse Bias (HTRB) Failure Rate

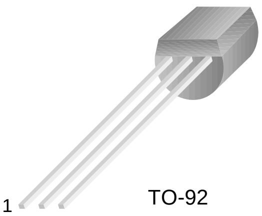
*The data shown is correct as of April 15, 1987. This information is updated on a quarterly basis; for the latest reliability data, please contact your local IR field office.

FAIRCHILD
SEMICONDUCTOR®

BC327/328

Switching and Amplifier Applications

- Suitable for AF-Driver stages and low power output stages
- Complement to BC337/BC338



1 TO-92

1. Collector 2. Base 3. Emitter

PNP Epitaxial Silicon Transistor

Absolute Maximum Ratings T_a=25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CES}	Collector-Emitter Voltage : BC327 : BC328	 -50 -30	 V V
V_{CEO}	Collector-Emitter Voltage : BC327 : BC328	 -45 -25	 V V
V_{EBO}	Emitter-Base Voltage	-5	V
I_C	Collector Current (DC)	-800	mA
P_C	Collector Power Dissipation	625	mW
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C

Electrical Characteristics T_a=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BV_{CEO}	Collector-Emitter Breakdown Voltage : BC327 : BC328	I_C= -10mA, I_B=0	 -45 -25			 V V
BV_{CES}	Collector-Emitter Breakdown Voltage : BC327 : BC328	I_C= -0.1mA, V_{BE}=0	 -50 -30			 V V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E= -10µA, I_C=0	-5			V
I_{CES}	Collector Cut-off Current : BC327 : BC328	 V_{CE}= -45V, V_{BE}=0 V_{CE}= -25V, V_{BE}=0		 -2 -2	 -100 -100	 nA nA
h_{FE1} h_{FE2}	DC Current Gain	V_{CE}= -1V, I_C= -100mA V_{CE}= -1V, I_C= -300mA	100 40		630	
V_{CE} (sat)	Collector-Emitter Saturation Voltage	I_C= -500mA, I_B= -50mA			-0.7	V
V_{BE} (on)	Base-Emitter On Voltage	V_{CE}= -1V, I_C= -300mA			-1.2	V
f_T	Current Gain Bandwidth Product	V_{CE}= -5V, I_C= -10mA, f=20MHz		100		MHz
C_{ob}	Output Capacitance	V_{CB}= -10V, I_E=0, f=1MHz		12		pF

h_{FE} Classification

Classification	16	25	40
h_{FE1}	100 ~ 250	160 ~ 400	250 ~ 630
h_{FE2}	60-	100-	170-

Typical Characteristics

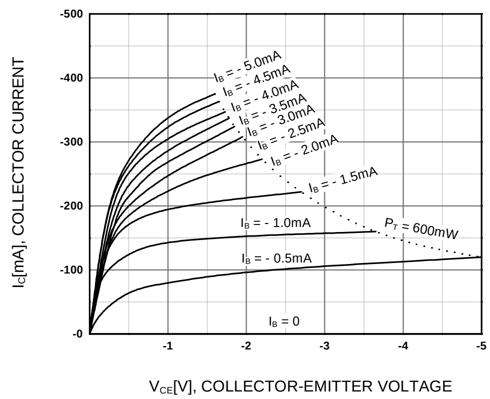


Figure 1. Static Characteristic

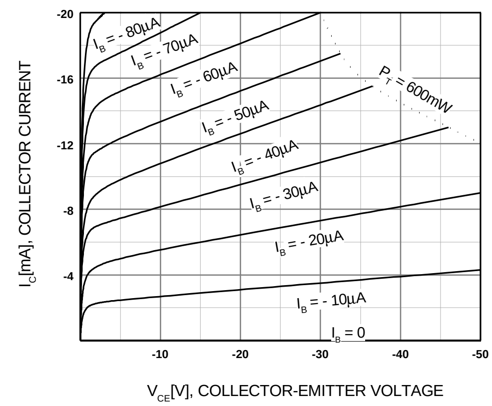


Figure 2. Static Characteristic

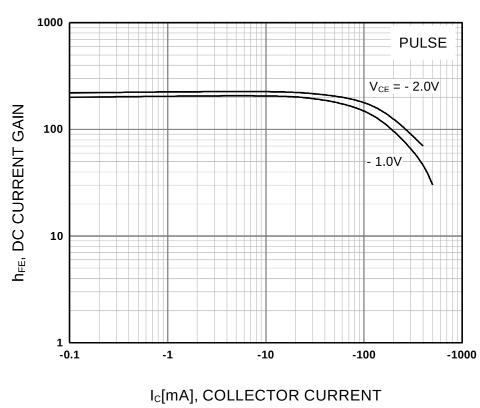


Figure 3. DC current Gain

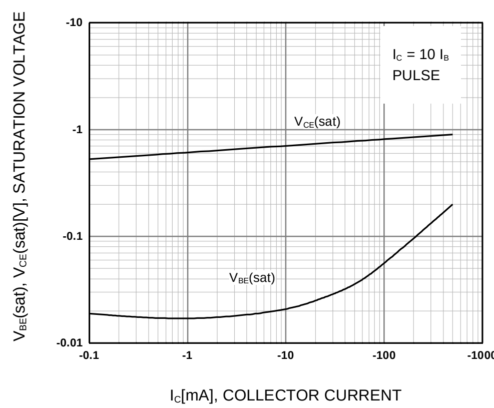


Figure 4. Base-Emitter Saturation Voltage Collector-Emitter Saturation Voltage

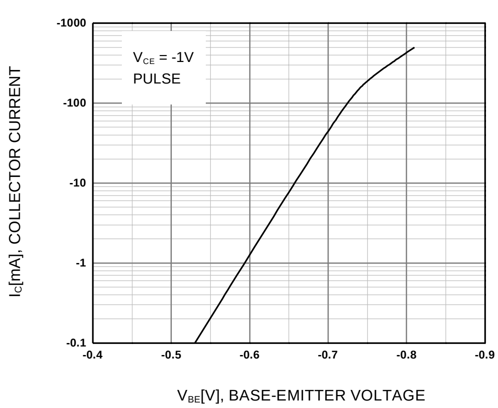


Figure 5. Base-Emitter On Voltage

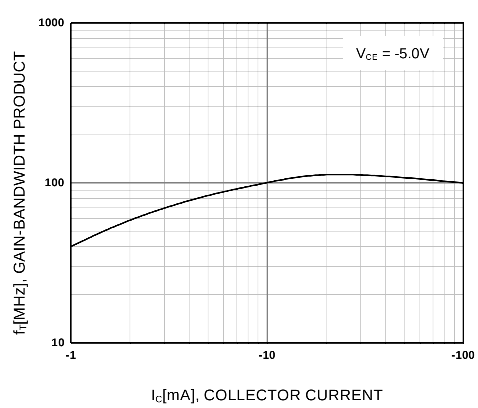
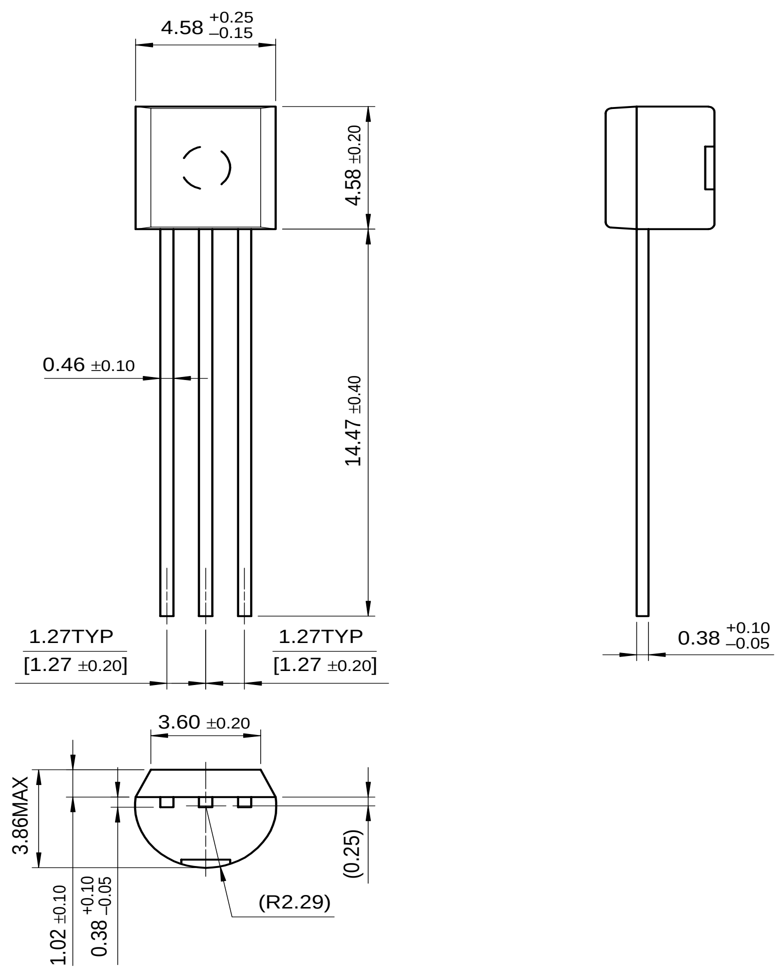


Figure 6. Gain Bandwidth Product

Package Dimensions

TO-92



Dimensions in Millimeters

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ActiveArray™	FACT Quiet series™	ISOPLANAR™	POP™	Stealth™
Bottomless™	FAST®	LittleFET™	Power247™	SuperSOT™-3
CoolFET™	FASTr™	MicroFET™	PowerTrench®	SuperSOT™-6
CROSSVOLT™	FRFET™	MicroPak™	QFET™	SuperSOT™-8
DOME™	GlobalOptoisolator™	MICROWIRE™	QS™	SyncFET™
EcoSPARK™	GTO™	MSX™	QT Optoelectronics™	TinyLogic™
E^2CMOS™	HiSeC™	MSXPro™	Quiet Series™	TruTranslation™
EnSigna™	I^2C™	OCX™	RapidConfigure™	UHC™
Across the board. Around the world.™		OCXPro™	RapidConnect™	UltraFET®
The Power Franchise™		OPTOLOGIC®	SILENT SWITCHER®	VCX™
Programmable Active Droop™		OPTOPLANAR™	SMART START™	

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

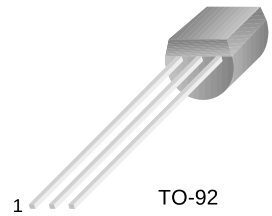
Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

FAIRCHILD SEMICONDUCTOR®

BC337/338

Switching and Amplifier Applications

- Suitable for AF-Driver stages and low power output stages
- Complement to BC327/BC328



TO-92

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NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_a=25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CES}	Collector-Emitter Voltage : BC337 : BC338	 50 30	 V V
V_{CEO}	Collector-Emitter Voltage : BC337 : BC338	 45 25	 V V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current (DC)	800	mA
P_C	Collector Power Dissipation	625	mW
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C

Electrical Characteristics T_a=25°C unless otherwise noted

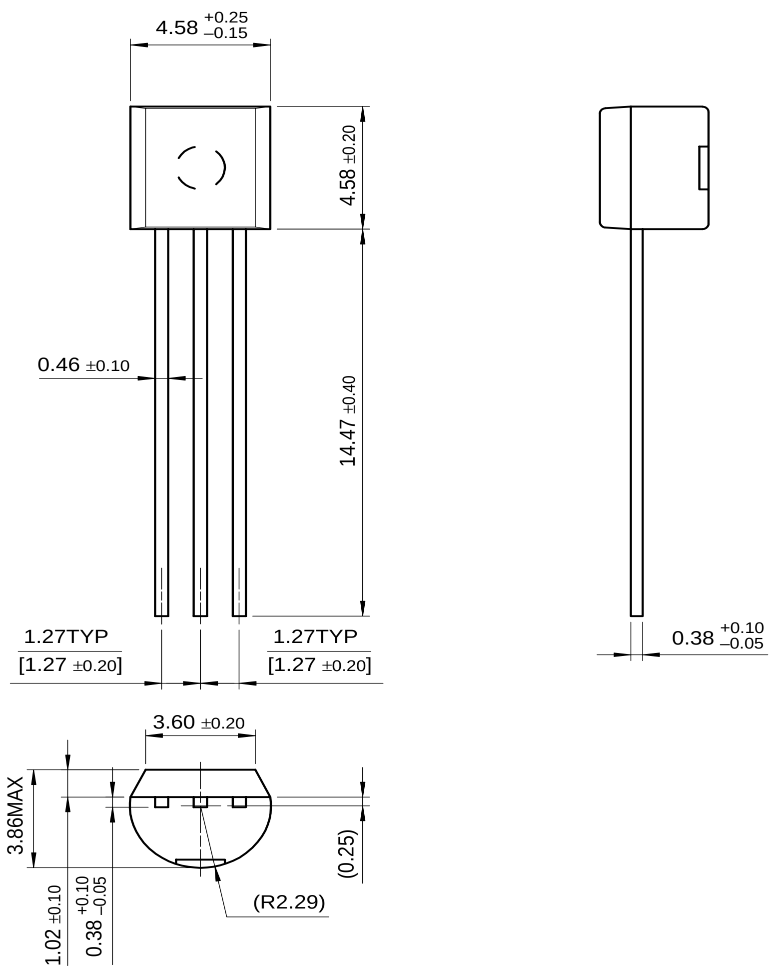
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BV_{CEO}	Collector-Emitter Breakdown Voltage : BC337 : BC338	I_C=10mA, I_B=0	 45 25			 V V
BV_{CES}	Collector-Emitter Breakdown Voltage : BC337 : BC338	I_C=0.1mA, V_{BE}=0	 50 30			 V V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E=0.1mA, I_C=0	5			V
I_{CES}	Collector Cut-off Current : BC337 : BC338	 V_{CE}=45V, I_B=0 V_{CE}=25V, I_B=0		 2 2	 100 100	 nA nA
h_{FE1} h_{FE2}	DC Current Gain	V_{CE}=1V, I_C=100mA V_{CE}=1V, I_C=300mA	100 60		630	
V_{CE} (sat)	Collector-Emitter Saturation Voltage	I_C=500mA, I_B=50mA			0.7	V
V_{BE} (on)	Base Emitter On Voltage	V_{CE}=1V, I_C=300mA			1.2	V
f_T	Current Gain Bandwidth Product	V_{CE}=5V, I_C=10mA, f=50MHz		100		MHz
C_{ob}	Output Capacitance	V_{CB}=10V, I_E=0, f=1MHz		12		pF

h_{FE} Classification

Classification	16	25	40
h_{FE1}	100 ~ 250	160 ~ 400	250 ~ 630
h_{FE2}	60-	100-	170-

Package Dimensions

TO-92



Dimensions in Millimeters

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ActiveArray™	FACT Quiet series™	ISOPLANAR™	POP™	Stealth™
Bottomless™	FAST®	LittleFET™	Power247™	SuperSOT™-3
CoolFET™	FASTr™	MicroFET™	PowerTrench®	SuperSOT™-6
CROSSVOLT™	FRFET™	MicroPak™	QFET™	SuperSOT™-8
DOME™	GlobalOptoisolator™	MICROWIRE™	QS™	SyncFET™
EcoSPARK™	GTO™	MSX™	QT Optoelectronics™	TinyLogic™
E^2CMOS™	HiSeC™	MSXPro™	Quiet Series™	TruTranslation™
EnSigna™	I^2C™	OCX™	RapidConfigure™	UHC™
Across the board. Around the world.™		OCXPro™	RapidConnect™	UltraFET®
The Power Franchise™		OPTOLOGIC®	SILENT SWITCHER®	VCX™
Programmable Active Droop™		OPTOPLANAR™	SMART START™	

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

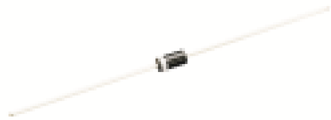
DC COMPONENTS CO., LTD.

RECTIFIER SPECIALISTS

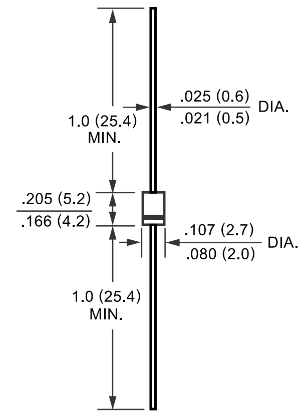
1N4001A / RL101
THRU
1N4007A / RL107

TECHNICAL SPECIFICATIONS OF SILICON RECTIFIER

VOLTAGE RANGE - 50 to 1000 Volts CURRENT - 1.0 Ampere



A-405



Dimensions in inches and (millimeters)

FEATURES

* High reliability
* Low leakage
* Low forward voltage drop
* High current capability

MECHANICAL DATA

* Case: Molded plastic
* Epoxy: UL 94V-0 rate flame retardant
* Lead: MIL-STD-202E, Method 208 guaranteed
* Polarity: Color band denotes cathode end
* Mounting position: Any
* Weight: 0.22 gram

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Ratings at 25 °C ambient temperature unless otherwise specified.
Single phase, half wave, 60 Hz, resistive or inductive load.
For capacitive load, derate current by 20%.

	SYMBOL	1N4001A RL101	1N4002A RL102	1N4003A RL103	1N4004A RL104	1N4005A RL105	1N4006A RL106	1N4007A RL107	UNITS
Maximum Recurrent Peak Reverse Voltage	V_{RRM}	50	100	200	400	600	800	1000	Volts
Maximum RMS Voltage	V_{RMS}	35	70	140	280	420	560	700	Volts
Maximum DC Blocking Voltage	V_{DC}	50	100	200	400	600	800	1000	Volts
Maximum Average Forward Rectified Current at T_A = 55°C	I_O	1.0							Amps
Peak Forward Surge Current, 8.3 ms single half sine-wave superimposed on rated load (JEDEC Method)	I_{FSM}	30							Amps
Maximum Instantaneous Forward Voltage at 1.0A DC	V_F	1.1							Volts
Maximum DC Reverse Current at Rated DC Blocking Voltage @T_A = 25°C	I_R	5.0							uAmps
Maximum DC Reverse Current at Rated DC Blocking Voltage @T_A = 100°C	I_R	500							uAmps
Maximum Full Load Reverse Current Average, Full Cycle .375*(9.5mm) lead length at T_L = 75°C	I_R	30							uAmps
Typical Junction Capacitance (Note)	C_J	15							pF
Typical Thermal Resistance	$R_{\theta JA}$	50							°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-65 to + 175							°C

NOTES : Measured at 1 MHz and applied reverse voltage of 4.0 volts

FIG. 1 - TYPICAL FORWARD CURRENT DERATING CURVE

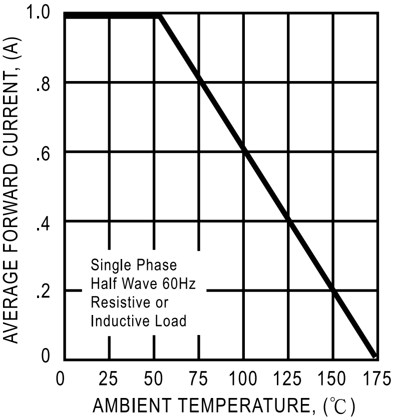


FIG. 2 - TYPICAL INSTANTANEOUS FORWARD CHARACTERISTICS

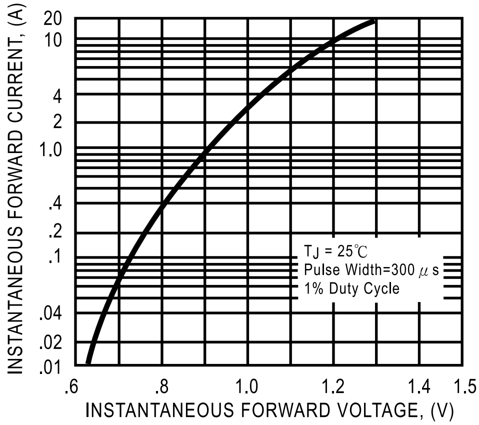


FIG. 3 - MAXIMUM NON-REPETITIVE FORWARD SURGE CURRENT

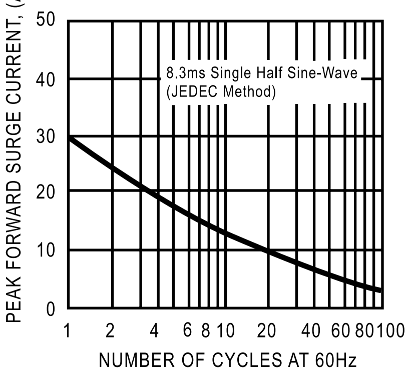


FIG. 4 - TYPICAL REVERSE CHARACTERISTICS

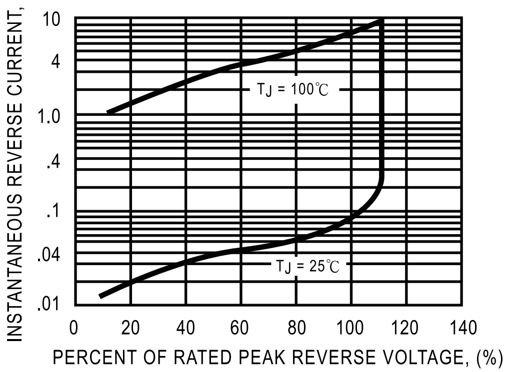
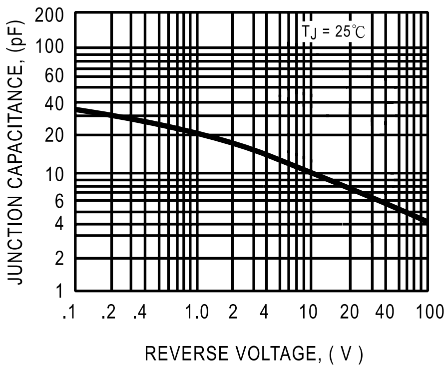


FIG. 5 - TYPICAL JUNCTION CAPACITANCE



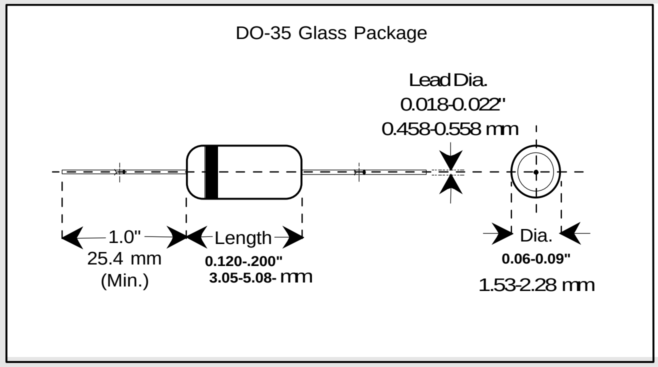
Silicon Switching Diode

1N914
or
1N914-1

DO-35 Glass Package

Applications

Used in general purpose applications, where performance and switching speed are important.



Features

- Six sigma quality
- Metallurgically bonded
- BKC's Sigma Bond™ plating for problem free solderability
- LL-34/35 MELF SMD available
- Full approval to Mil-S-19500/116
- Available up to JANTXV levels
- "S" level screening available to SCDs

Maximum Ratings	Symbol	Value	Unit
Peak Inverse Voltage	PIV	100 (Min.)	Volts
Average Rectified Current	I_{Avg}	75	mAmps
Continuous Forward Current	I_{Fdc}	300	mAmps
Peak Surge Current (t_{peak} = 1 sec.)	I_{peak}	0.5	Amp
Power Dissipation @ T_L=50 °C, L = 3/8" from body	P_{tot}	250	mWatts
Storage & Operating Temperature Range	$T_{St\ \&\ Op}$	-65 to +200	°C

Electrical Characteristics @ 25 °C*	Symbol	Absolute Limits	Unit
Breakdown Voltage @ Ir = 0.1 mA	PIV	100 (Min)	Volts
Reverse Leakage Current @ V_R = 20 V	I_R	0.025 (Max)	µA
Reverse Leakage (Vr =20 V, 150 °C)	I_R	50 (Max)	µA
Reverse Leakage Current @ V_R = 75 V	I_R	5.0 (Max)	µA
Capacitance @ V_R = 0 V, f = 1mHz	C_T	4.0 (Max)	pF
Reverse Recovery Time (note 1)	t_{rr}	4.0 (Max)	nSecs
Forward Recovery Time (note 2)	V_{fr}	2.5 (Max)	Volts

Note 1: I_F = 10 mA, R_L = 100 Ohms, Vr = 6.0 Volts , Irr =1.0 mA

Note 2: I_F = 50 mA dc

***UNLESS OTHERWISE SPECIFIED**

Microsemi

6 Lake Street - Lawrence, MA 01841

Tel: 978-681-0392 - Fax: 978-681-9135

DATA SHEET

NE/SA/SE555/SE555C
Timer

Product data
Supersedes data of 1994 Aug 31

2003 Feb 14

DESCRIPTION

The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA.

FEATURES

- Turn-off time less than 2 µs
- Max. operating frequency greater than 500 kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C

APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation

PIN CONFIGURATION

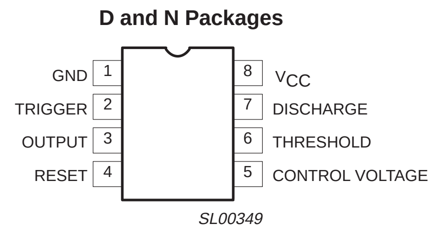


Figure 1. Pin configuration

BLOCK DIAGRAM

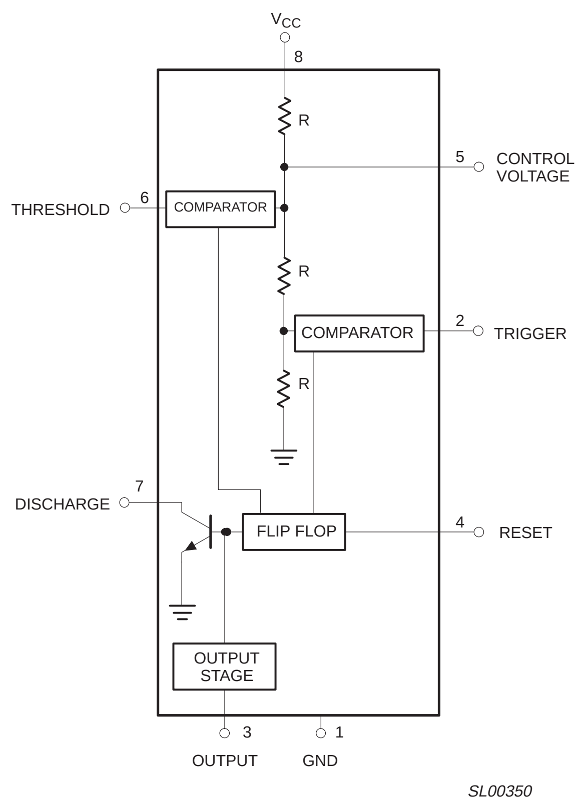


Figure 2. Block Diagram

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	0 to +70 °C	NE555D	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70 °C	NE555N	SOT97-1
8-Pin Plastic Small Outline (SO) Package	–40 °C to +85 °C	SA555D	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	–40 °C to +85 °C	SA555N	SOT97-1
8-Pin Plastic Dual In-Line Package (DIP)	–55 °C to +125 °C	SE555CN	SOT97-1
8-Pin Plastic Dual In-Line Package (DIP)	–55 °C to +125 °C	SE555N	SOT97-1

EQUIVALENT SCHEMATIC

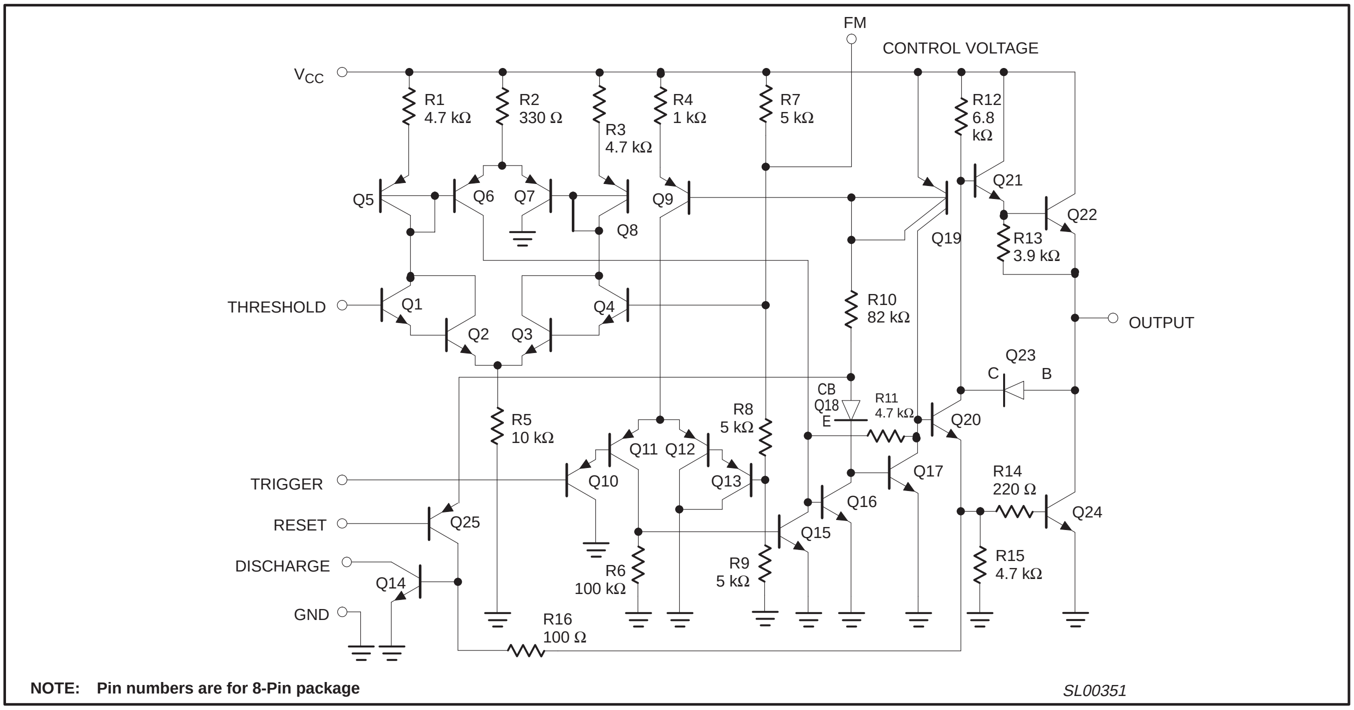


Figure 3. Equivalent schematic

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage SE555 NE555, SE555C, SA555	 +18 +16	 V V
P_D	Maximum allowable power dissipation[1]	600	mW
T_{amb}	Operating ambient temperature range NE555 SA555 SE555, SE555C	 0 to +70 –40 to +85 –55 to +125	 °C °C °C
T_{stg}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec max)	+230	°C

NOTE:
1. The junction temperature must be kept below 125 °C for the D package and below 150°C for the N package. At ambient temperatures above 25 °C, where this limit would be derated by the following factors:
   D package 160 °C/W
   N package 100 °C/W

DC AND AC ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C, V_{CC} = +5 V to +15 V unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE555			NE555/SA555/SE555C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		4.5		18	4.5		16	V
I_{CC}	Supply current (low state)[1]	V_{CC} = 5 V, $R_L = \infty$ V_{CC} = 15 V, $R_L = \infty$		3 10	5 12		3 10	6 15	mA mA
 t_M $\Delta t_M/\Delta T$ $\Delta t_M/\Delta V_S$	Timing error (monostable) Initial accuracy[2] Drift with temperature Drift with supply voltage	R_A = 2 kΩ to 100 kΩ C=0.1 μF		 0.5 30 0.05	 2.0 100 0.2		 1.0 50 0.1	 3.0 150 0.5	 % ppm/°C %/V
 t_A $\Delta t_A/\Delta T$ $\Delta t_A/\Delta V_S$	Timing error (astable) Initial accuracy[2] Drift with temperature Drift with supply voltage	R_A, R_B = 1 kΩ to 100 kΩ C = 0.1 μF V_{CC} = 15 V		 4 0.15	 6 500 0.6		 5 0.3	 13 500 1	 % ppm/°C %/V
V_C	Control voltage level	V_{CC} = 15 V V_{CC} = 5 V	9.6 2.9	10.0 3.33	10.4 3.8	9.0 2.6	10.0 3.33	11.0 4.0	V V
V_{TH}	Threshold voltage	V_{CC} = 15 V V_{CC} = 5 V	9.4 2.7	10.0 3.33	10.6 4.0	8.8 2.4	10.0 3.33	11.2 4.2	V V
I_{TH}	Threshold current[3]			0.1	0.25		0.1	0.25	μA
V_{TRIG}	Trigger voltage	V_{CC} = 15 V V_{CC} = 5 V	4.8 1.45	5.0 1.67	5.2 1.9	4.5 1.1	5.0 1.67	5.6 2.2	V V
I_{TRIG}	Trigger current	V_{TRIG} = 0 V		0.5	0.9		0.5	2.0	μA
V_{RESET}	Reset voltage[4]	V_{CC} = 15 V, V_{TH} = 10.5 V	0.3		1.0	0.3		1.0	V
I_{RESET}	Reset current Reset current	V_{RESET} = 0.4 V V_{RESET} = 0 V		0.1 0.4	0.4 1.0		0.1 0.4	0.4 1.5	mA mA
V_{OL}	LOW-level output voltage	V_{CC} = 15 V I_{SINK} = 10 mA I_{SINK} = 50 mA I_{SINK} = 100 mA I_{SINK} = 200 mA		 0.1 0.4 2.0 2.5	 0.15 0.5 2.2		 0.1 0.4 2.0 2.5	 0.25 0.75 2.5	 V V V V
		V_{CC} = 5 V I_{SINK} = 8 mA I_{SINK} = 5 mA		 0.1 0.05	 0.25 0.2		 0.3 0.25	 0.4 0.35	 V V
V_{OH}	HIGH-level output voltage	V_{CC} = 15 V I_{SOURCE} = 200 mA I_{SOURCE} = 100 mA	 13.0	 12.5 13.3		 12.75	 12.5 13.3		 V V
		V_{CC} = 5 V I_{SOURCE} = 100 mA	 3.0	 3.3		 2.75	 3.3		 V
t_{OFF}	Turn-off time[5]	V_{RESET} = V_{CC}		0.5	2.0		0.5	2.0	μs
t_R	Rise time of output			100	200		100	300	ns
t_F	Fall time of output			100	200		100	300	ns
	Discharge leakage current			20	100		20	100	nA

NOTES:
1. Supply current when output high typically 1 mA less.
2. Tested at V_{CC} = 5 V and V_{CC} = 15 V.
3. This will determine the max value of R_A+R_B, for 15 V operation, the max total R = 10 MΩ, and for 5 V operation, the max. total R = 3.4 MΩ.
4. Specified with trigger input HIGH.
5. Time measured from a positive-going input pulse from 0 to 0.8×V_{CC} into the threshold to the drop from HIGH to LOW of the output. Trigger is tied to threshold.

TYPICAL PERFORMANCE CHARACTERISTICS

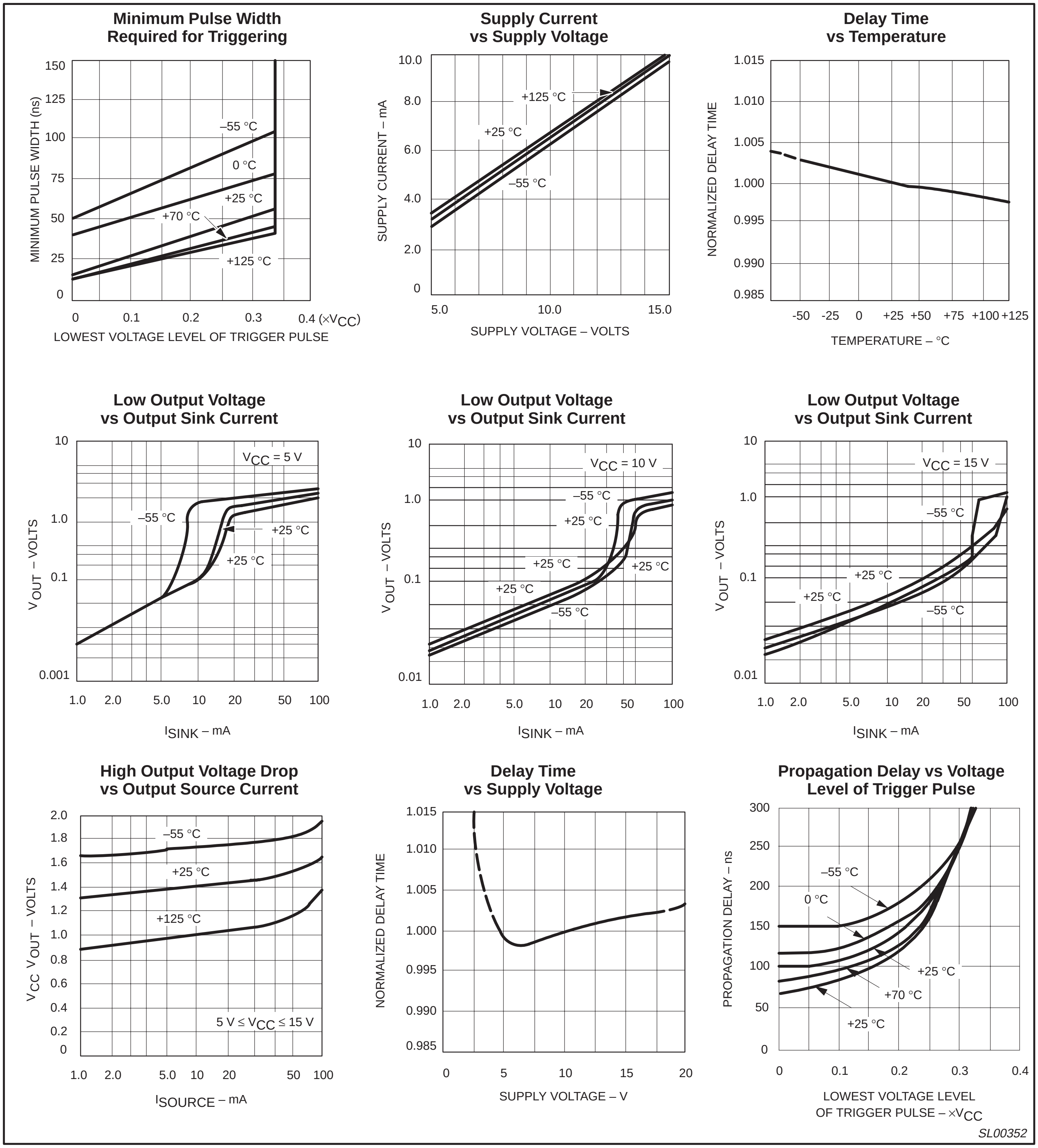
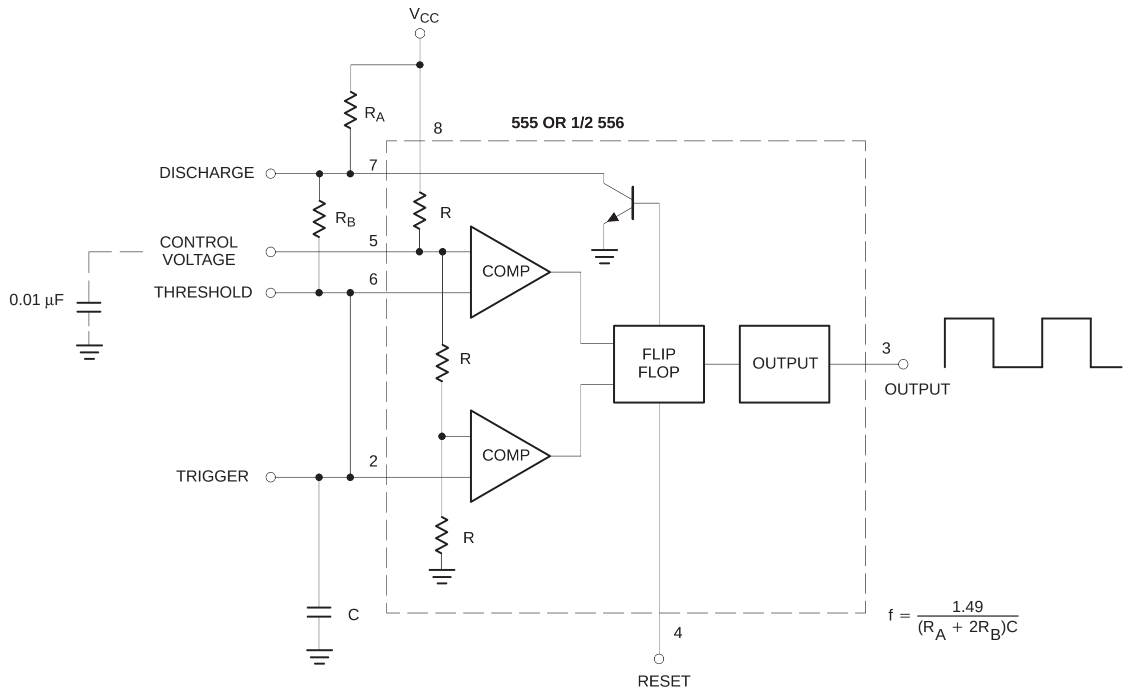
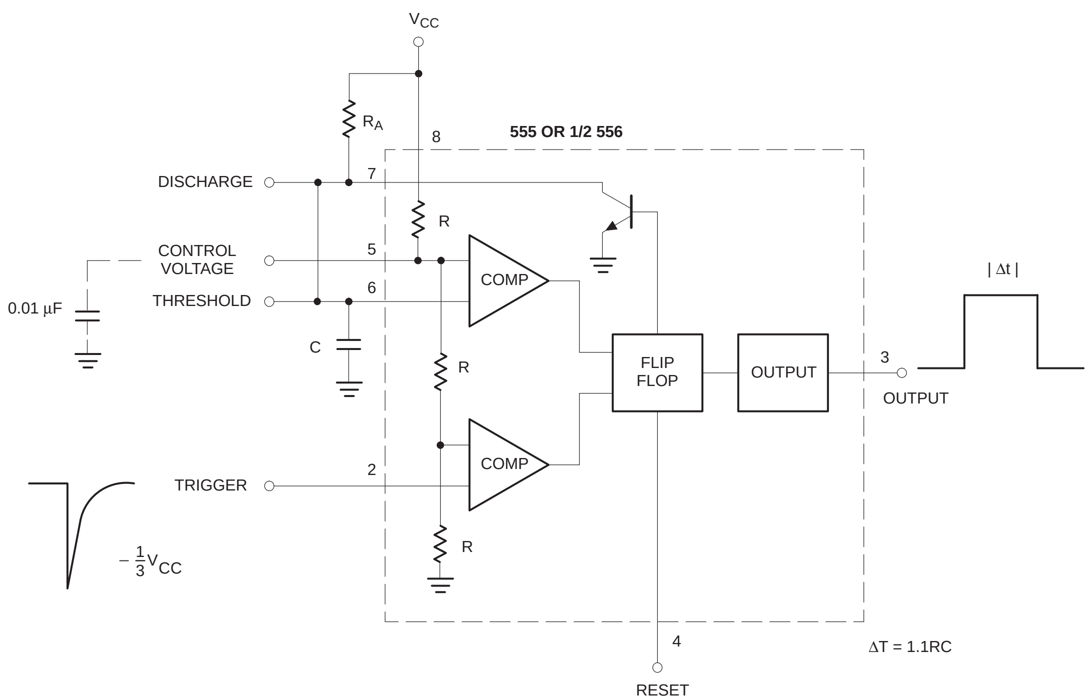


Figure 4. Typical Performance Characteristics

TYPICAL APPLICATIONS



Astable Operation



Monostable Operation

SL00353

Figure 5. Typical Applications

TYPICAL APPLICATIONS

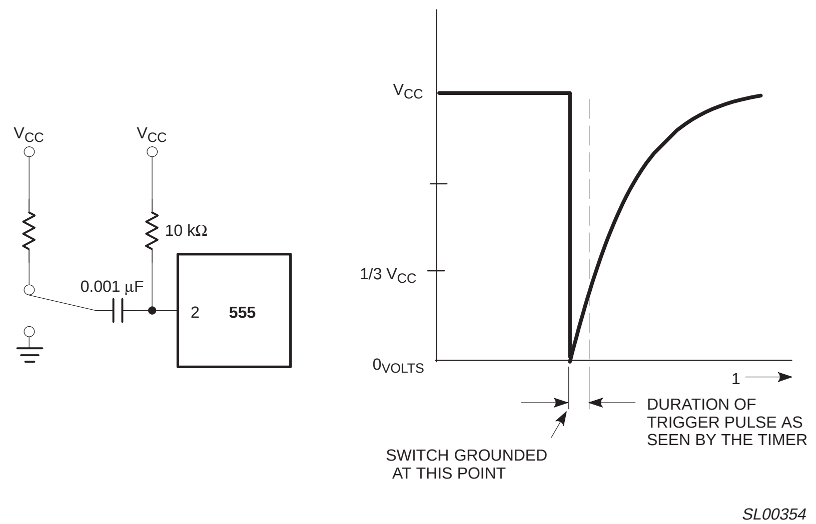


Figure 6. AC Coupling of the Trigger Pulse

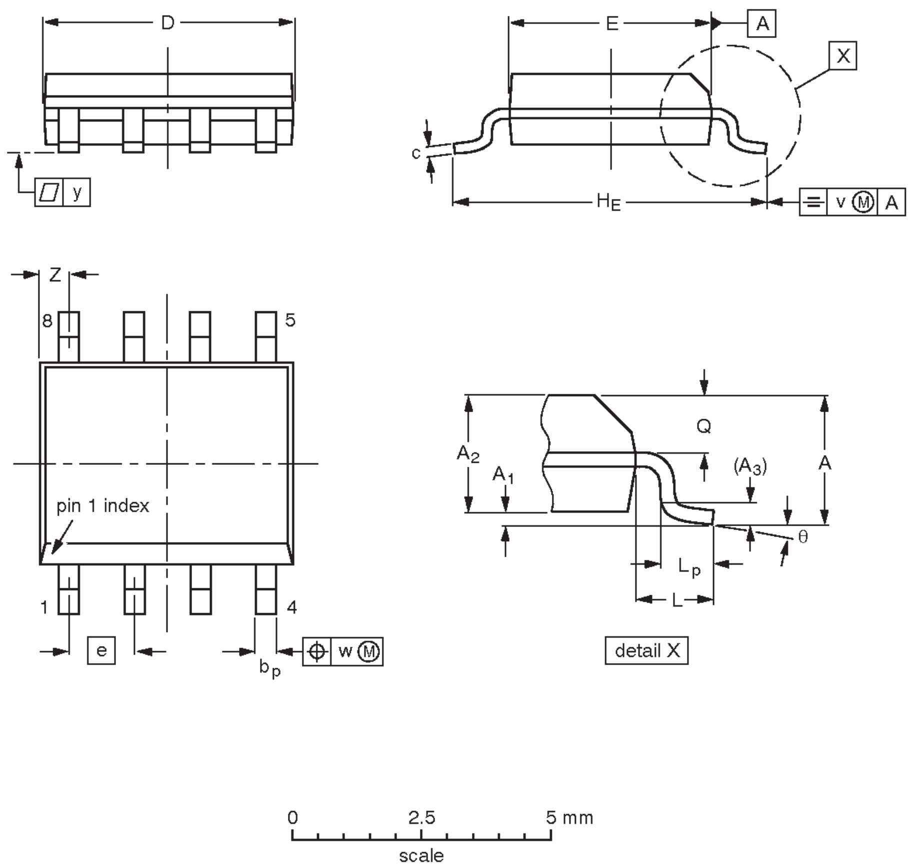
Trigger Pulse Width Requirements and Time Delays

Due to the nature of the trigger circuitry, the timer will trigger on the negative going edge of the input pulse. For the device to time out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the time out period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger, see Figure 6, a short negative going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle the output will remain in a high state for the duration of the low trigger signal, without regard to the threshold comparator state. This is due to the predominance of Q_{15} on the base of Q_{16}, controlling the state of the bi-stable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Another consideration is the “turn-off time”. This is the measurement of the amount of time required after the threshold reaches 2/3 V_{CC} to turn the output low. To explain further, Q_1 at the threshold input turns on after reaching 2/3 V_{CC}, which then turns on Q_5, which turns on Q_6. Current from Q_6 turns on Q_{16} which turns Q_{17} off. This allows current from Q_{19} to turn on Q_{20} and Q_{24} to given an output low. These steps cause the 2 µs max. delay as stated in the data sheet.

Also, a delay comparable to the turn-off time is the trigger release time. When the trigger is low, Q_{10} is on and turns on Q_{11} which turns on Q_{15}. Q_{15} turns off Q_{16} and allows Q_{17} to turn on. This turns off current to Q_{20} and Q_{24}, which results in output high. When the trigger is released, Q_{10} and Q_{11} shut off, Q_{15} turns off, Q_{16} turns on and the circuit then follows the same path and time delay explained as “turn off time”. This trigger release time is very important in designing the trigger pulse width so as not to interfere with the output signal as explained previously.

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**

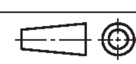


DIMENSIONS (inch dimensions are derived from the original mm dimensions)

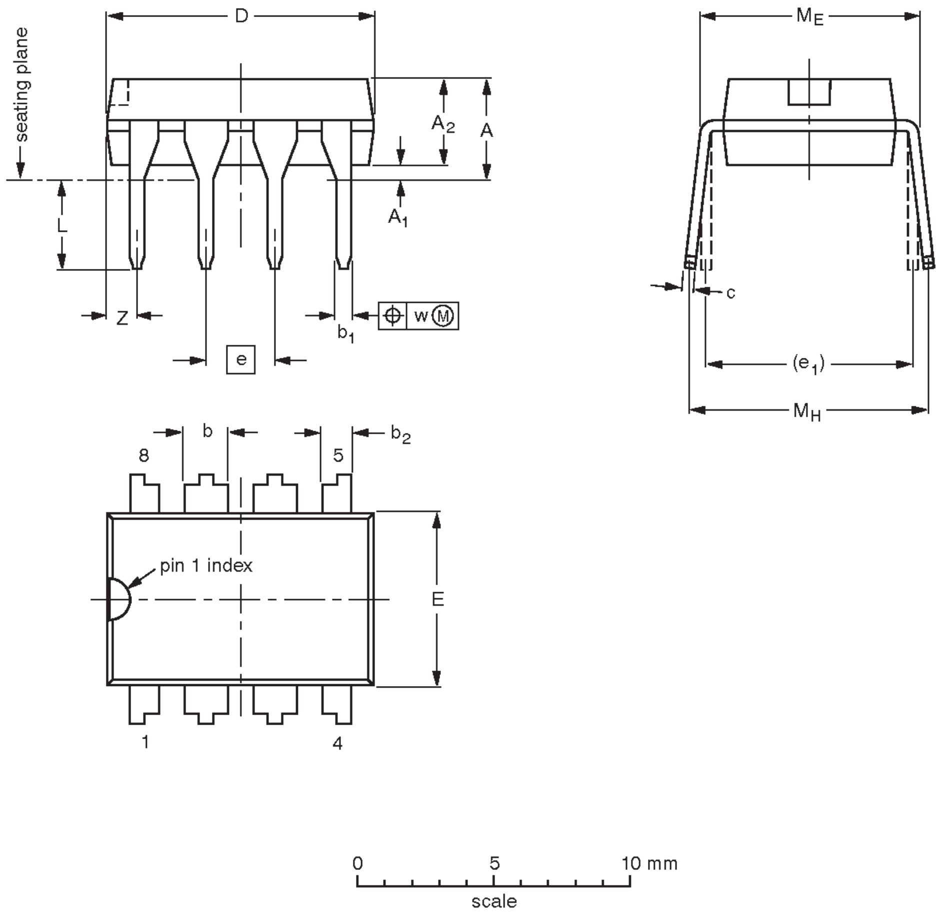
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				~~97-05-22~~ 99-12-27

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**

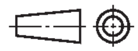


DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A1 min.	A2 max.	b	b1	b2	c	D (1)	E (1)	e	e1	L	ME	MH	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001	SC-504-8			~~95-02-04~~ 99-12-27

REVISION HISTORY

Rev	Date	Description
_2	20030214	**Product data (9397 750 11129); ECN 853-0036 29156 of 06 November 2002. Supersedes Product specification dated August 31, 1994.** Modifications: • Remove all cerdip information from the data sheet. Package type discontinued. • 'Absolute maximum ratings' table: T_{SOLD} rating changed from '+300 °C' to '+230 °C'.
	19940831	**Product specification; ECN 853-0036 13721 of 31 August 1994.** (Filename = NE_SA555X.pdf)

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contact information

For additional information please visit
http://www.semiconductors.philips.com. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com.

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